

[illegible]

Texas Instruments

DSP/Analog Technologies

1998 Seminar Series



Agenda

DAY 1: Digital Signal Processing

8:00–8:30 am	Registration
8:30–8:45 am	Your system considerations How TI's high-performance platforms, integrated development environment (IDE), and new devices are designed to meet your needs
8:45–10:15 am	How to work with TI's 'C6000
10:15–10:30 am	15-minute break
10:30–12:00	How to work with TI's 'C5000
12:00–1:00 pm	Lunch
1:00–2:15 pm	Part I: How TI's tools make your development easier A step-by-step, on-screen review of the development cycle in TI's state-of-the-art IDE
2:15–2:25 pm	10-minute break
2:25–3:10 pm	Part II: Tools Demo of audio application and real-time analysis
3:10–3:30 pm	Support available to you Conclusion and Q&A

All products described herein are subject to Seller's terms and conditions of sale and Seller's data book/sheet notices. Buyer is advised to obtain the most current information about Seller's products before placing orders.



TEXAS
INSTRUMENTS

World Leader



Mixed Signal/ Analog/ DSP Solutions

1

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



Mixed Signal/ Analog/ DSP Solutions

**While we can't claim to solve every problem,
we're solving lots of them by leveraging
our strengths**

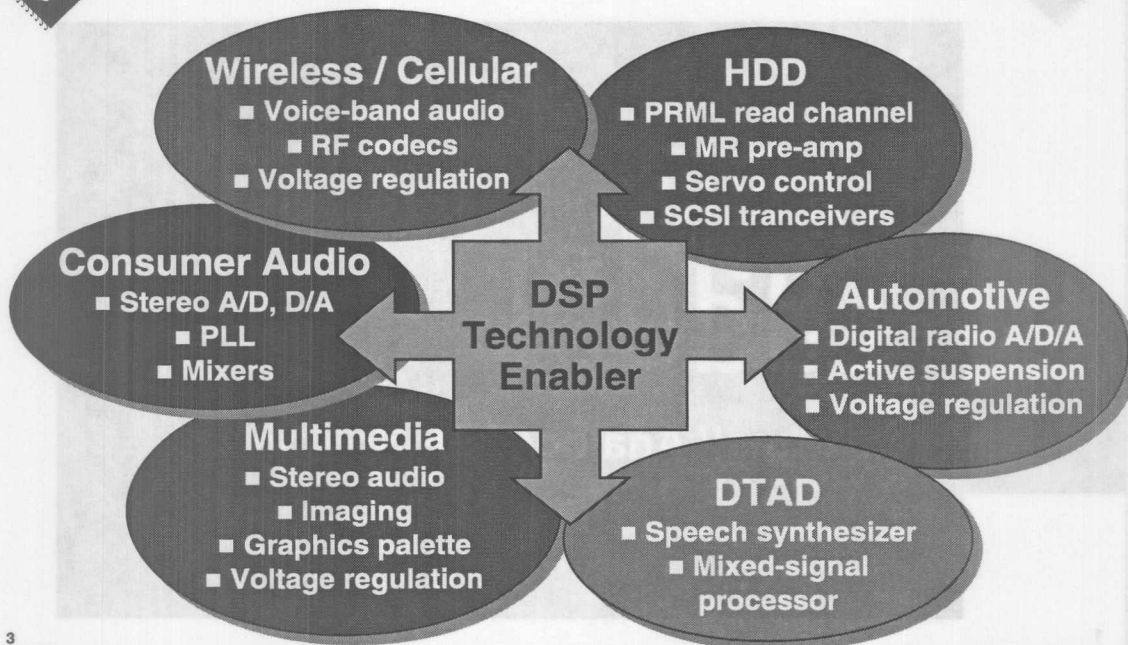
- Broad differentiated, optimized product range
- Leadership in both Analog and DSP technologies
- Hundreds of man-years developing industry's most effective debug and evaluation tools
- Extensive support – from TI and a worldwide network of third-party companies
- Investment in ongoing research
- Global university program
- Enablers for emerging markets

2

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

DSP/Analog: One stop shopping

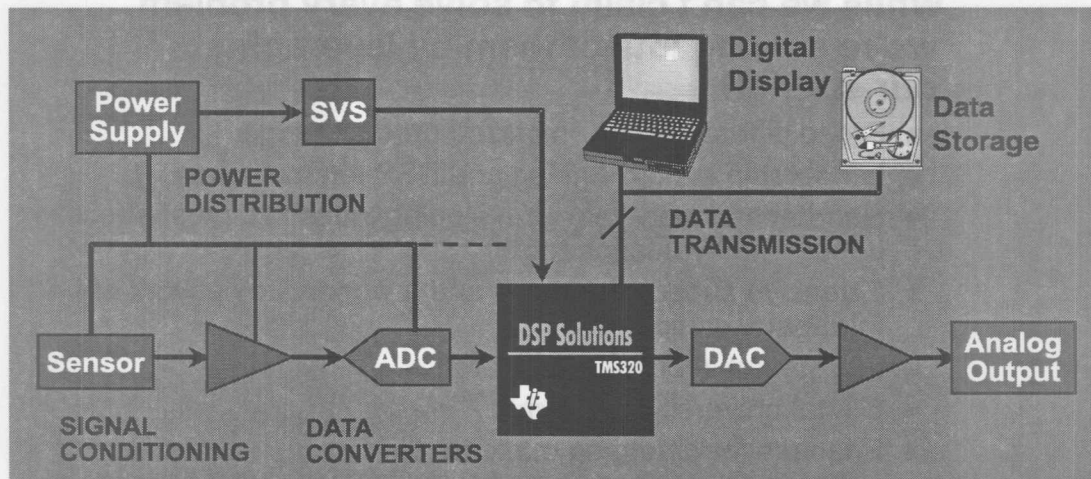


3

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

DSP/Analog: System solution



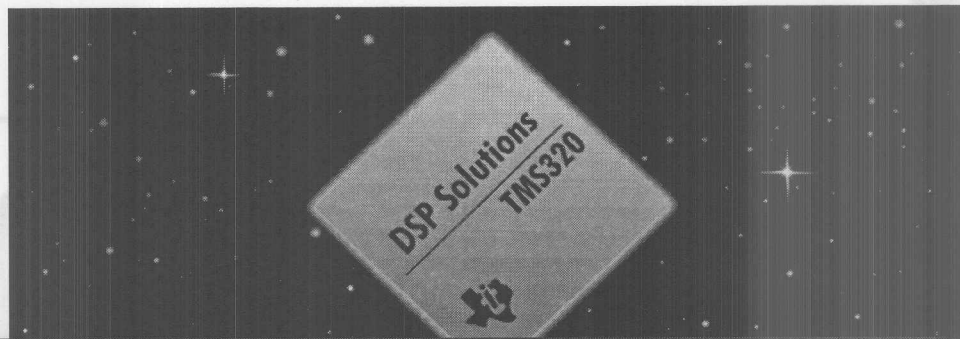
4

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



DSP Seminar: Our objective



Performance-intensive, real-time applications need the right optimized DSP... and an easy-to-use unified development environment

5

THE WORLD LEADER IN DSP SOLUTIONS



Today's Agenda

✓ What are my system requirements?

How do I work with TI's 'C6000?

How do I work with TI's 'C5000?

How do TI's tools make my development easier?

What support can I count on?

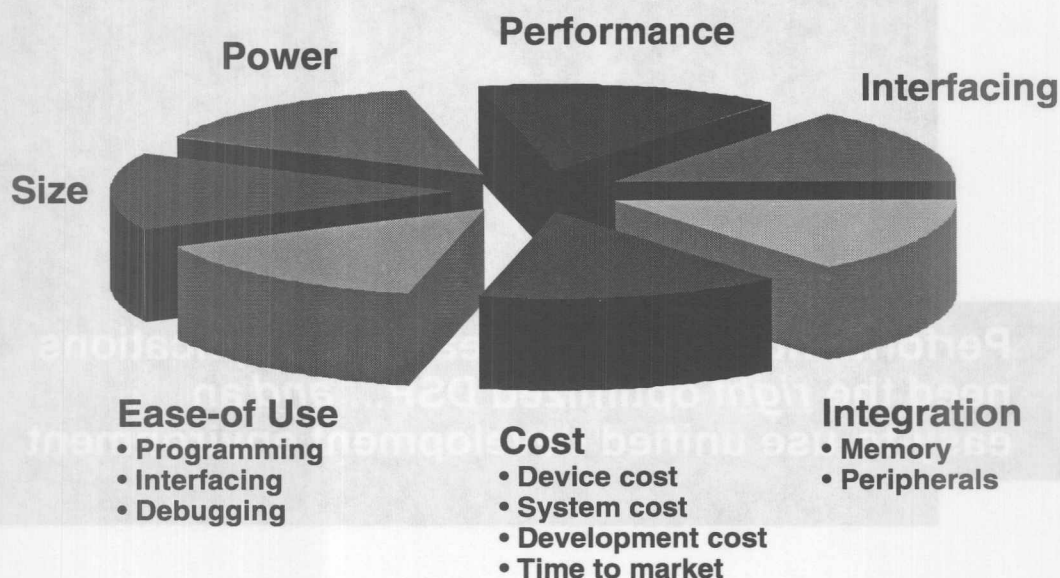
6

THE WORLD LEADER IN DSP SOLUTIONS





Tradeoffs: System requirements

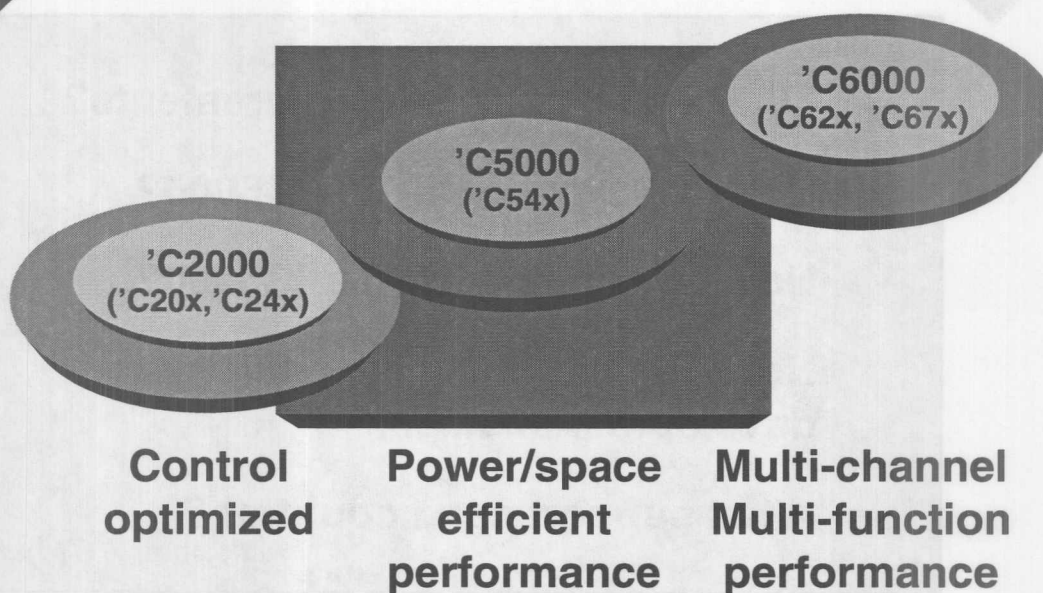


7

THE WORLD LEADER IN DSP SOLUTIONS



Three Platforms: For different needs



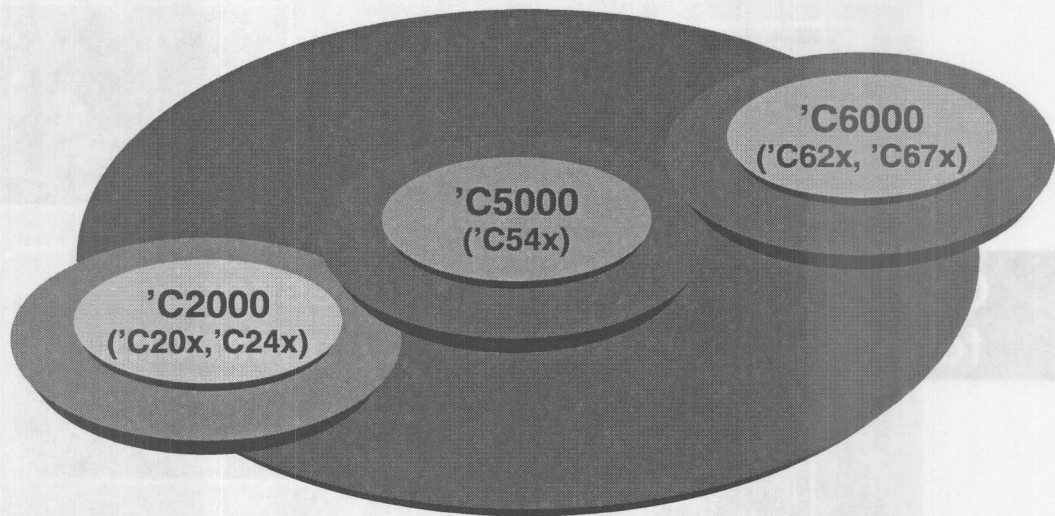
8

THE WORLD LEADER IN DSP SOLUTIONS





Unified development environment



Three ISAs. One Development Environment.

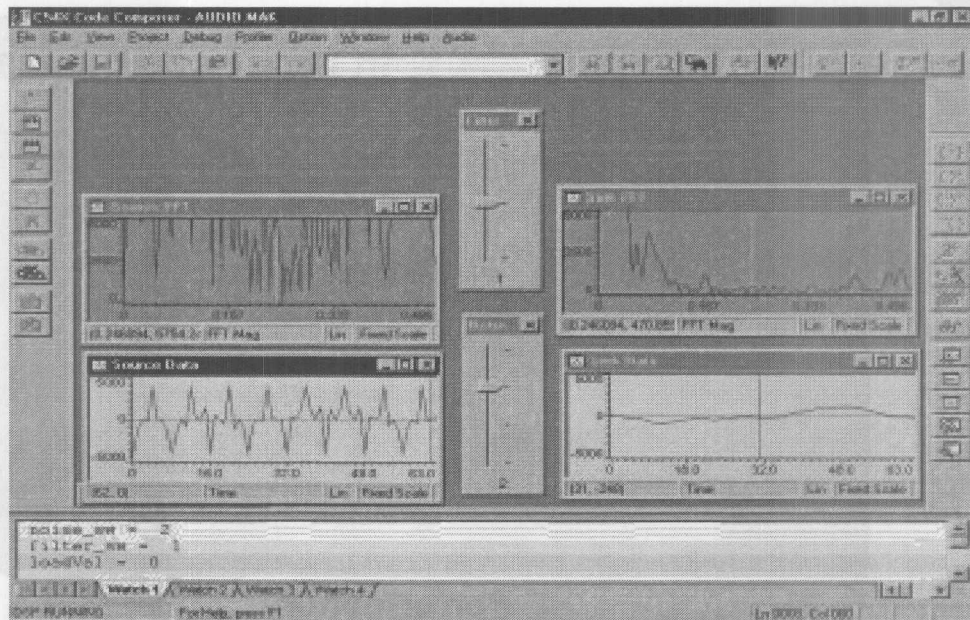


9

THE WORLD LEADER IN DSP SOLUTIONS



Tools: State-of-the-art IDE



10

THE WORLD LEADER IN DSP SOLUTIONS





'C2000: Optimized for control



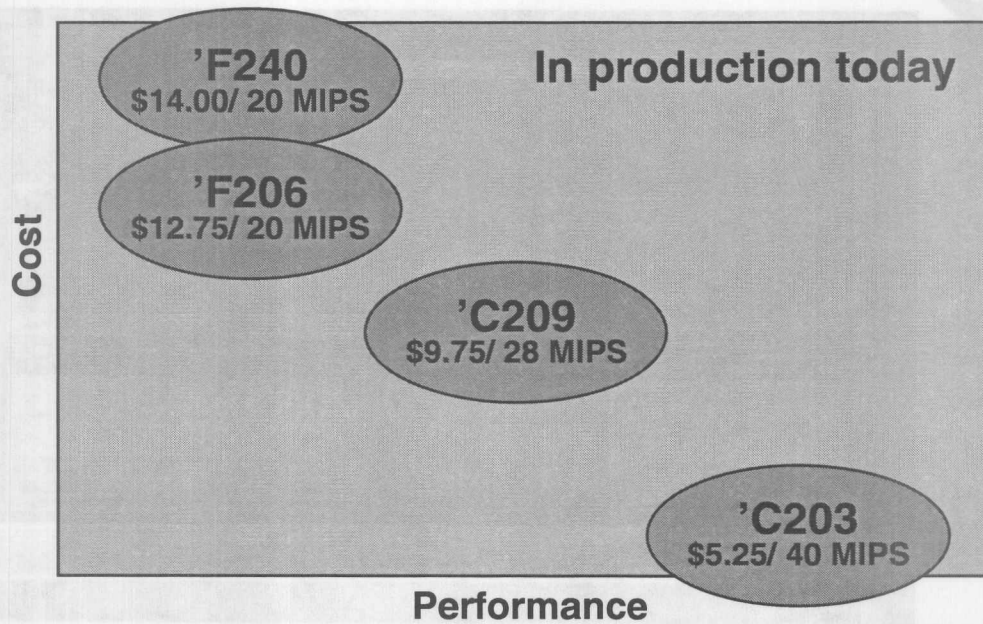
**Control + DSP in a uniprocessor
for embedded real-time applications**

11

THE WORLD LEADER IN DSP SOLUTIONS



'C2000: Optimized for control



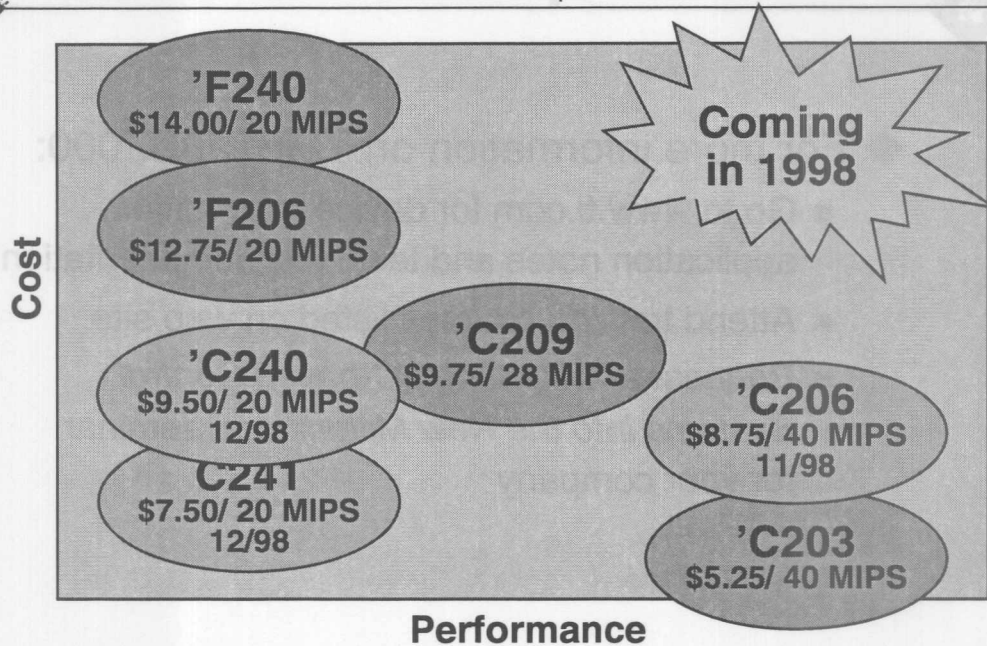
12

THE WORLD LEADER IN DSP SOLUTIONS





'C2000: As Low as \$5.25 for 40 MIPS

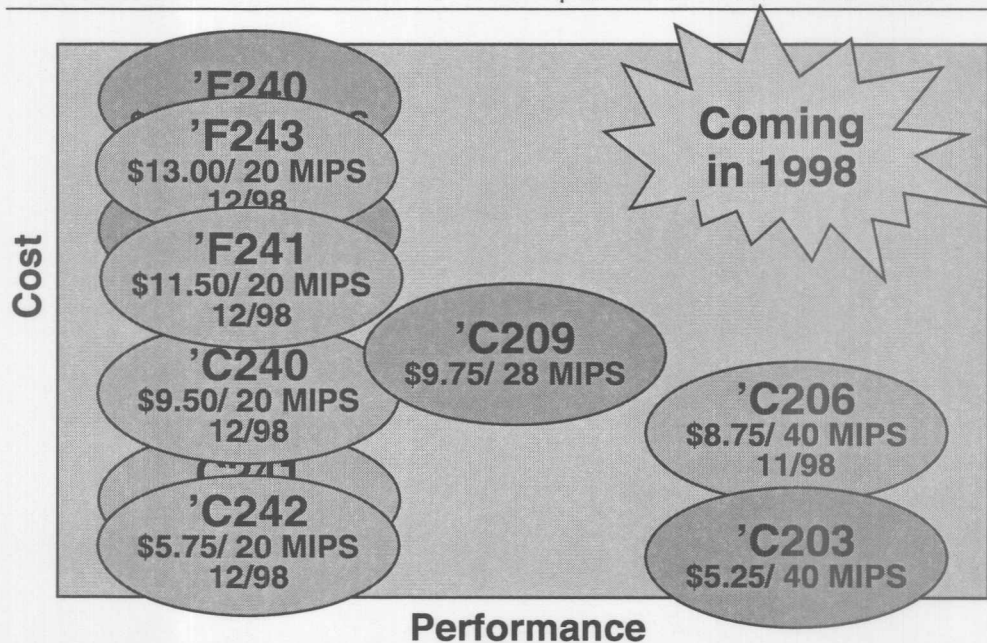


13 All dates are planned availability.

THE WORLD LEADER IN DSP SOLUTIONS



'C2000: As Low as \$5.25 for 40 MIPS



14 All dates are planned availability.

THE WORLD LEADER IN DSP SOLUTIONS





'C2000: Optimized for control

◆ For more information on TMS320C2000:

- Go to www.ti.com for device information, application notes and technical documentation
- Attend training courses listed on web site
- Request a *"Migrating μ C-based Control Systems into the New Millennium"* seminar for your company

15

THE WORLD LEADER IN DSP SOLUTIONS



'C5000: Power-efficient performance



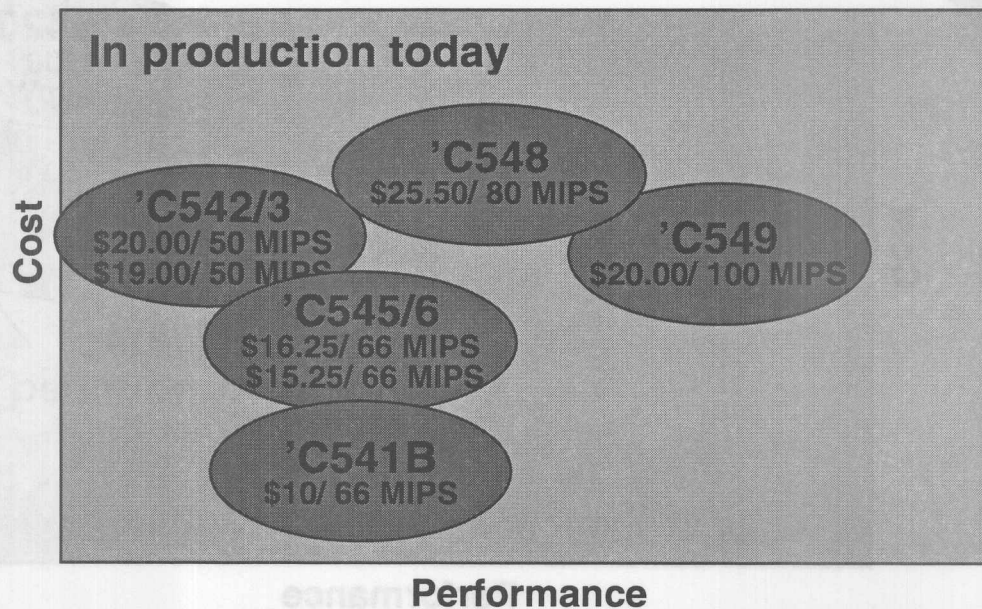
**Optimizing performance
in space/power/cost constraints**

16

THE WORLD LEADER IN DSP SOLUTIONS



'C5000: Power efficient performance



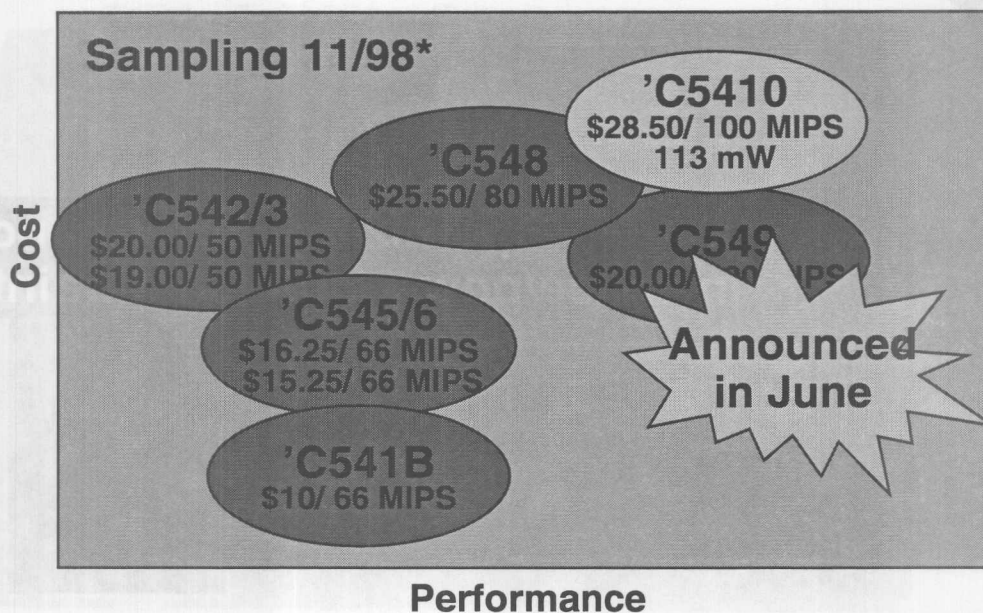
17

THE WORLD LEADER IN DSP SOLUTIONS





'C5000: Power efficient performance

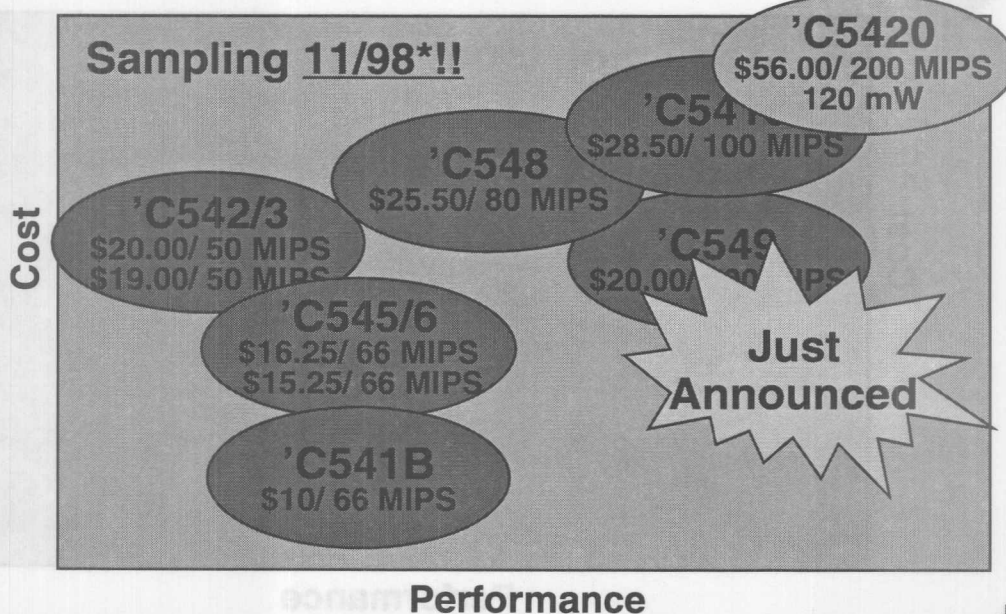


18 *Planned availability.

THE WORLD LEADER IN DSP SOLUTIONS



'C5000: Sub \$5 to 200 MIPS



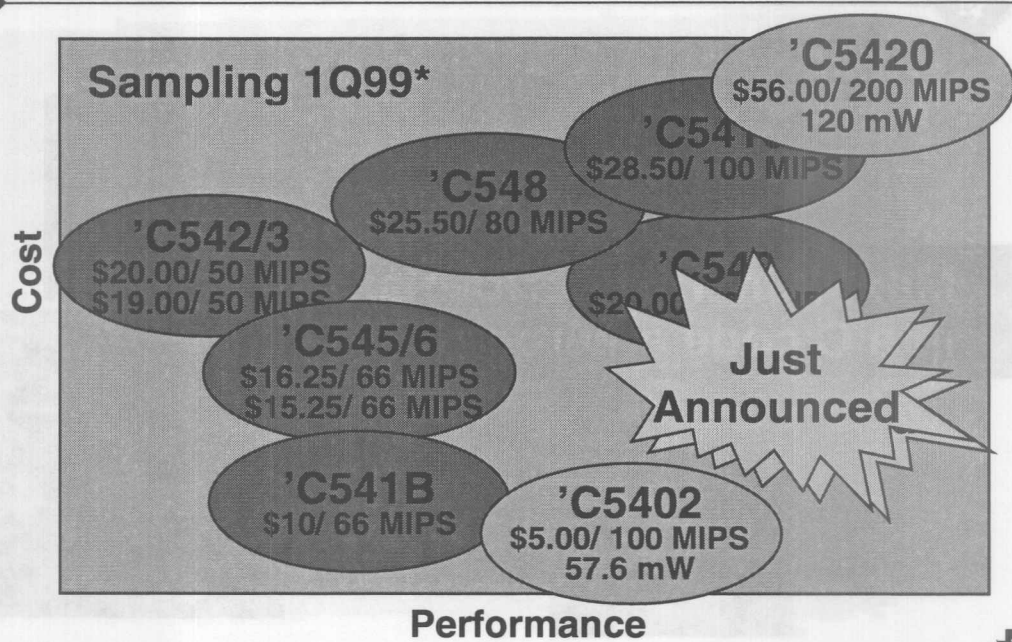
19 *Planned availability.

THE WORLD LEADER IN DSP SOLUTIONS





'C5000: Sub \$5 to 200 MIPS



20 *Planned availability.



THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



'C6000: Maximizing \$ / channel

Maximum raw performance
in a C code environment

21

THE WORLD LEADER IN DSP SOLUTIONS



'C6000: Maximizing \$ / channel

In production today

Cost

'C6201
\$96/ 1600 MIPS

Performance

22

THE WORLD LEADER IN DSP SOLUTIONS





'C6000: Maximizing \$ / channel

Cost

Samples available NOW!

'C6701
\$128/ 1 GFLOPS
1.9 W

Floating point

'C6201B
\$85/ 1600 MIPS
1.9 W

Performance

23

THE WORLD LEADER IN DSP SOLUTIONS



'C6000: \$25 to 2000 MIPS

Cost

Just
announced

'C6701
\$128/ 1 GFLOPS
1.9 W

'C6202
\$130/ 2000 MIPS
1.9 W

'C6201B
85/ 1600 MIPS
1.9 W

'C6211
\$25/ 1200 MIPS
1.5 W

Performance

24

THE WORLD LEADER IN DSP SOLUTIONS





Handouts: Full device listing

■ See your handout for a complete table of all TMS320C5000 and TMS320C6000 devices:

- ◆ Price
- ◆ Availability
- ◆ MIPS/MFLOPS
- ◆ Process technology
- ◆ On-chip memory
- ◆ Typical internal power consumption
- ◆ Clock rate
- ◆ Voltage
- ◆ Package
- ◆ Peripherals

■ Also see Selection Guide

25

THE WORLD LEADER IN DSP SOLUTIONS



TMS320C5000 Devices

	Price 1KU/ 25KU	TMX†	TMS†	MIPS/ MFLOPS**	Process Technol- ogy (μ)	RAM (words)	ROM	Typical Internal Power (CPU + Mem)	Clock Rate	Voltage (Int/ I/O)	Package	Peripherals
'C5402 ***** Announced (9/28/98)	\$5.00 / 25 KU \$7.50 / 1 KU	1Q99	2Q99	100	0.18	16K x 16	4K	57.6 mW	10 ns	1.8 V	144 / 144 BGA	2 McBSPs 1 HPI (8-bit) 6-ch DMA 2 Timers SW/PLL
'C541B	\$10.00 / 25 KU \$11.50 / 1 KU	—	Now	66	0.25	5K x 16	28K	98 mW	15 ns	3.3 V	TQFP 100	2 Serial ports 1 Timer SW/PLL
'C542	\$20.00 / 25 KU \$23.00 / 1 KU	—	Now	50	0.44	10K x 16	2K	165 mW	20 ns	3.3 V	TQFP 128/144	1 BSP 1 TDM 1 HPI (8-bit) 1 Timer PLL
'C543	\$19.00 / 25KU \$22.00 / 1 KU	—	Now	50	0.44	10K x 16	2K	165 mW	20 ns	3.3 V	TQFP 128/144	1 BSP 1 TDM 1 Timer PLL
'C545A	\$16.25 / 25 KU \$19.00 / 1 KU	—	Now	66	0.35	6K x 16	48K	131 mW	15 ns	3.3 V	TQFP 128	1 BSP 1 HPI (8-bit) 1 Timer SW/PLL
'C546A	\$15.25 / 25 KU \$17.75 / 1 KU	—	Now	66	0.35	6K x 16	48K	131 mW	15 ns	3.3 V	TQFP 100	1 BSP 1 HPI (8-bit) 1 Timer SW/PLL

Pricing is suggested resale as of 1/99

* McBSP is a multi-channel buffered serial port providing a glueless link to T1/E1 framer chips

** Fastest speed version

†All dates are planned availability, subject to change.

Updated 9/10/98

TMS320C5000 Devices

	Price 1KU/ 25KU	TMX†	TMS†	MIPS/ MFLOPS**	Process Technol- ogy (μ)	RAM (words)	ROM	Typical Internal Power (CPU + Mem)	Clock Rate	Voltage (Int/ I/O)	Package	Peripherals
'C548	\$25.50 / 25 KU \$29.75 / 1 KU	—	Now	80	0.35	32K x 16	2K	160 mW	12.5 ns	3.3 V	TQFP 144 BGA 144	2 BSPs 1 TDM 1 HPI (8-bit) 1 Timer SW/PLL
'C549	\$20.00 / 25 KU \$24.00 / 1 KU	—	Now	100	0.25	32K x 16	16K	113 mW	10 ns	3.3 V/ 2.5 V	TQFP 144 BGA 144	2 BSPs 1 TDM 1 HPI (8-bit) 1 Timer SW/PLL
'C5410 ***** Announced (June 98)	\$28.50 / 25 KU \$33.00 / 1 KU	11/98	2Q99	100	0.25	64K x 16	16K	113 mW	10 ns	2.5 V	TQFP 144 BGA 176	3 McBSPs 1 HPI (8-bit) 6-ch DMA 1 Timer SW/PLL
'C5420 ***** Announced (9/28/98)	\$56.00 / 25KU \$69.00 / 1 KU	11/98 ****	2Q99	200 (2 cores)	0.18	200K x 16	Ext Boot- loader	120 mW	10 ns (each core)	1.8 V	BGA 144	6 McBSPs 1 HPI (16-bit) 12-ch DMA 2 Timers SW/PLL

Pricing is suggested resale as of 1/99

* McBSP is a multi-channel buffered serial port providing a glueless link to T1/E1 framer chips

** Fastest speed version

†All dates are planned availability, subject to change.

Updated 9/10/98

TMS320C6000 Devices

	Price 1KU/ 25KU	TMX†	TMS†	MIPS/ MFLOPS**	Process Technol- ogy (μ)	RAM (words)	ROM	Typical Internal Power (CPU + Mem)	Clock Rate	Voltage (Int/ I/O)	Package	Peripherals
'C6201	\$ 96 / 25 KU \$135 / 1 KU	—	Now	1600	0.25	32K x 32	n/a	5 to 6 W	5 ns	2.5 V / 3.3 V	35 mm 352 BGA	2 McBSPs 1 HPI 4-ch DMA 2 Timers
'C6201B	\$ 85 / 25 KU \$105 / 1 KU	Now 35 mm 10/98 27 mm	1Q99 35 mm 1Q99 27 mm	1600	0.18	32K x 32	n/a	1.9 W	5 ns	1.8 V / 3.3 V	35 mm 352 BGA 27 mm 352 BGA	2 McBSPs 1 HPI 4-ch DMA 2 Timers
'C6202 ***** Announced (9/7/98)	\$130 / 25 KU 143 / 1 KU	1Q99	3Q99	2000	0.18	96K x 32	n/a	1.9 W	4 ns	1.8 V / 3.3 V	27 mm 352 BGA	2 McBSPs Exp bus 4-ch DMA 2 Timers
'C6211 ***** Announced (9/7/98)	\$ 25 / 25KU \$ 33 / 1 KU	2Q99	2H99	1200	0.18	18K x 32 New Dual-level cache	n/a	1.5 W	6.7 ns	1.8 V / 3.3 V	27 mm 256 BGA	2 McBSPs 1 HPI 16-ch enhanced DMA 2 Timers
'C6701	\$128 / 25 KU \$157 / 1 KU	10/98	2Q99	1 GFLOPS	0.18	32K x 32	n/a	1.9 W	6 ns	1.8 V / 3.3 V	35 mm 352 BGA	2 McBSPs 1 HPI 4-ch DMA 2 Timers

Pricing is suggested resale as of 1/99

* McBSP is a multi-channel buffered serial port providing a glueless link to T1/E1 framer chips

** Fastest speed version

†All dates are planned availability, subject to change.

Updated 9/10/98



Today's Agenda

✓ What are my system requirements?

✓ How do I work with TI's 'C6000?

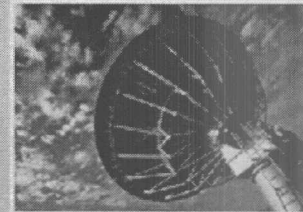
How do I work with TI's 'C5000?

How do TI's tools make my development easier?

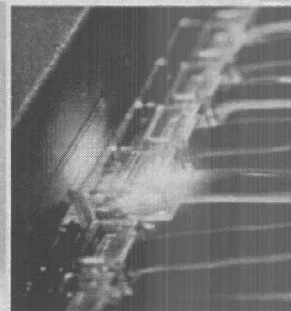
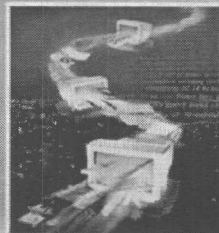
What support can I count on?

1

THE WORLD LEADER IN DSP SOLUTIONS



TMS320C6000

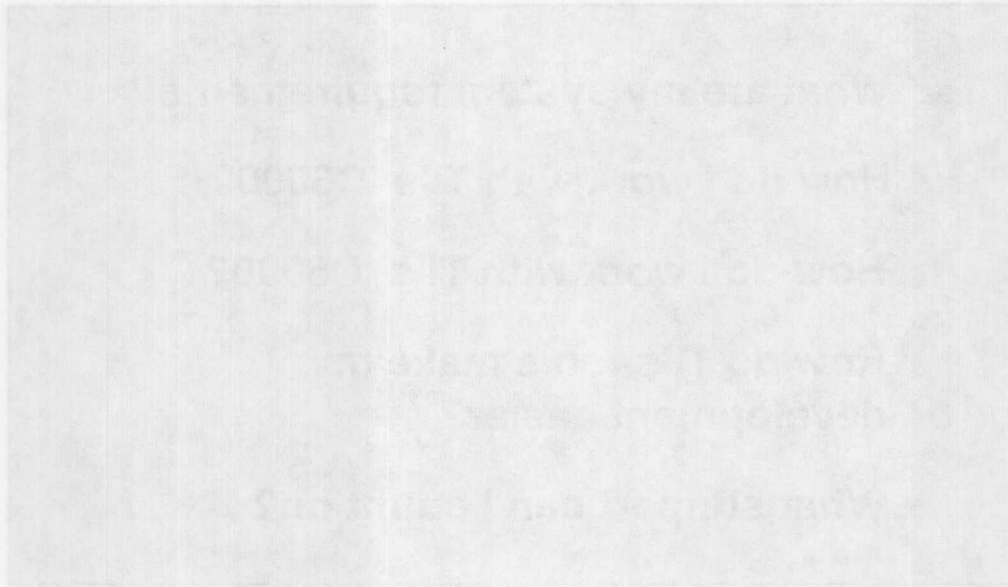


2

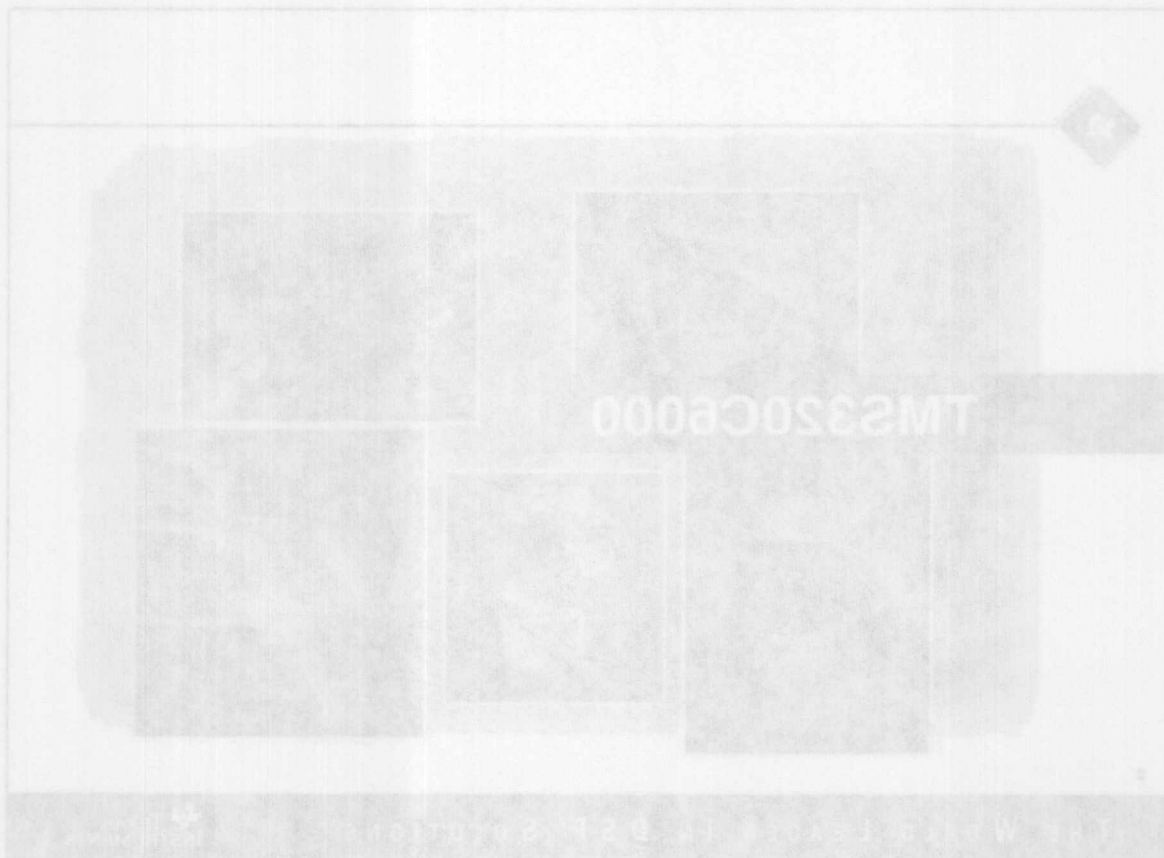
THE WORLD LEADER IN DSP SOLUTIONS



Today's Agenda



The World's Most Innovative Solutions





How do I work with TI's 'C6000?

What performance can I expect?

How do I get my performance?

How do I interface easily?

What are the new 'C6000 devices?

What is my power consumption?

How does TI enable maximum
performance at lower cost?

3

THE WORLD LEADER IN DSP SOLUTIONS



'C6000: Raw performance

1600 MIPS is a lot of MIPS.

But...

400 MMACS is a lot of processing.

Well, you're right... but...

But what matters to you is
how fast you can
process your algorithm, right?

Show me ...

4

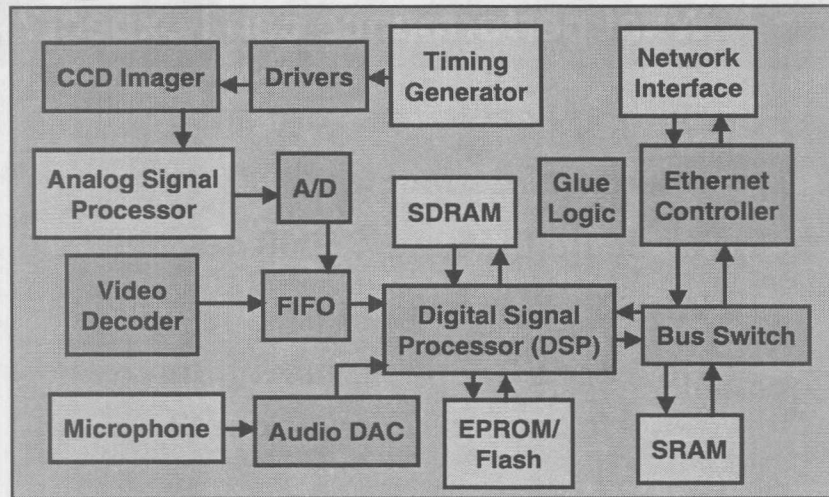
THE WORLD LEADER IN DSP SOLUTIONS





'C6000: Maximum raw performance

R&D: High-end network security camera system



5

TI devices available

THE WORLD LEADER IN DSP SOLUTIONS



For more information on full System Block Diagram, go to:
<http://www.ti.com/sc/docs/psheets/diagrams/netcam.htm>



'C6000: Maximizing multi-function

Imaging: Processing-intensive tasks

Algorithms required:

- Absolute difference threshold
- Morph dilation erosion
- Run length encoding
- Logical filtering
- JPEG compression at 10Hz
- Communications/tracking

>30 million instructions/frame

6



THE WORLD LEADER IN DSP SOLUTIONS





'C6201: Power of a workstation

**High-end UNIX
workstation**

**300 MHz
20 frame/sec**

320x240 image size

OR

'C6201

**200 MHz
30 frame/sec**

680x480 image size

**... with 600 MIPS
to spare**

6A

THE WORLD LEADER IN DSP SOLUTIONS



'C6000: Maximizing multi-channel

'C6201

**Channels
@ 200 MHz**

G.729A

30+

G.723.1

22+

G.726

50-80

**Echo Cancellation
(32-msec tail)**

51

GSM EFR

16+

EVRC

12

V.34/V.90

12-15

7

THE WORLD LEADER IN DSP SOLUTIONS

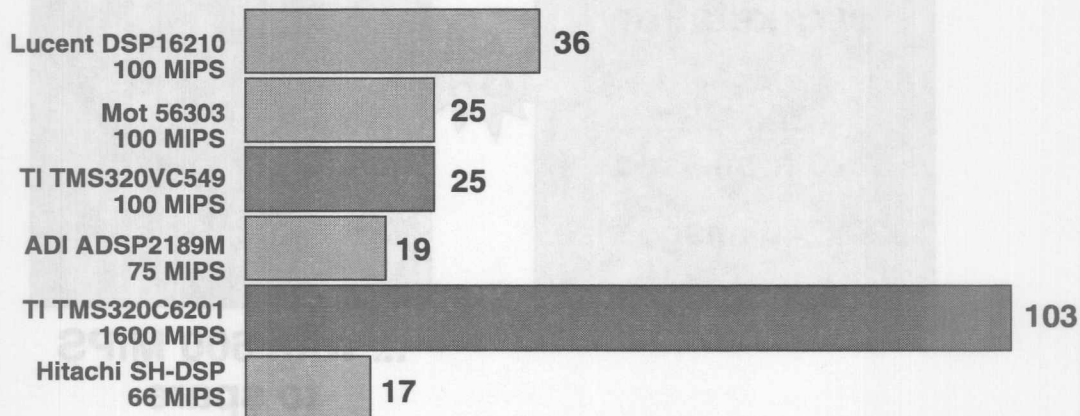




'C62x: Raw performance

BDTImark™: A DSP Speed Metric

Source www.BDTI.com. ©1999 BDTI



8

THE WORLD LEADER IN DSP SOLUTIONS



Source: www.BDTI.com. © 1999 Berkeley Design Technology, Inc.

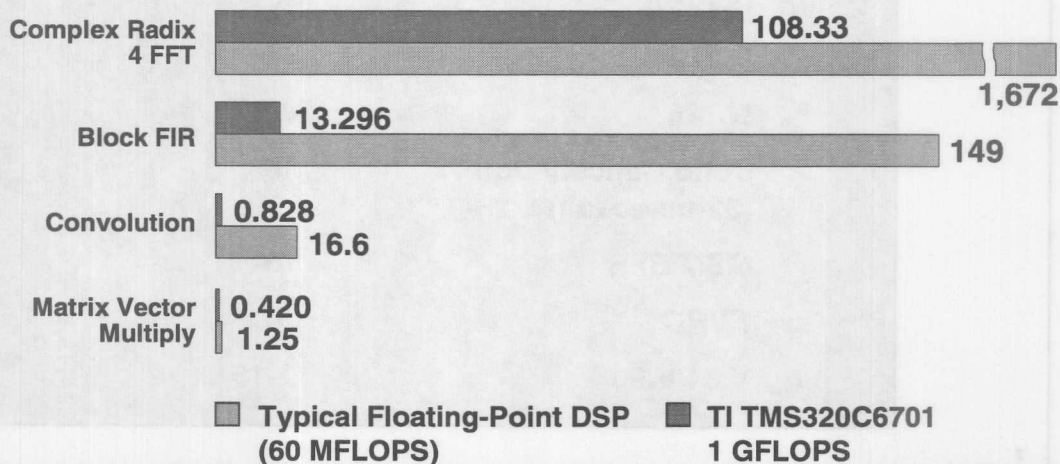
Additional benchmarks at: www.ti.com/sc/docs/dsps/products/c6000/c62x/benchmk.htm



'C67x: Raw performance

Floating-Point Performance

Execution time (in μ Sec)



9

THE WORLD LEADER IN DSP SOLUTIONS



For more TI benchmarks, please visit:

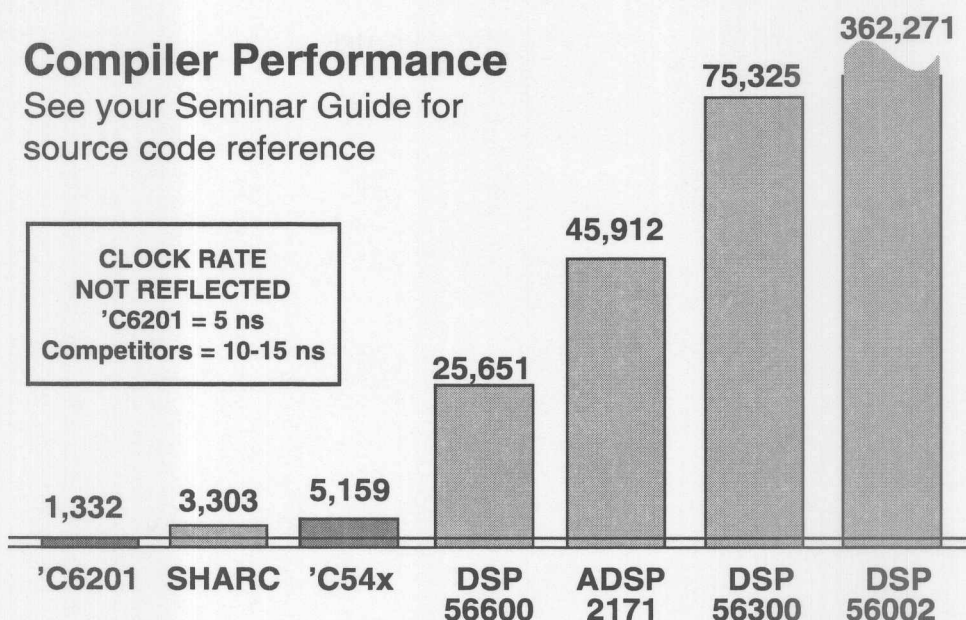
www.ti.com/sc/docs/dsps/products/c6000/c67x/c67bench.htm

'C6000 Compiler: Lowest cycle count

Compiler Performance

See your Seminar Guide for
source code reference

CLOCK RATE
NOT REFLECTED
'C6201 = 5 ns
Competitors = 10-15 ns



10 Source: TI internal testing on source code referenced in Seminar Guide.

THE WORLD LEADER IN DSP SOLUTIONS

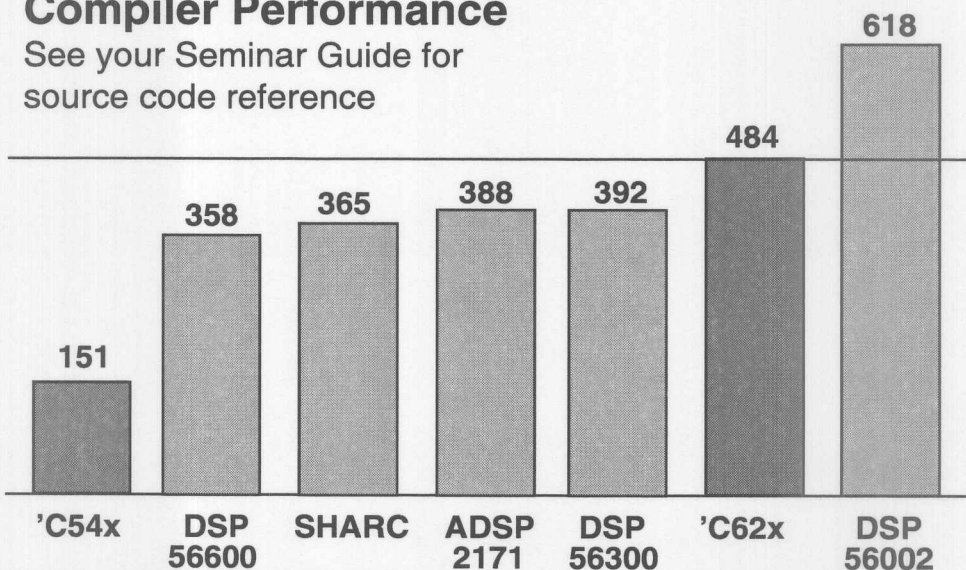


Reference: Public Domain C Source Code
www.ednmag.com/reg/1997/060597/12df.02.cfm

'C6000 Compiler: Average byte count

Compiler Performance

See your Seminar Guide for
source code reference



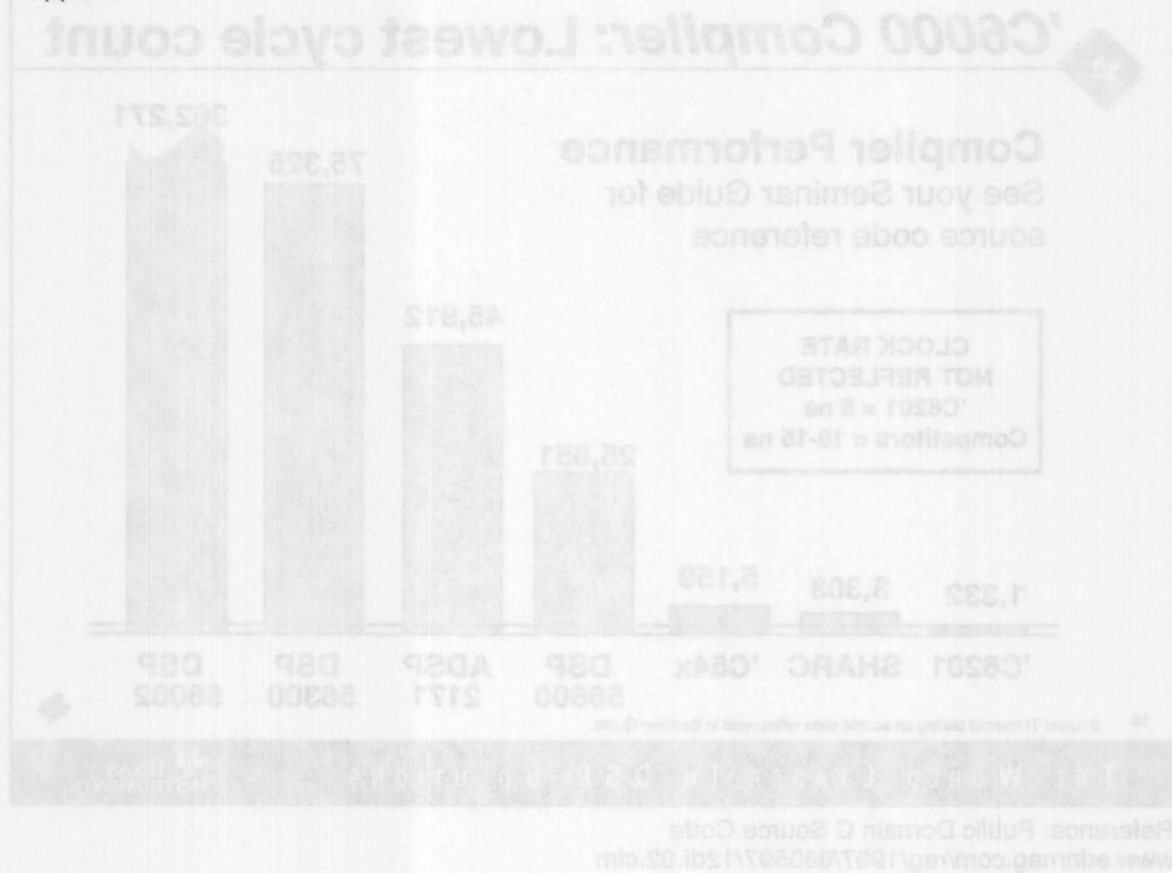
11 Source: TI internal testing on source code referenced in Seminar Guide.

THE WORLD LEADER IN DSP SOLUTIONS



Reference: Public Domain C Source Code
www.ednmag.com/reg/1997/060597/12df.02.cfm

For a list of related application reports, white papers, and Designer Notebook Pages, see the Appendix.





How do I work with TI's 'C6000?

What performance can I expect?

How do I get my performance?

How do I interface easily?

What are the new 'C6000 devices?

What is my power consumption?

How does TI enable maximum performance at lower cost?

12

THE WORLD LEADER IN DSP SOLUTIONS



'C6000: Built for speed

What kind of architecture...

- ◆ Enables 5 ns clock rate and 2000 MIPS?
- ◆ Enables future clock rates of 1 ns or 10,000 MIPS?

... and allows you to access all this in C code?



THE WORLD LEADER IN DSP SOLUTIONS

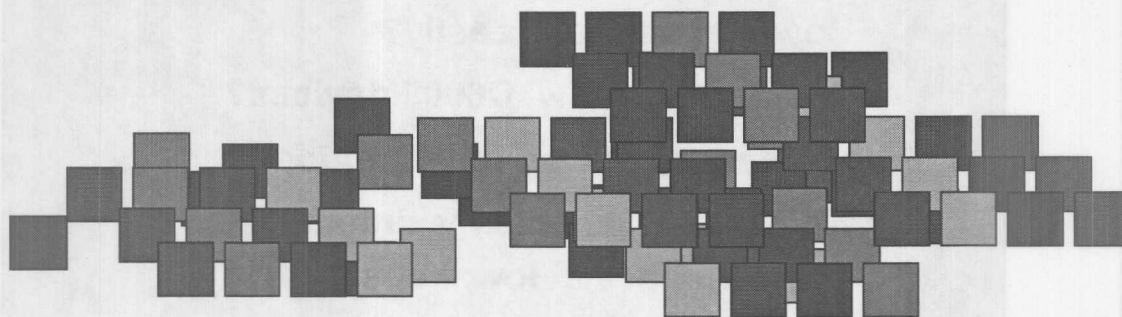




Concept: Built for speed

An environment that enables speed might have:

- ◆ Lots of blocks that can be moved easily
- ◆ Few restrictions on what order they are placed
- ◆ A machine designed to move them quickly
- ◆ Ability to do as much as possible, simultaneously



14

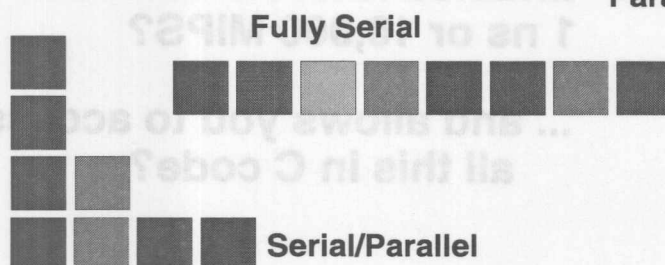


THE WORLD LEADER IN DSP SOLUTIONS



VelociTI™: Speed with efficiency

- ◆ **Execute:** CPU executes 1 to 8 instructions/cycle
- ◆ As a result, fetch packets can contain multiple execute packets
- ◆ Parallelism is determined at compile/assembly time



Fully
Parallel

Fully Serial

Serial/Parallel

15

THE WORLD LEADER IN DSP SOLUTIONS

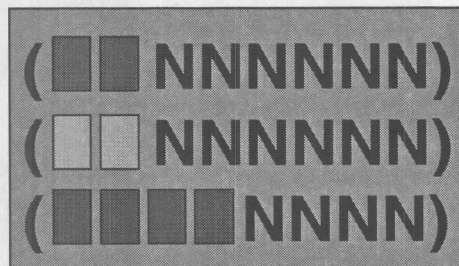




VelociTI™: Advanced VLIW

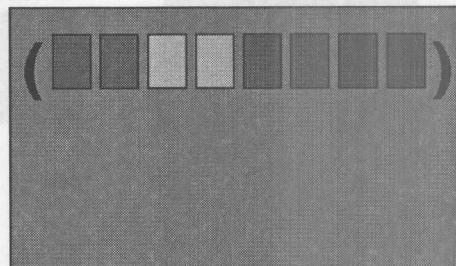
Fetch: CPU fetches 8 instructions/cycle (256 bits)

Traditional VLIW:



8 instructions x 32 bits
...plus NOPs

VelociTI:



8 instructions x 32 bits
...with minimal NOPs

16



THE WORLD LEADER IN DSP SOLUTIONS



'C6000: Sum of Products example

How is 'C6000
designed to
handle
math-intensive
calculations?

$$Y = \sum_{n=1}^{40} a_n * x_n$$

Let's look at the
two basic instructions
required by a MAC --
DSP's fundamental
algorithm...

- Multiply
- Add

17



THE WORLD LEADER IN DSP SOLUTIONS





SOP Example: Add

Where
are the
variables
stored?

.M

.L

$$Y = \sum_{n=1}^{40} a_n * x_n$$

MPY
ADD

a, x, prod
Y, prod, Y

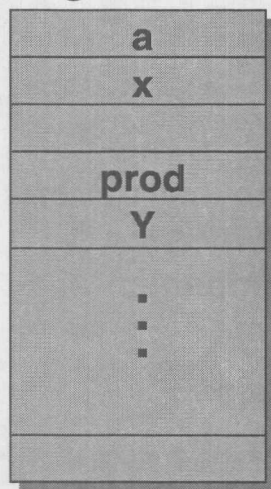
18

THE WORLD LEADER IN DSP SOLUTIONS



SOP Example: Add

Register File A



32 bits

$$Y = \sum_{n=1}^{40} a_n * x_n$$

MPY
ADD

a, x, prod
Y, prod, Y

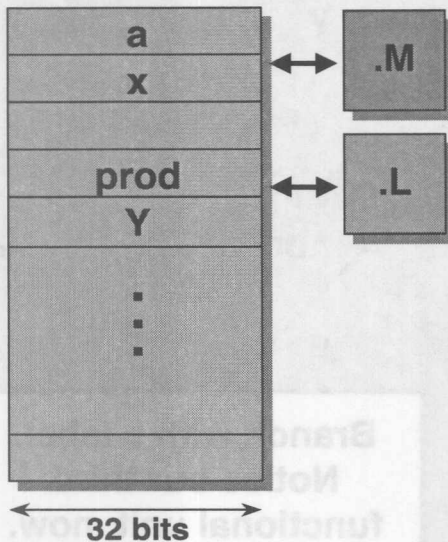
19

THE WORLD LEADER IN DSP SOLUTIONS



SOP Example: Next, a loop

Register File A



$$Y = \sum_{n=1}^{40} a_n * x_n$$

MPY a, x, prod
ADD Y, prod, Y

Now, we need a loop

20

THE WORLD LEADER IN DSP SOLUTIONS



SOP Example: Creating a loop

1. Add branch instruction (B) and a label

B loop

2. Create a loop counter (= 40) counter

MVK 40, ctr

3. Add an instruction to decrement the loop counter

SUB ctr, 1, ctr

21

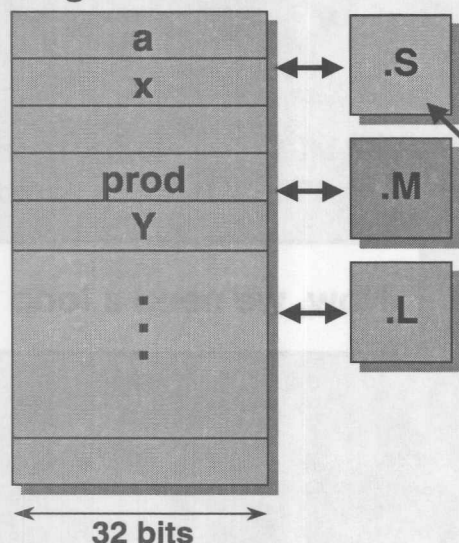
THE WORLD LEADER IN DSP SOLUTIONS



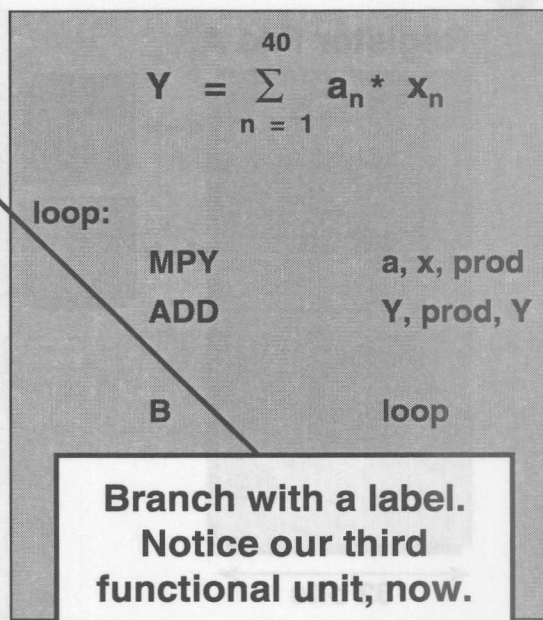


SOP Example: Decrement counter

Register File A



22

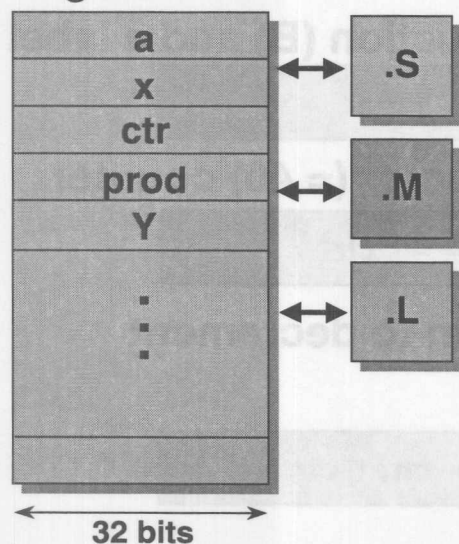


THE WORLD LEADER IN DSP SOLUTIONS

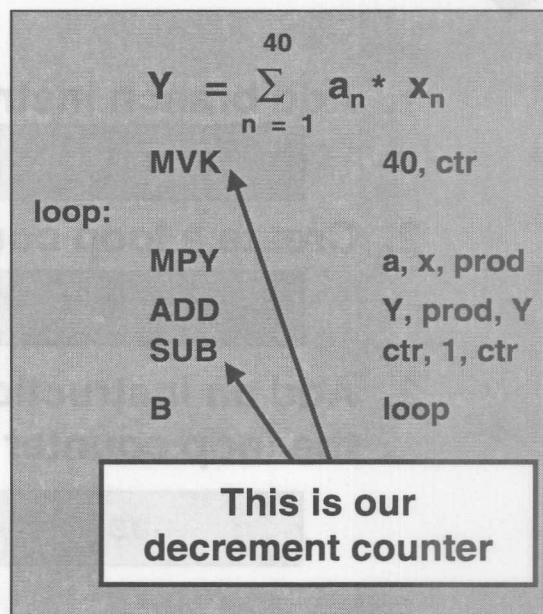


SOP Example: Decrement counter

Register File A



23

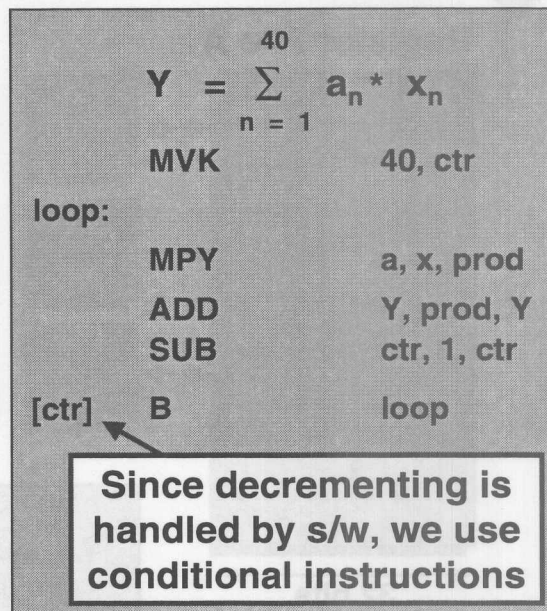
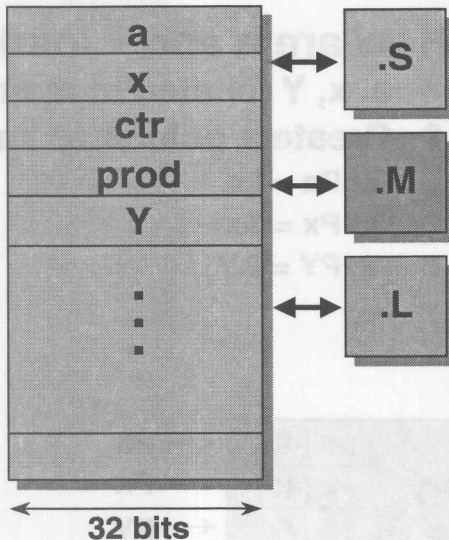


THE WORLD LEADER IN DSP SOLUTIONS



SOP Example: Decrement counter

Register File A



24

THE WORLD LEADER IN DSP SOLUTIONS



'C6000: 100% conditional instructions

[condition] B loop

**In order to reduce branching,
all instructions are conditional**
based on zero or nonzero values
of condition variables.

Code Syntax

Execute instruction if :

[ctr]

ctr ≠ 0

[!ctr]

ctr = 0

Note: if condition is false, NOP is executed

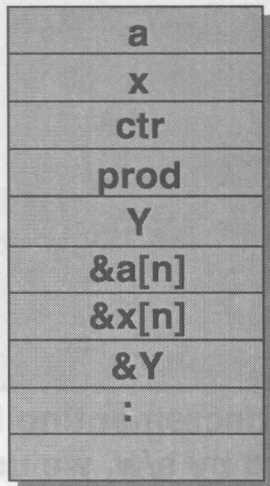
25

THE WORLD LEADER IN DSP SOLUTIONS



SOP Example: Loading values

Register File A

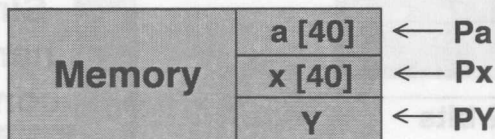


32 bits



How are a and x loaded?

- ◆ a, x, Y located in memory
- ◆ Create a pointer to values
 - Pa = &a
 - Px = &x
 - PY = &Y



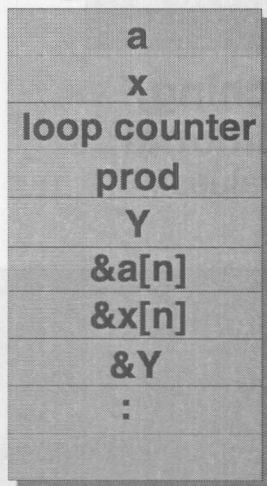
26

THE WORLD LEADER IN DSP SOLUTIONS

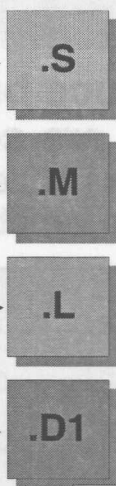
TEXAS
INSTRUMENTS

SOP Example: Loading values

Register File A



32 bits



Memory

$$Y = \sum_{n=1}^{40} a_n * x_n$$

MVK 40, ctr

loop:

LDH *Pa++, a

LDH *Px++, x

MPY a, x, prod

How do we increment through the array?

STH Y, *PY

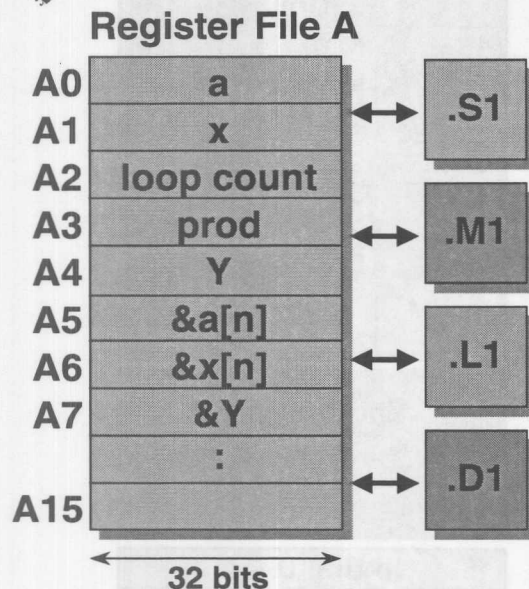
27

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



'C62x ASM: Sum of Products



$$Y = \sum_{n=1}^{40} a_n * x_n$$

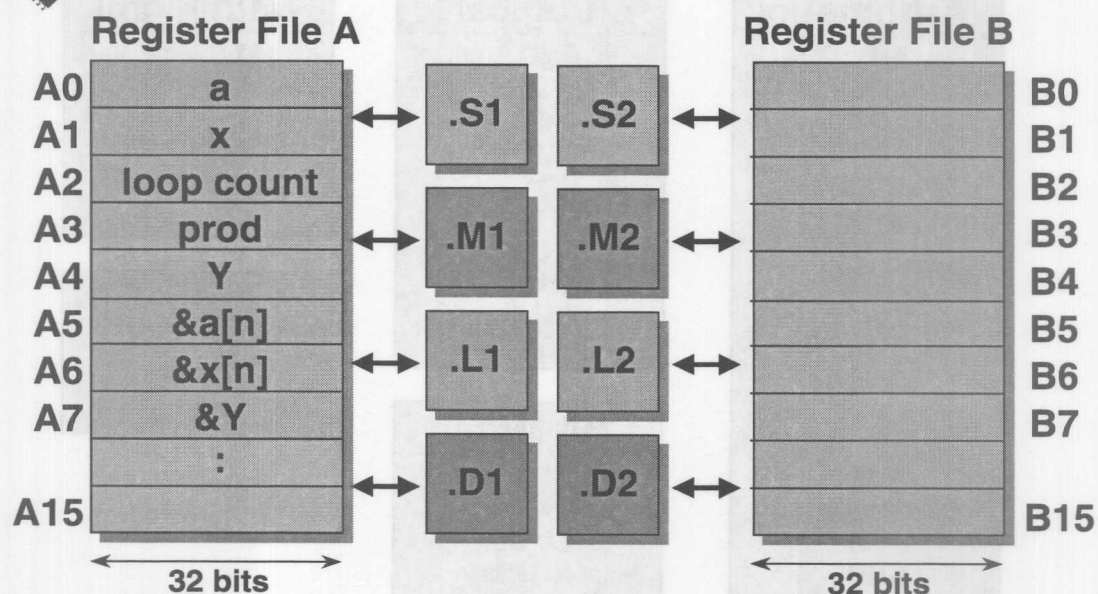
```
loop:  MVK    .S1    40, A2
       LDH    .D1    *A5++, A0
       LDH    .D1    *A6++, A1
       MPY    .M1    A0, A1, A3
       ADD    .L1    A4, A3, A4
       SUB    .S1    A2, 1, A2
       [A2] B    .S1    loop
       STH    .D1    A4, *A7
```

28

THE WORLD LEADER IN DSP SOLUTIONS



'C62x ASM: Dual paths



29

THE WORLD LEADER IN DSP SOLUTIONS





'C62x: RISC-like instruction set

.S Unit			.L Unit		
ADD	NEG		ABS	NOT	
ADDK	NOT		ADD	OR	
ADD2	OR		AND	SADD	
AND	SET		CMPEQ	SAT	
B	SHL		CMPGT	SSUB	
CLR	SHR		CMPLT	SUB	
EXT	SSHL		LMBD	SUBC	
MV	SUB		MV	XOR	
MVC	SUB2		NEG	ZERO	
MVK	XOR				
MVKH	ZERO				

.D Unit		
ADD	ST	
ADDA	SUB	
LD	SUBA	
MV	ZERO	
NEG		

.M Unit		
MPY	SMPY	
MPYH	SMPYH	

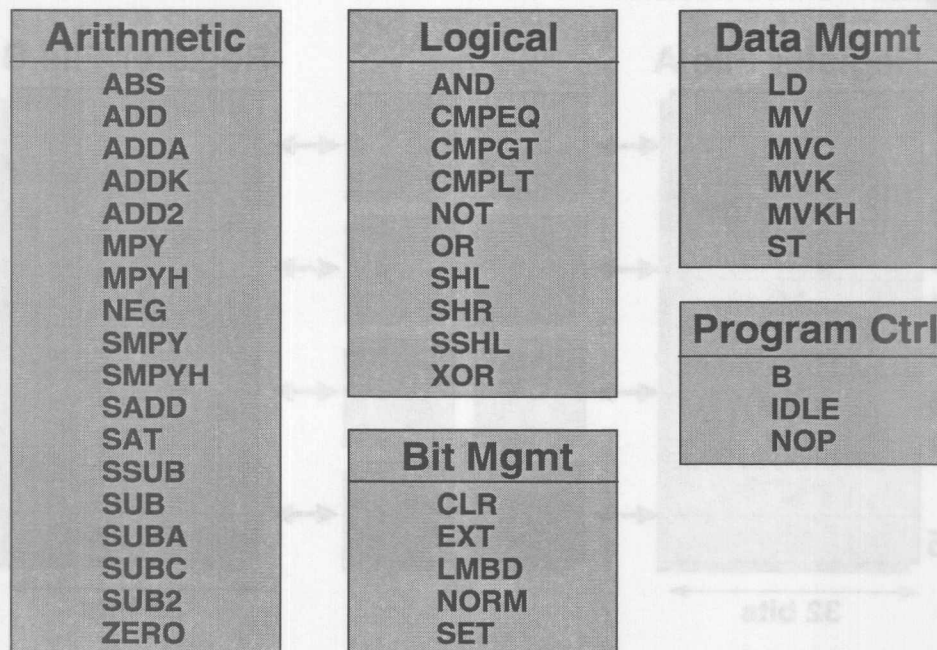
No Unit Used	
NOP	IDLE

30

THE WORLD LEADER IN DSP SOLUTIONS



'C62x Instruction Set (by category)





'C67x: Superset of fixed-point set

.S Unit			.L Unit		
ADD	NEG	ABSSP	ABS	NOT	ADDSP
ADDK	NOT	ABSDP	ADD	OR	ADDDP
ADD2	OR	CMPGTSP	AND	SADD	SUBSP
AND	SET	CMPEQSP	CMPEQ	SAT	SUBDP
B	SHL	CMPLTSP	CMPGT	SSUB	INTSP
CLR	SHR	CMPGTDP	CMPLT	SUB	INTDP
EXT	SSHL	CMPEQDP	LMBD	SUBC	SPINT
MV	SUB	CMPLTDP	MV	XOR	DPINT
MVC	SUB2	RCPSP	NEG	ZERO	SPRTUNC
MVK	XOR	RCPDP	NORM		DPTRUNC
MVKH	ZERO	RSQRSP			DPSP
		RSQRDP			
		SPDP			

.D Unit		
ADD	ST	
ADDA	SUB	
LD	SUBA	
MV	ZERO	
NEG		

.M Unit		
MPY	SMPY	MPYSP
MPYH	SMPYH	MPYDP
		MPYI
		MPYID

No Unit Used	
NOP	IDLE

31

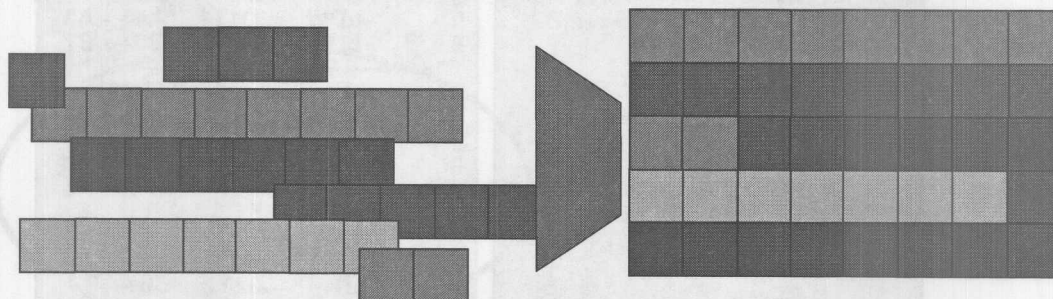
THE WORLD LEADER IN DSP SOLUTIONS



VelociTI: A true C engine

VelociTI is designed as an ideal target
for the 'C6000 C compiler,
enabling highly efficient
C code development...

... with the compiler handling scheduling for you



32

THE WORLD LEADER IN DSP SOLUTIONS





'C62x: Generic C code

Sum of Products

```
#define N      40

short  a[N] = {0x0001, 0x0002, 0x0003, 0x0004, ... };
short  x[N] = {0x0005, 0x0006, 0x0007, 0x0008, ... };

int sumprod(void) {
    char    i;
    int     sum=0;

    for(i=0; i<N; i++) {
        sum += a[i] * x[i];
    }

    return(sum);
}
```

33

THE WORLD LEADER IN DSP SOLUTIONS



Optimized output = 2 taps per cycle

Two Sums of Product per iteration

<pre>L2: ; PIPED LOOP PROLOG LDW .D1T1 *A4++,A3 LDW .D2T2 *B6++,B7 LDW .D1T1 *A4++,A3 LDW .D2T2 *B6++,B7 [B0] B .S1 L3 LDW .D1T1 *A4++,A3 LDW .D2T2 *B6++,B7 [B0] B .S1 L3 LDW .D1T1 *A4++,A3 LDW .D2T2 *B6++,B7 [B0] B .S1 L3 LDW .D1T1 *A4++,A3 LDW .D2T2 *B6++,B7</pre>	<pre>MPY .M2X B7,A3,B4 MPYH .M1X B7,A3,A5 [B0] B .S1 L3 LDW .D1T1 *A4++,A3 LDW .D2T2 *B6++,B7 MPY .M2X B7,A3,B4 MPYH .M1X B7,A3,A5 [B0] B .S1 L3 LDW .D1T1 *A4++,A3 LDW .D2T2 *B6++,B7 *** L3: ; PIPED LOOP KERNEL ADD .L2 B4,B5,B5 ADD .L1 A5,A0,A0 MPY .M2X B7,A3,B4 MPYH .M1X B7,A3,A5 [B0] B .S1 L3 [B0] SUB .S2 B0,1,B0 LDW .D1T1 *A4++,A3 LDW .D2T2 *B6++,B7 ***</pre>
--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------	--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------

34

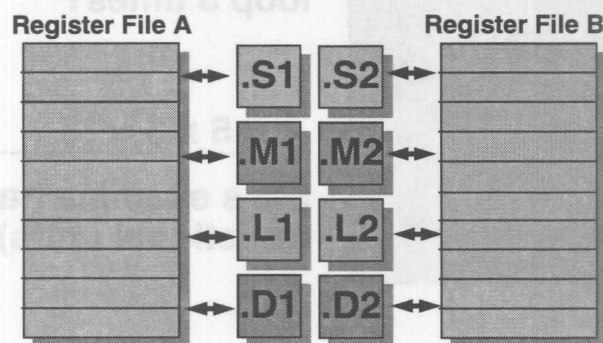
THE WORLD LEADER IN DSP SOLUTIONS



How can we get 40 taps in 28 cycles?

Key #1: Dual paths create two results per loop.

We split the problem in half, and worked on the halves simultaneously... doing intermediate calculations two at a time.



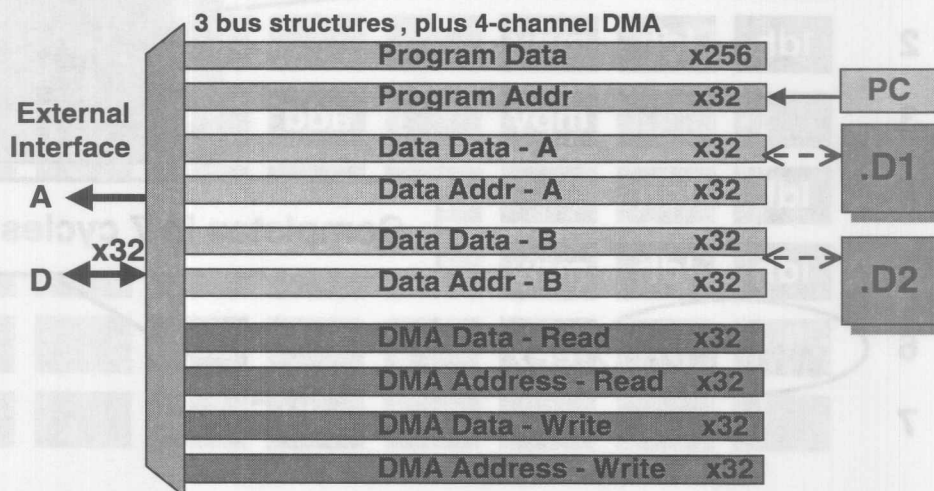
35

THE WORLD LEADER IN DSP SOLUTIONS



Busses: Supporting 5-ns clock rate

Key #2: Multiple busses allow dual data access and program fetch simultaneously.



36

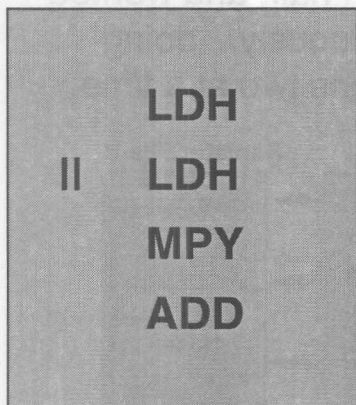
THE WORLD LEADER IN DSP SOLUTIONS





Concept: Software pipelining

Key #3: Software pipelining enables efficiency.



How many cycles would it take to perform this loop 5 times?

$$5 \times 3 = 15 \text{ cycles}$$

Let's examine hardware (functional units) usage ...

37



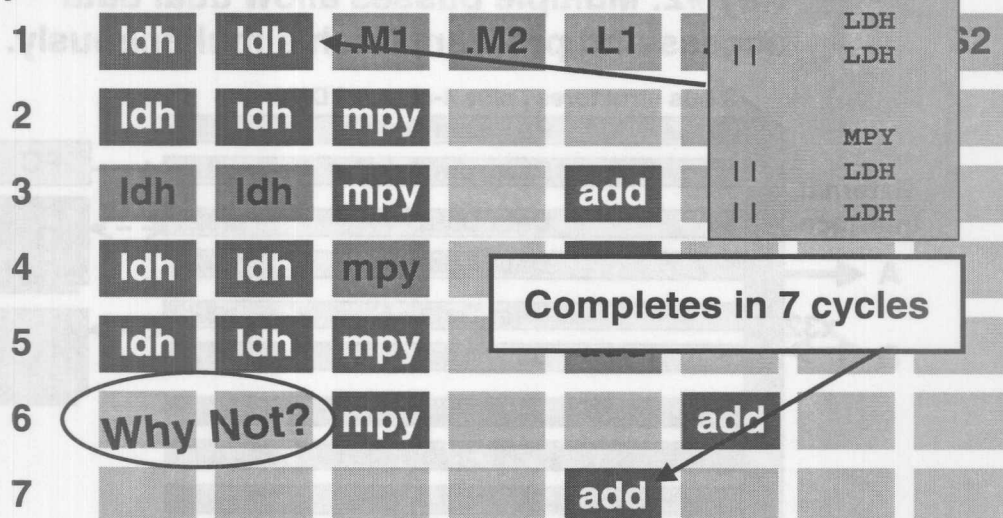
THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



Software Pipelining: 1/2 the cycles

Cycle



38



THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



Results: 2x taps; half the cycles

#1 -- Dual paths enable 2 taps per cycle

```

L2:  ; PIPED LOOP PROLOG
      LDW  .D1T1  *A4++,A3
      ||   LDW  .D2T2  *B6++,B7

      LDW  .D1T1  *A4++,A3
      ||   LDW  .D2T2  *B6++,B7

      [ B0] B      .S1    L3
      ||   LDW  .D1T1  *A4++,A3
      ||   LDW  .D2T2  *B6++,B7

      [ B0] B      .S1    L3
      ||   LDW  .D1T1  *A4++,A3
      ||   LDW  .D2T2  *B6++,B7

      [ B0] B      .S1    L3
      ||   LDW  .D1T1  *A4++,A3
      ||   LDW  .D2T2  *B6++,B7

      MPY  .M2X    B7,A3,B4
      ||   MPYH .M1X    B7,A3,A5
      || [ B0] B      .S1    L3
      ||   LDW  .D1T1  *A4++,A3
      ||   LDW  .D2T2  *B6++,B7

      MPY  .M2X    B7,A3,B4
      ||   MPYH .M1X    B7,A3,A5
      || [ B0] B      .S1    L3
      ||   LDW  .D1T1  *A4++,A3
      ||   LDW  .D2T2  *B6++,B7
      **-----*
L3:  ; PIPED LOOP KERNEL
      ADD  .L2     B4,B5,B5
      ||   ADD  .L1     A5,A0,A0
      ||   MPY  .M2X    B7,A3,B4
      ||   MPYH .M1X    B7,A3,A5
      || [ B0] B      .S1    L3
      || [ B0] SUB  .S2     B0,1,B0
      ||   LDW  .D1T1  *A4++,A3
      ||   LDW  .D2T2  *B6++,B7
      **-----*
  
```

39

THE WORLD LEADER IN DSP SOLUTIONS



Results: 2x taps; half the cycles

#2 -- Busses enable multiple data loads

```

L2:  ; PIPED LOOP PROLOG
      LDW  .D1T1  *A4++,A3
      ||   LDW  .D2T2  *B6++,B7

      LDW  .D1T1  *A4++,A3
      ||   LDW  .D2T2  *B6++,B7

      [ B0] B      .S1    L3
      ||   LDW  .D1T1  *A4++,A3
      ||   LDW  .D2T2  *B6++,B7

      [ B0] B      .S1    L3
      ||   LDW  .D1T1  *A4++,A3
      ||   LDW  .D2T2  *B6++,B7

      [ B0] B      .S1    L3
      ||   LDW  .D1T1  *A4++,A3
      ||   LDW  .D2T2  *B6++,B7

      MPY  .M2X    B7,A3,B4
      ||   MPYH .M1X    B7,A3,A5
      || [ B0] B      .S1    L3
      ||   LDW  .D1T1  *A4++,A3
      ||   LDW  .D2T2  *B6++,B7

      MPY  .M2X    B7,A3,B4
      ||   MPYH .M1X    B7,A3,A5
      || [ B0] B      .S1    L3
      ||   LDW  .D1T1  *A4++,A3
      ||   LDW  .D2T2  *B6++,B7
      **-----*
L3:  ; PIPED LOOP KERNEL
      ADD  .L2     B4,B5,B5
      ||   ADD  .L1     A5,A0,A0
      ||   MPY  .M2X    B7,A3,B4
      ||   MPYH .M1X    B7,A3,A5
      || [ B0] B      .S1    L3
      || [ B0] SUB  .S2     B0,1,B0
      ||   LDW  .D1T1  *A4++,A3
      ||   LDW  .D2T2  *B6++,B7
      **-----*
  
```

40

THE WORLD LEADER IN DSP SOLUTIONS





```
L2:      ; PIPED LOOP PROLOG
```

	MPY	.M2X	B7,A3,B4
	MPYH	.M1X	B7,A3,A5
[B0]	B	.S1	L3
	LDW	.D1T1	*A4++,A3
	LDW	.D2T2	*B6++,B7

	MPY	.M2X	B7,A3,B4
	MPYH	.M1X	B7,A3,A5
[B0]	B	.S1	L3
	LDW	.D1T1	*A4++,A3
	LDW	.D2T2	*B6++,B7

```

L8:      ; PIPED LOOP KERNEL
      ADD    .L2      B4,B5,B5
      ADD    .L1      A5,A0,A0
      MPY    .M2X      B7,A3,B4
      MPYH   .M1X      B7,A3,A5
      [ B0]  B         .S1      L3
      [ B0]  SUB       .S2      B0,1,B0
      LDW    .D1T1     *A4++,A3
      LDW    .D2T2     *B6++,B7

```

41



TEXAS
INSTRUMENTS



- 42



TEXAS
INSTRUMENTS

4Q98



How do I work with TI's 'C6000?

What performance can I expect?

How do I get my performance?

How do I interface easily?

What are the new 'C6000 devices?

What is my power consumption?

How does TI enable maximum performance at lower cost?

43

THE WORLD LEADER IN DSP SOLUTIONS



'C6000: Interfacing

Varied sources for flexible interfacing:

- ✓ Internal Memory
- ✓ External Memory Interface (EMIF)
- ✓ Host Port Interface (HPI)
- ✓ New Expansion Port
- ✓ Multi-channel Buffered Serial Port (McBSP)
- ✓ Direct Memory Access (DMA)

44

THE WORLD LEADER IN DSP SOLUTIONS





Internal Memory: Feeding the CPU

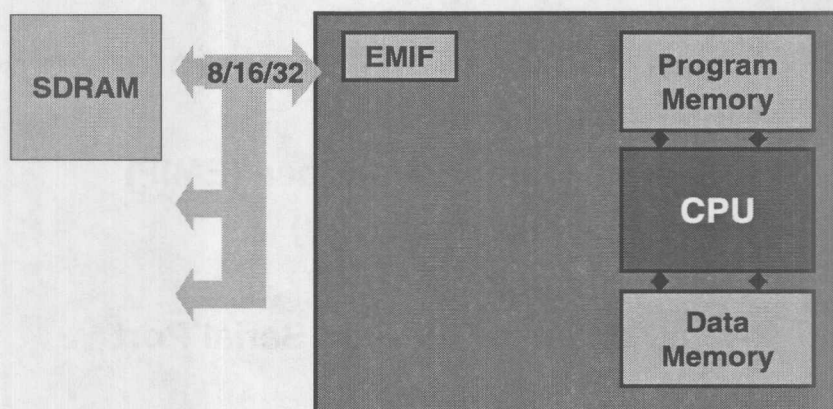
	L1 Memory		L2 Memory
	Program Memory	Data Memory	
'C6201	64KB 1 blk Pgm/Cache	64KB 2 blks 4 banks ea	External
'C6701	64KB 1 blk Pgm/Cache	64KB 2 blks 8 banks ea	External
'C6202	256KB 1 blk Pgm/Cache 1 blk Mapped Pgm	128 KB 2 blks 4 banks ea	External
'C6211	4 KB 1 blk Cache	4 KB 1 blk Cache	64 KB 4 blk Mapped Cache

45

THE WORLD LEADER IN DSP SOLUTIONS



Interfacing: External memory I/F



SDRAM

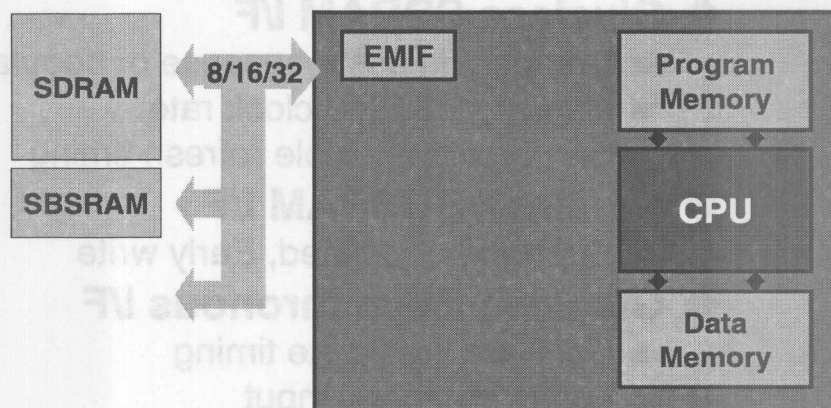
Provides lowest cost/bit and operates up to 125MHz

46

THE WORLD LEADER IN DSP SOLUTIONS



Interfacing: External memory I/F



SBSRAM

I/F allows higher sustained throughput with no refresh/page penalty

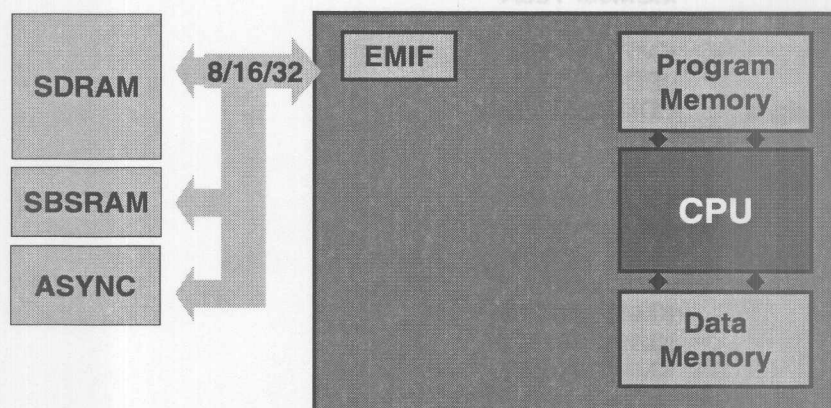
47



THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

Interfacing: External memory I/F



ASYNC

Provides I/F to ROMs, asynchronous RAMs and other parallel peripherals

48



THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



EMIF: Glueless I/F

◆ Glueless SDRAM I/F

- Decreasing costs because of popularity
- Runs at 1/2 CPU clock rate
- Can provide flexible refresh timing

◆ Glueless SBSRAM I/F

- Supports: Pipelined, Early write

◆ Glueless Asynchronous I/F

- Software wait state timing
- Hardware ready input
- Non-pipelined access
- Interface with Asynchronous RAMs, ROMs, FLASH, FIFOs

49

THE WORLD LEADER IN DSP SOLUTIONS



Synchronous Memory Compatible Devices

SBSRAM:

Micron	MT58LC128K32D8
Galvantech	GVT71128G36
Motorola	MCM63P733A
Motorola	MCM69P737
Samsung	KM736V789/L
NEC	uPD4311632L
Electronic Designs	EDI2DL32256V

SDRAM:

Micron	TMS626812B
Hitachi	HM5216165
Hitachi	HM5216805
Hitachi	HM5264165
Samsung	KM416S1020C
Samsung	KM48S2020C
Samsung	KM416S4030B

Note: Other devices are usable as long as functionality is equivalent to the devices listed above and the timing requirements of the 'C6000 are met with the desired timing margin.

EMIF: Glueless Asynchronous I/F

Asynchronous memory is the most traditional memory type. The asynchronous interface provides a flexible, glueless interface to many different devices. Since it is asynchronous, this interface can be much slower than one of the synchronous options.

- Software wait state timing
 - Selectable for each Async memory region
 - Separate for Read and Write accesses
 - Parameters programmable in clock cycles (Setup time, strobe width, hold time)
- Hardware ready input
- Non-pipelined access
- Interfaces with
 - Asynchronous RAMs
 - ROMs (32-, 16-, 8-bit)
 - Flash (Read & Write)
 - FIFOs (Strobed, clocked, synchronous, asynchronous)

EMIF: Glueless SBSRAM I/F

SBSRAM is very similar to SRAM, but it is clocked, thus allowing the fastest memory connection available on the 'C6000. This interface uses pipelined accesses to achieve this high-level performance.

- Glueless interface
- Supports: Pipelined, Early write

EMIF: Glueless SDRAM I/F

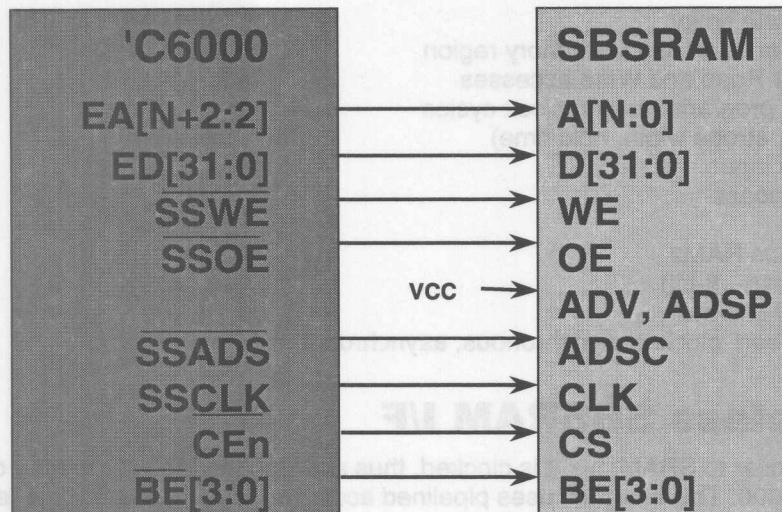
SDRAM provides high-performance and low cost per-bit. It is the primary memory interface in many 'C6000 systems because it balances cost vs. performance tradeoffs well.

- Glueless interface
- Decreasing costs because of popularity in the PC market
- Runs at 1/2 CPU clock rate
- 'C6000 can provide flexible refresh timing

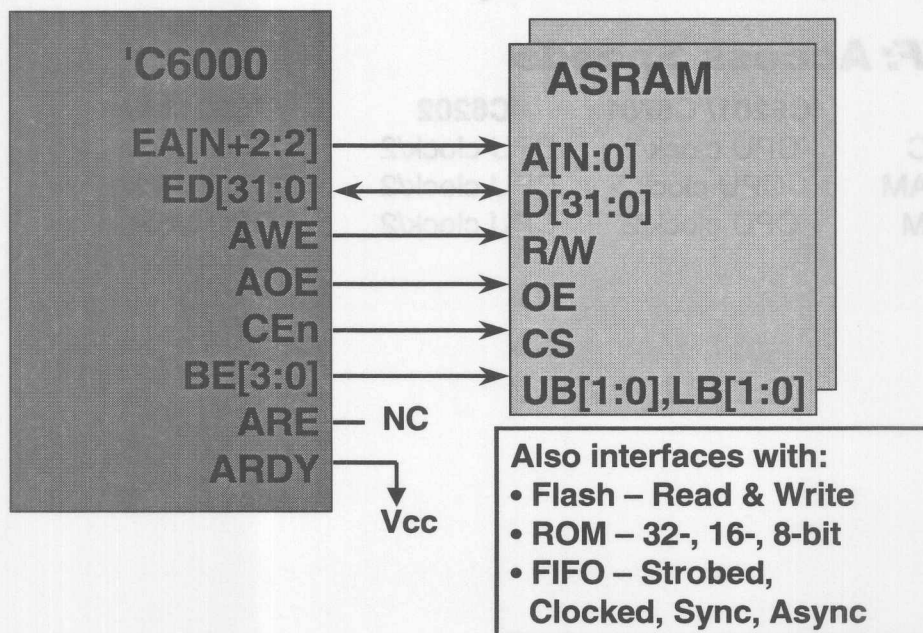
EMIF: Access Speeds

	'C6201/'C6701	'C6202	'C6211
ASYNCR	CPU clock/2	CPU clock/2	≤CPU clock
SBSRAM	CPU clock	CPU clock/2	≤CPU clock
SDRAM	CPU clock/2	CPU clock/2	≤CPU clock

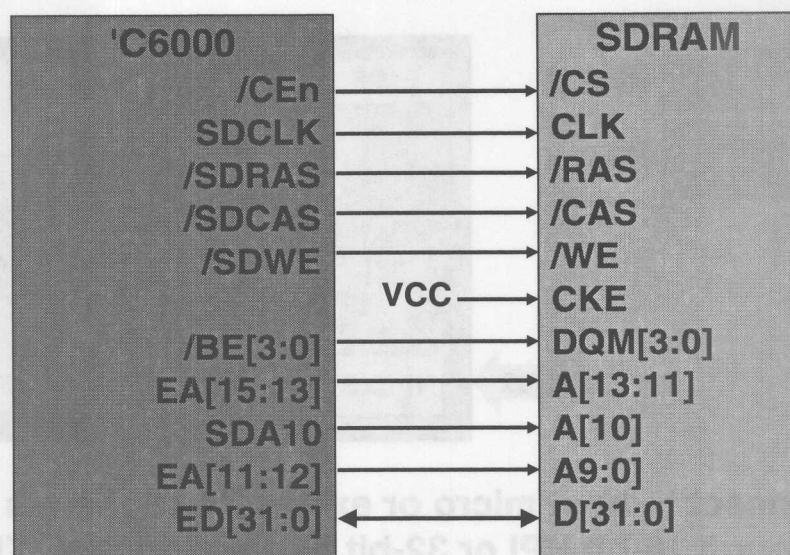
EMIF: SBSRAM interface ...



EMIF: ASRAM interface



EMIF: SDRAM interface



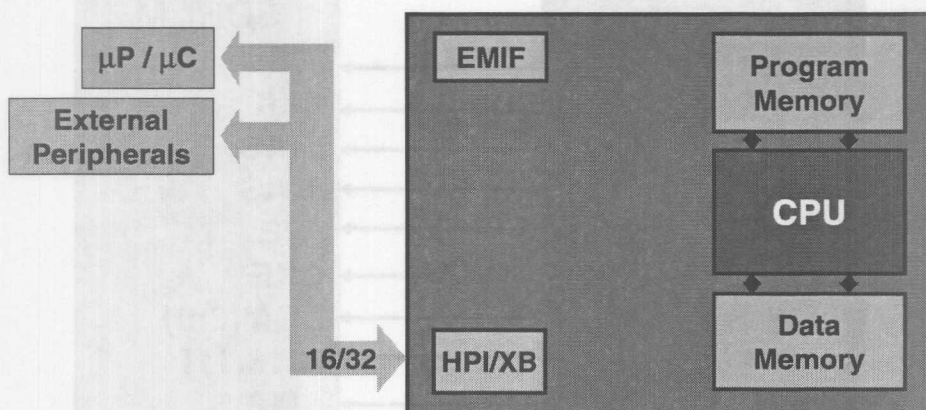
Provides an additional 16-bit wide asynchronous port allowing a host processor FULL access to the 'C6000 memory map (internal, external and peripherals).

Not a glue IC to standard general-purpose processors:

- Motorola 68020, 68360, PowerPC 601
- Intel 486
- IBM PowerPC
- Slave mode interface to host, PCI, etc.
- Can initialize (boot-strap) CPU through HPI. This is very cost-effective for systems with host processors or when interfaced through PCI interface.
- Support of multiplexed address/data (Intel)



Interfacing: HPI and Expansion Bus



Connect to host micro or external peripherals through 16-bit HPI or 32-bit Expansion Bus (XB)

50



THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

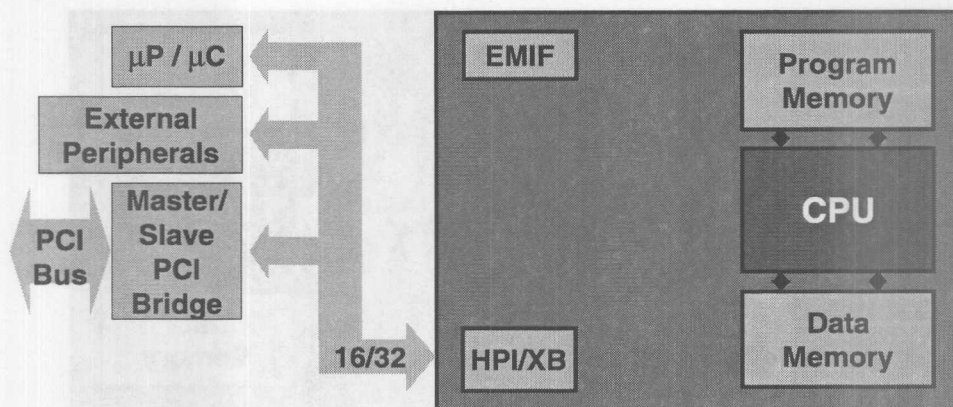
HPI

Provides an additional 16-bit wide asynchronous port allowing a host processor FULL access to the 'C6000 memory map (internal, external and peripherals).

- No/Low-glue I/F to standard general-purpose processors:
 - Motorola 68302, 68360, Power PC 860
 - Intel i960
 - IBM Power PC
- Slave mode interface to host, PCI, etc.
- Can initialize (boot-strap) CPU through HPI. This is very cost-effective for systems with host processors or when interfaced through PCI interface.
- Support of multiplexed address data hosts (Intel).



Interfacing: HPI and Expansion Bus



HPI provides convenient PCI slave connection while XB provides 32-bit, low-glue Master/Slave connection

51



THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

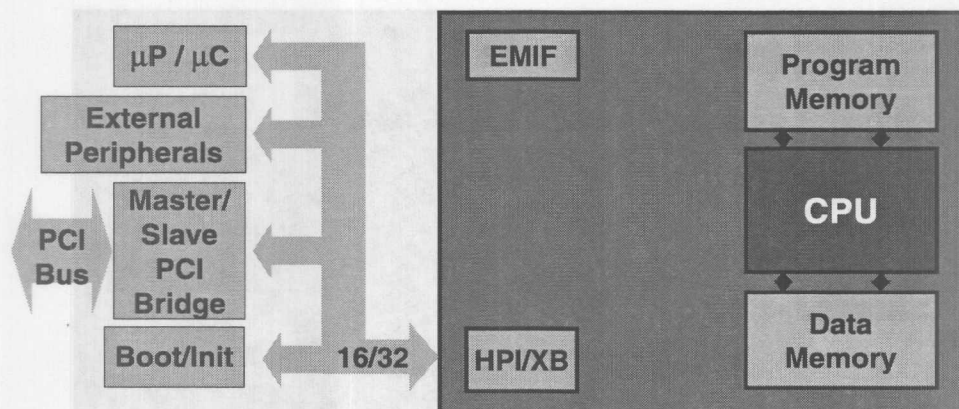
Expansion Bus

The expansion bus is a 32-bit wide bus that supports interfaces to a variety of asynchronous peripherals, asynchronous or synchronous FIFOs, PCI bridge chips, and other external masters. Basically, the Expansion Bus provides all the features of the HPI plus the following:

- Replaces 16-bit HPI with 32-bit bus
- Two major sub blocks—the I/O port and Host Port Interface, which can coexist in the same system.
 - The I/O port has two modes: Async memory and FIFO
 - Both can coexist in a single system
 - Async timings are programmable
 - FIFO provides glueless interface
 - Host Port Interface can operate in one of two modes: asynchronous (same as HPI) and synchronous.
 - Master/Slave PCI Bridge Interface (without FPGA support)
 - Fast support of industry-standard RISC hosts (through synchronous local bus)
 - Sustained 133–266 Mbytes/sec throughput (4–8x improvement over 'C6201 HPI)
- Second 32-bit bus allows DMA access to host/peripherals/etc. while CPU accesses memory via EMIF. Big increase in device bandwidth.



Interfacing: HPI and Expansion Bus



HPI/XB allows simple processor initialization (boot-up)

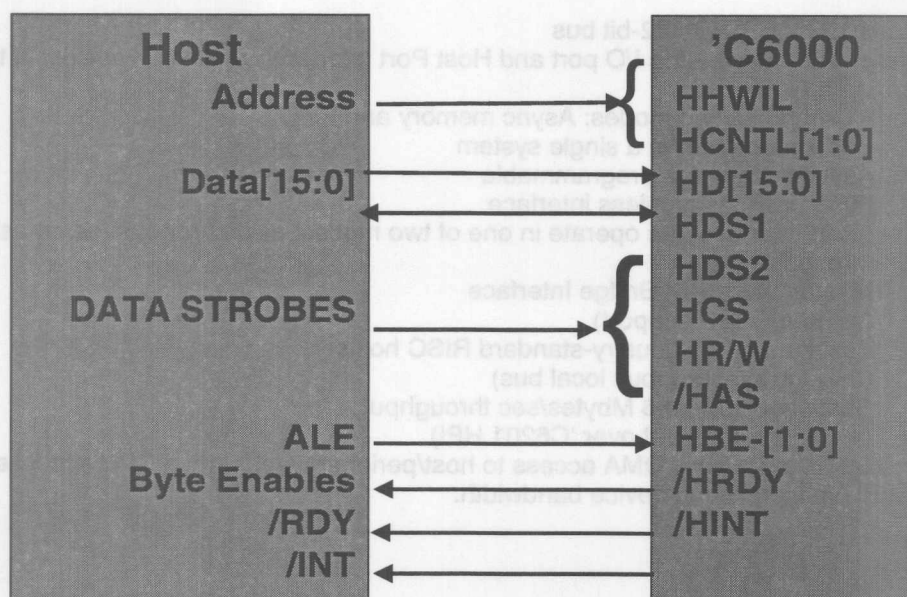
52



THE WORLD LEADER IN DSP SOLUTIONS

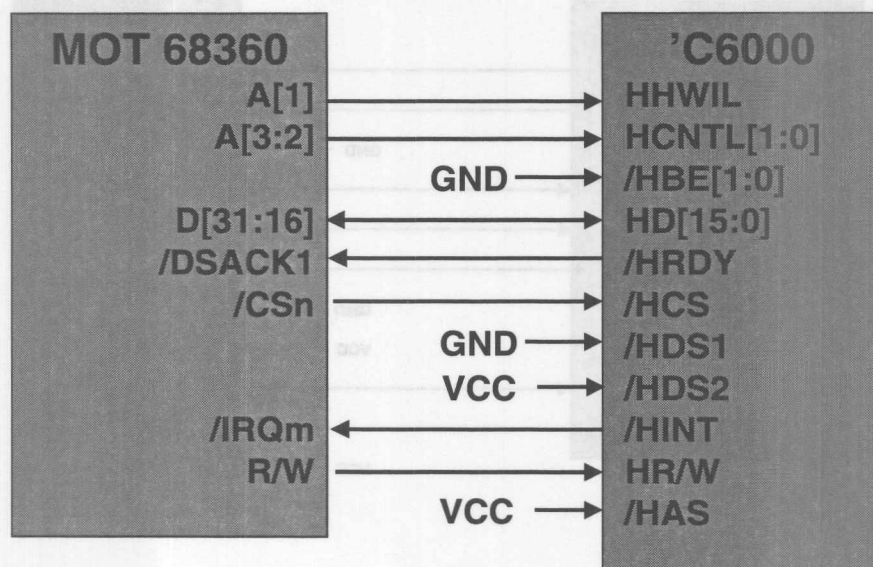
TEXAS
INSTRUMENTS

HPI: Typical connection





HPI: MOT 68360-to-'C6000

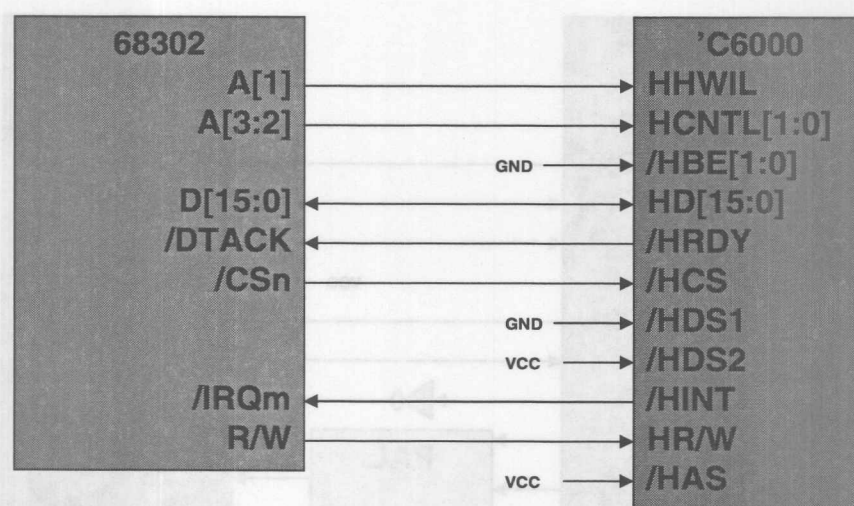


53

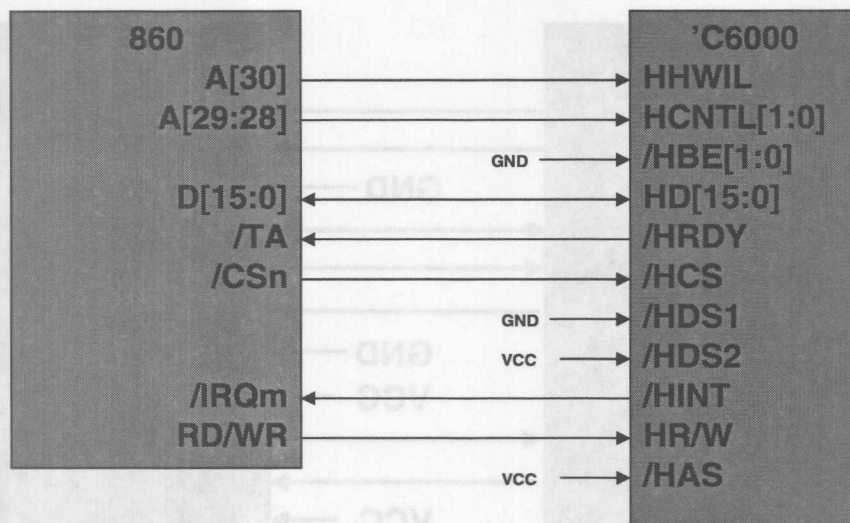
THE WORLD LEADER IN DSP SOLUTIONS



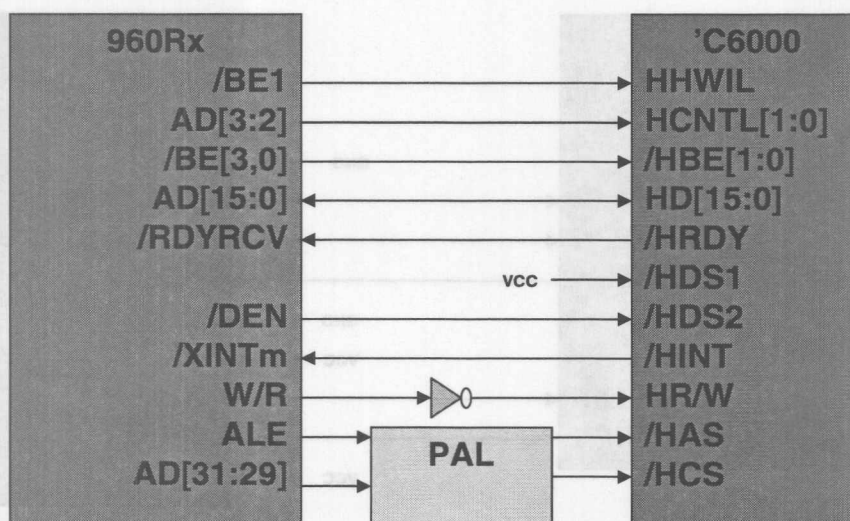
HPI: MOT 68302-to-'C6000



HPI: MOT Power PC 860-to-'C6000



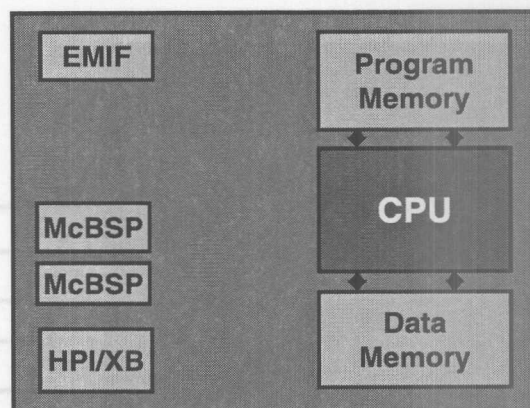
HPI: Intel i960Rx-to-'C6000





Interfacing: Multi-channel BSP

- Full duplex
- Runs at up to 1/2 CPU clock rate
- Double-buffered transmit, triple-buffered receive
- u-Law, A-Law companding
- Support for 128 time slots
- Compliant with variety of standards



54

THE WORLD LEADER IN DSP SOLUTIONS



Interfacing: Multi-channel BSP

We support:

- ST-BUS
- T1/E1 Framing Chips
- IOM2
- SPI (4 different polarity bit-delay options)
- IIS
- AC97
- Industry-standard Codecs
- MVIP
- H.100
- Analog Interface Chips: TI TLC320

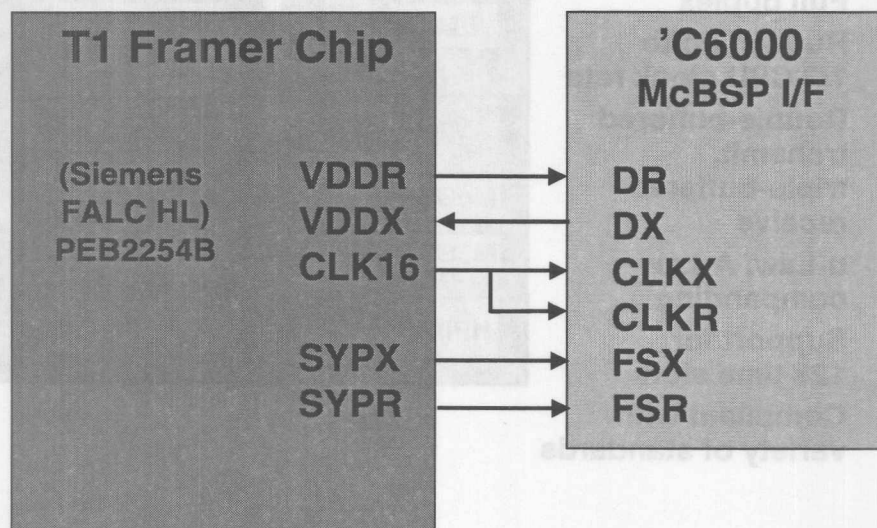
55

THE WORLD LEADER IN DSP SOLUTIONS





McBSP: Glueless I/F



56

THE WORLD LEADER IN DSP SOLUTIONS



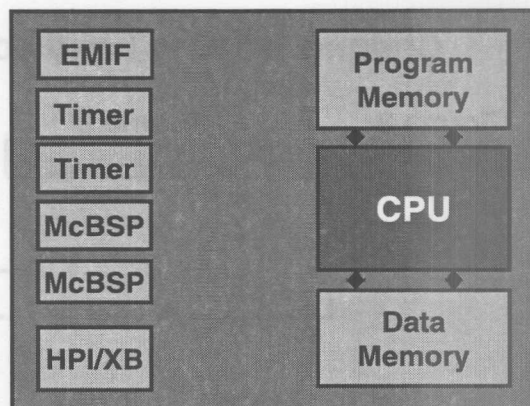
'C6000 McBSP: Framing chips

- ST Bus
 - MVIP framers: Mitel 90810
 - Mitel T1/E1 framers
 - SCSA framers: VLSI SC2000 & SC4000
 - Future H.100 framing chips
- Other Framing Chips
 - Brooktree (T1 & E1) BT8370
 - Dallas Semiconductor DS 2151/2 (T1) 2153/4 (E1)
 - PMC Sierra PM4341/44 (T1/Quad TI) PM6341/44 (E1/Quad E1)
 - Siemens PEB 2254/5 (T1 & E1)



Timers: General purpose

- 32-bit timers:
 - Time events
 - Count events
 - Generate pulses
 - Interrupt the CPU and send synchronization events to the DMA



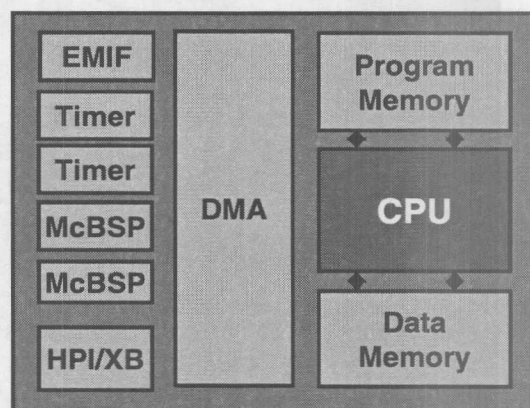
57

THE WORLD LEADER IN DSP SOLUTIONS



DMA: Transfers transparent to CPU

- DMA can access all components for transfers
- DMA transfers are transparent to the CPU



58

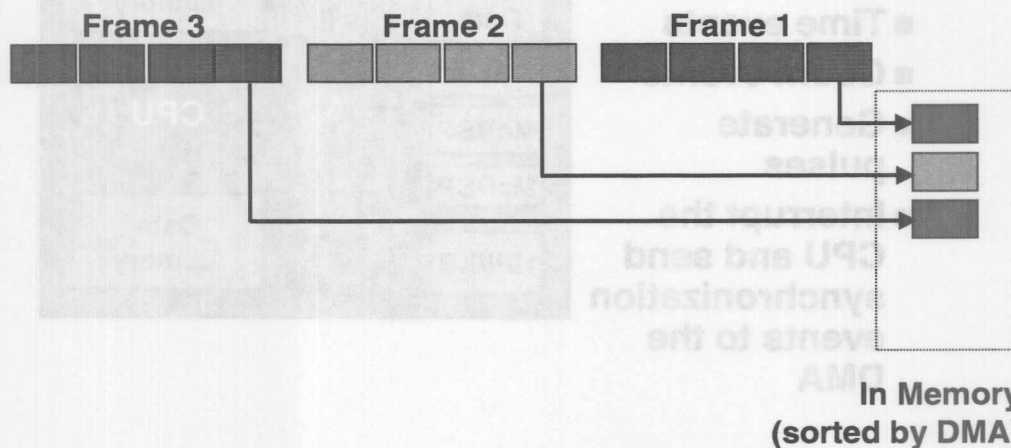
THE WORLD LEADER IN DSP SOLUTIONS





DMA: Flexible addressing

Channel sorting handled by 'C6000 DMA



59

THE WORLD LEADER IN DSP SOLUTIONS



EDMA: Enhanced DMA

	DMA	EDMA
Channels	4 channels + 1 dedicated to HPI	16 channels
Auto-Init	~2 tasks	69 tasks
Priority	4 fixed levels	2 variable levels

60

THE WORLD LEADER IN DSP SOLUTIONS



For a list of related application reports, white papers, and Designer Notebook Pages, see the Appendix.



How do I work with TI's 'C6000?

What performance can I expect?

How do I get my performance?

How do I interface easily?

What are the new 'C6000 devices?

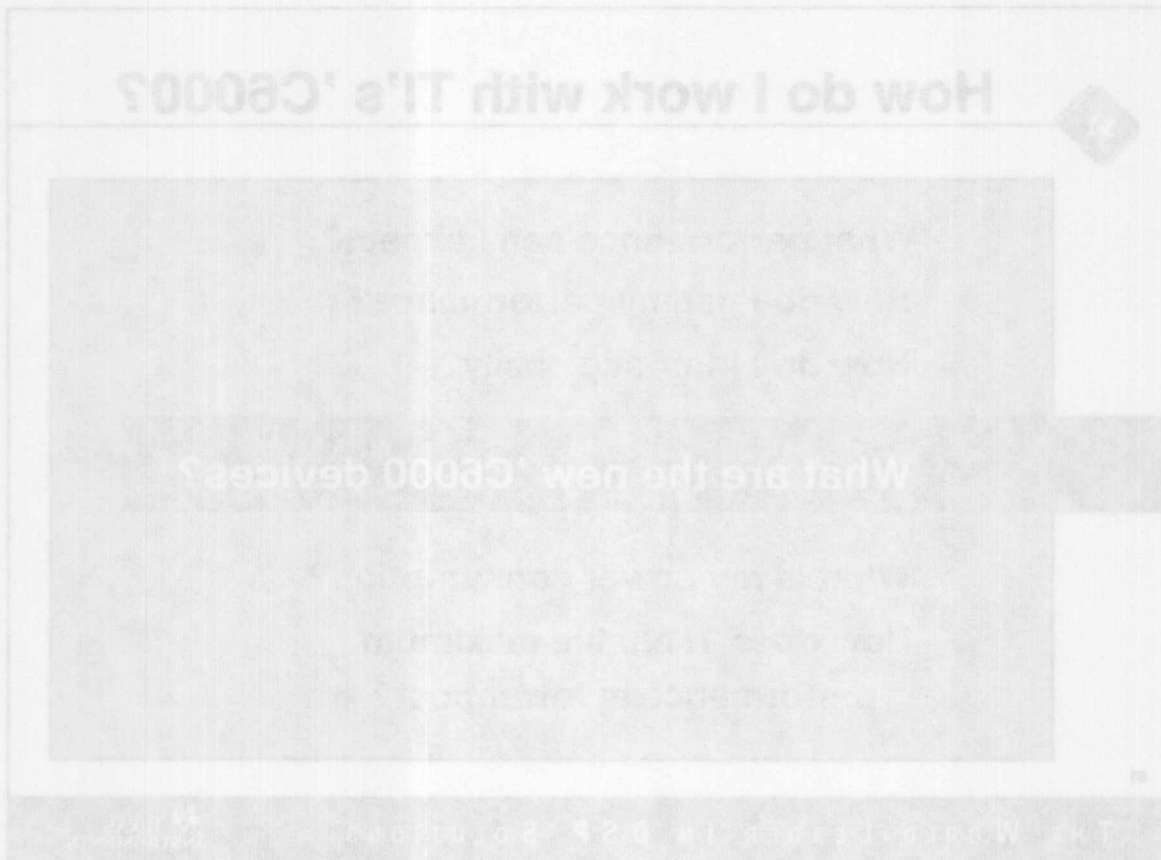
What is my power consumption?

How does TI enable maximum
performance at lower cost?

61

THE WORLD LEADER IN DSP SOLUTIONS

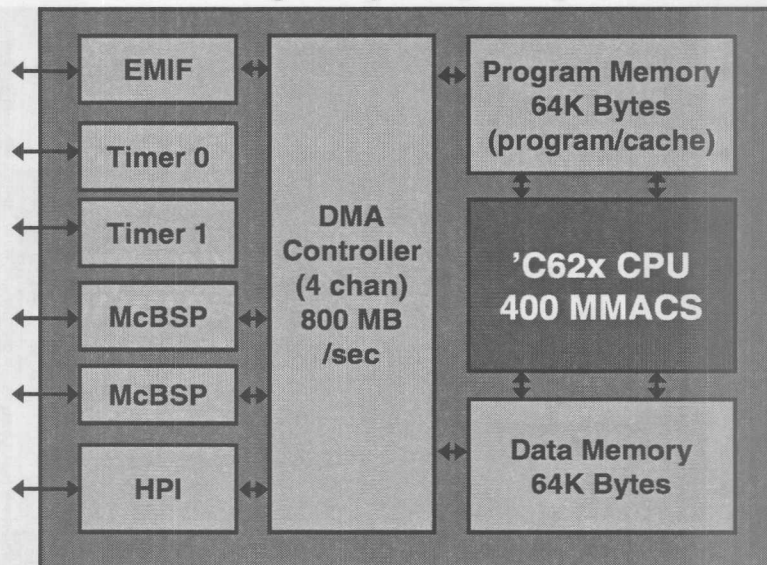






'C6201: 1600 MIPS in production

TMS320C6201B Digital Signal Processor: 200 MHz at .18 μ



62



THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

TMS320C6201

- 1.9-watt typical internal active power

'C6201 Rev 3:

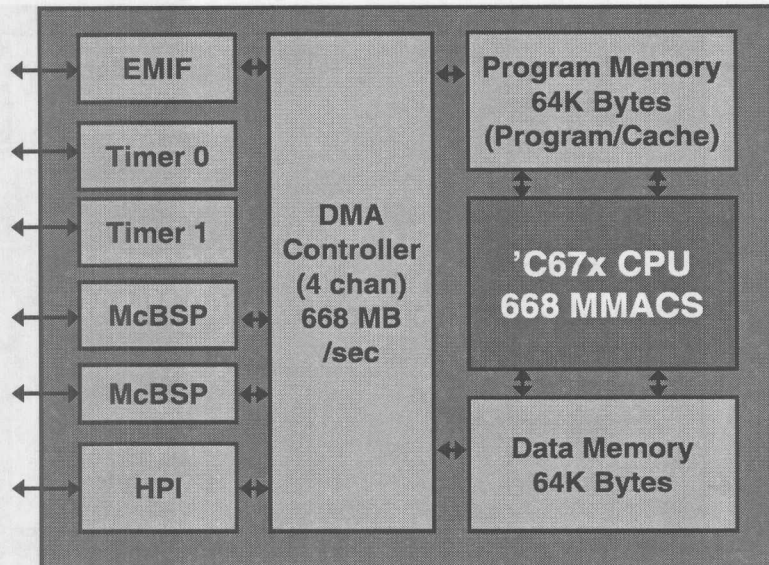
- Production 1Q99*
- Sampling now
- Two package options:
 - Both 352-pin BGA
 - 35 mm
 - 27 mm (begins sampling 10/98*)

* Planned availability



'C6701: Floating point sampling now

TMS320C6701 Digital Signal Processor: 1 GFLOPS; 167 MHz at .18 μ



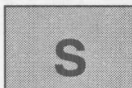
63

THE WORLD LEADER IN DSP SOLUTIONS



'C6000: Shared core

Shifter Unit



'C62x Fixed Point

32-bit ALU
shifts
bit field operations
branches

'C67x Floating Point

float comparison
float ABS
reciprocal
sq. root reciprocal
sngl/dbl prec. conv.

Multiply Unit



16x16 integer
multiply

32x32 integer/floating mpy
64 x64 integer/floating mpy

Logic Unit



40-bit ALU
integer comparison
normalization
leftmost bit detect

fix/float conversion
float arithmetic

Load (Data) Unit



loads and stores
32-bit add/sub
address calculations

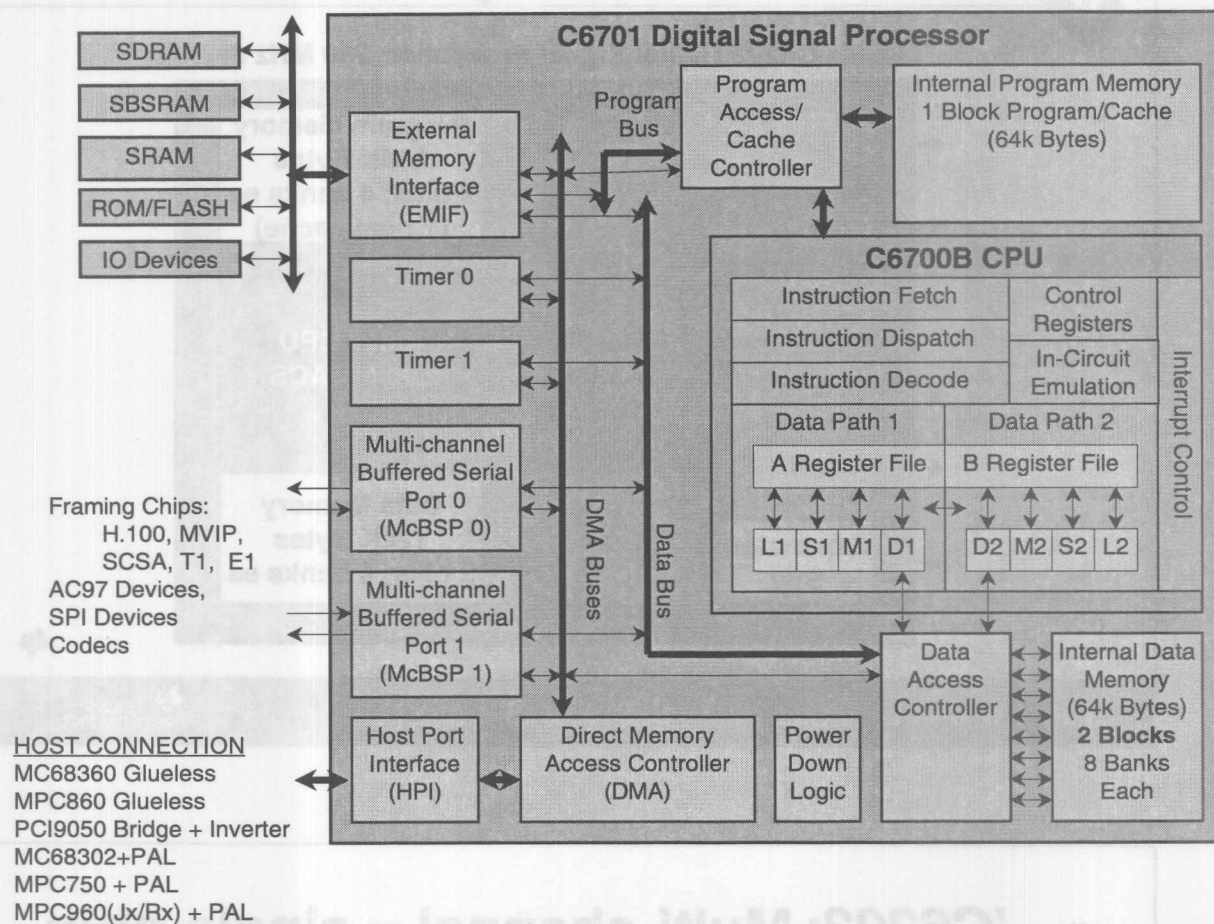
doubleword loads

64

THE WORLD LEADER IN DSP SOLUTIONS



TMS320C6701 Detailed Block Diagram



TMS320C6701

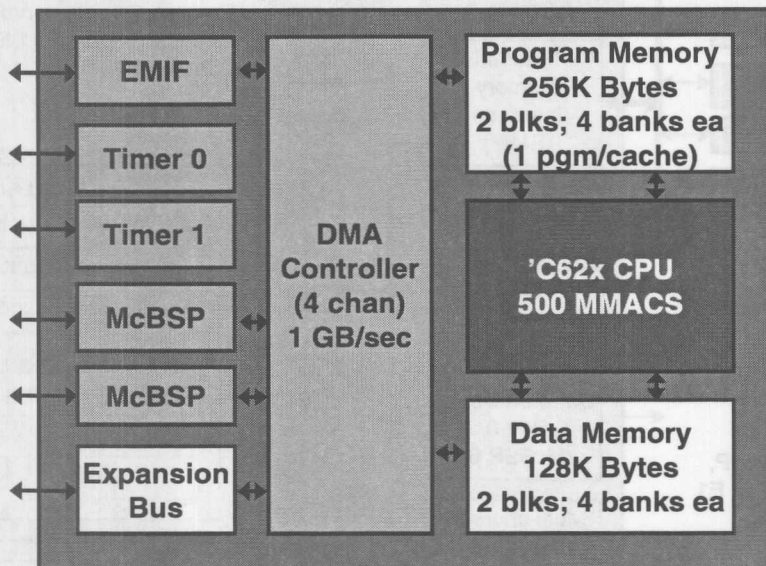
- 1.9-watt typical internal active power
- Assembly-source-code compatible with 'C62x
- Pin-compatible with 'C6201 (35-mm pkg.)
- Silicon available now
- EVM available 11/98*

* Planned availability



'C6202: 2000 MIPS just announced

TMS320C6202 Digital Signal Processor: 250 MHz at .18 μ



65

THE WORLD LEADER IN DSP SOLUTIONS



'C6202: Multi-channel = single-chip

Three vocoders + LEC + DTMF = One chip solution

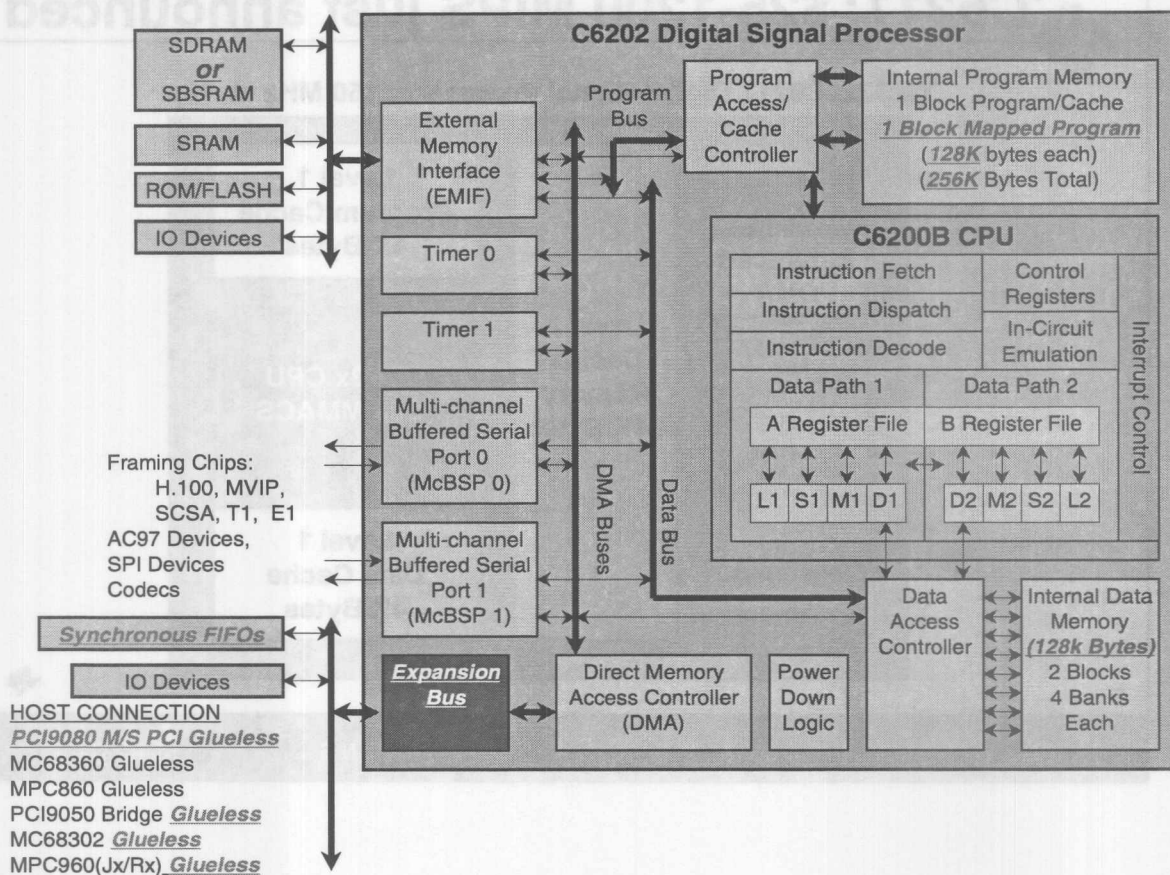
Algorithm	Program Memory (Kbytes)	24-Channel Data Memory (Kbytes)
G.723	104	63.5
G.729A	90	69.5
G.726	4.8	5.6
32ms LEC	4.4	24.6
DTMF	5	10.8

66

THE WORLD LEADER IN DSP SOLUTIONS



TMS320C6202 Detailed Block Diagram



TMS320C6202

- <2-watt typical internal active power

384K on-chip memory:

- Dual blocks allow concurrent DMA and CPU access without cycle stealing

Expansion bus = 'C6201 HPI, plus:

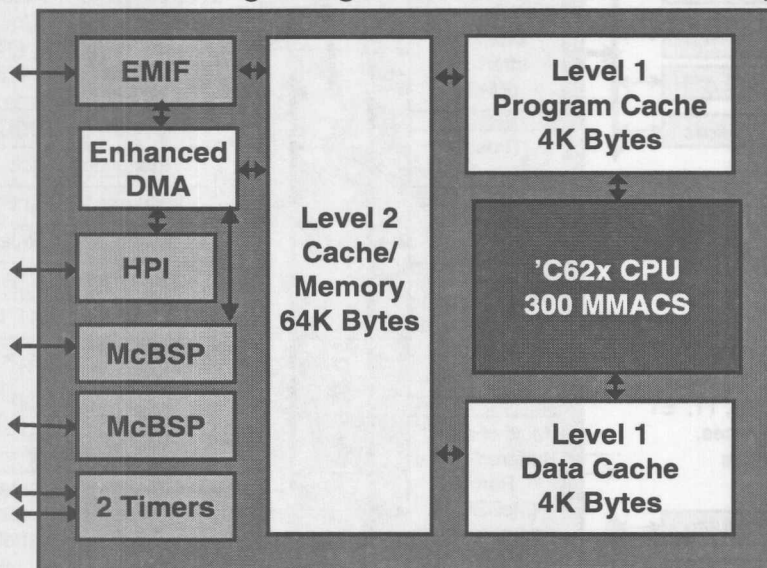
- Support for synchronous FIFO
- Low-glue I/F to PCI and bridge chips

'C6202 enables maximum density

- 27-mm 352 BGA
- Large on-chip memories
- Double MIPS/mm vs. 'C6201 (35 mm)

'C6211: \$25-1200 MIPS just announced

TMS320C6211 Digital Signal Processor: 150 MHz at .18μ

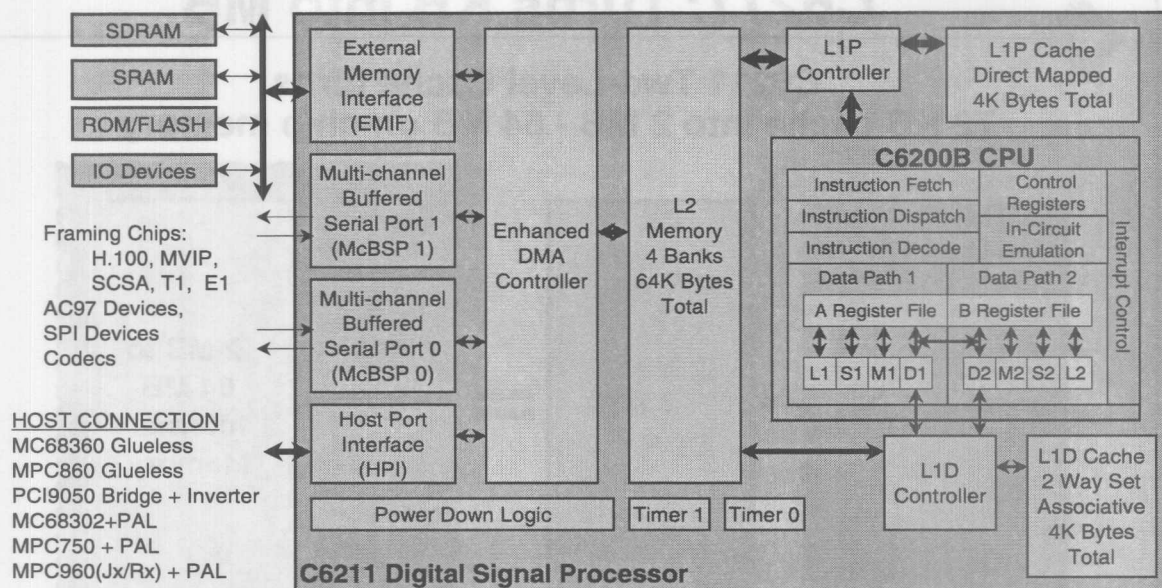


67

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

TMS320C6211 Detailed Block Diagram



TMS320C6211

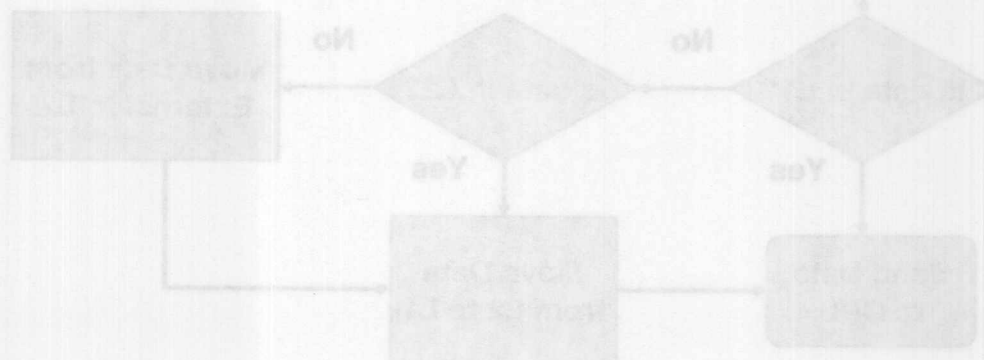
- 1.5-watt typical internal active power
- \$0.02 / MIPS ... with 'C6000 performance

Two-level cache:

- L1 Program / Data
- L2 unified space (program or data as needed)

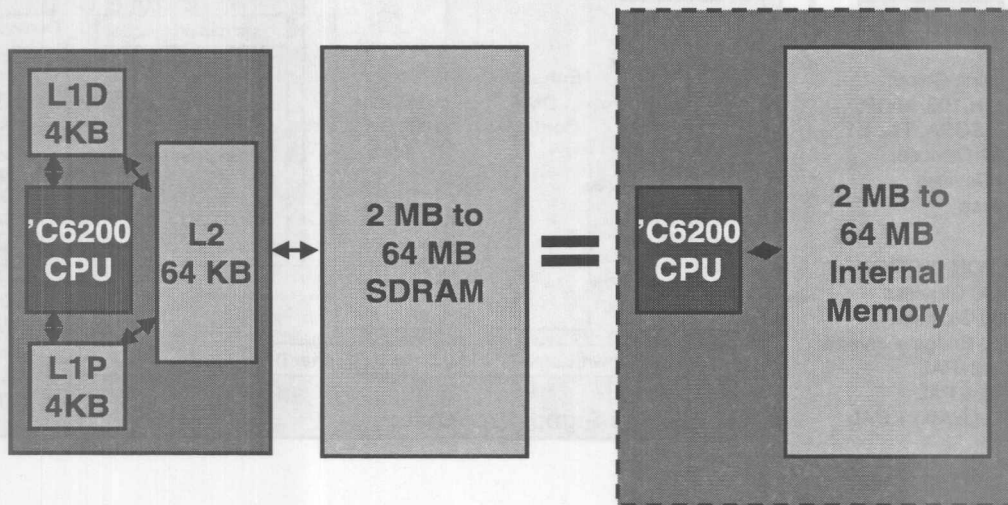
Enhanced DMA:

- 16 channels
- 600 MB/sec
- Optimized for efficient use of memory
- Services all CPU and cache requests (makes cache transparent to user)



'C6211: Turns KB into MB

'C6211 Two-Level Cache turns
72 KB cache into 2 MB - 64 MB on-chip memory

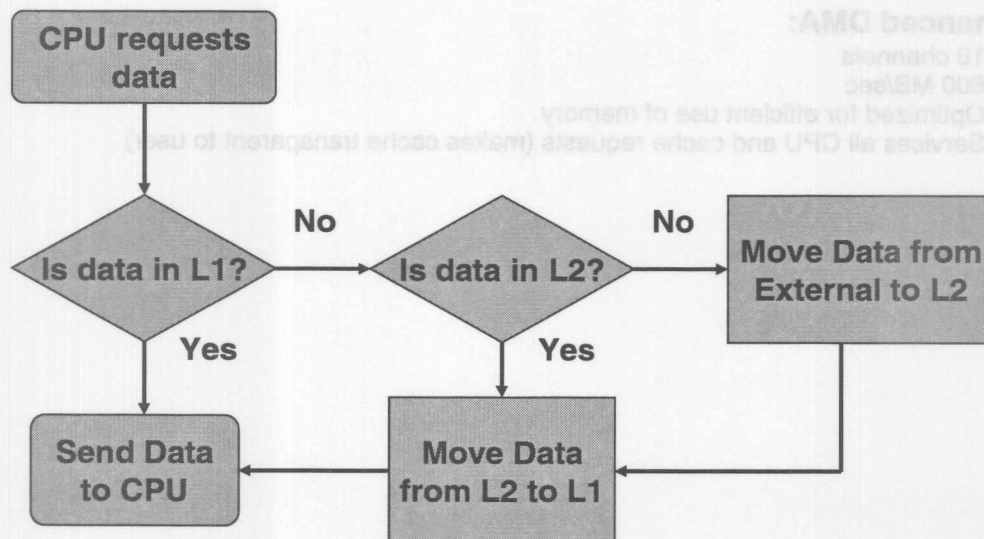


68

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

'C6211: L1/L2 cache flow



69

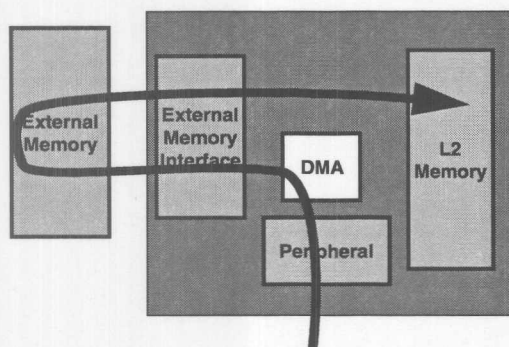
THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

'C6211: L2 flexibility

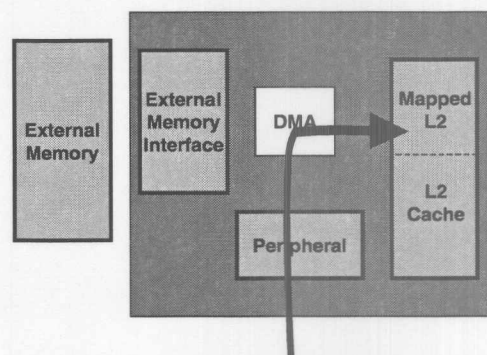
■ Typical cache architecture

- ♦ Lacks non-cacheable regions
- ♦ Requires external storage of peripheral data



'C6211

- ♦ Configurable as cache and direct mapped
- ♦ Allows peripheral data storage on-chip



70

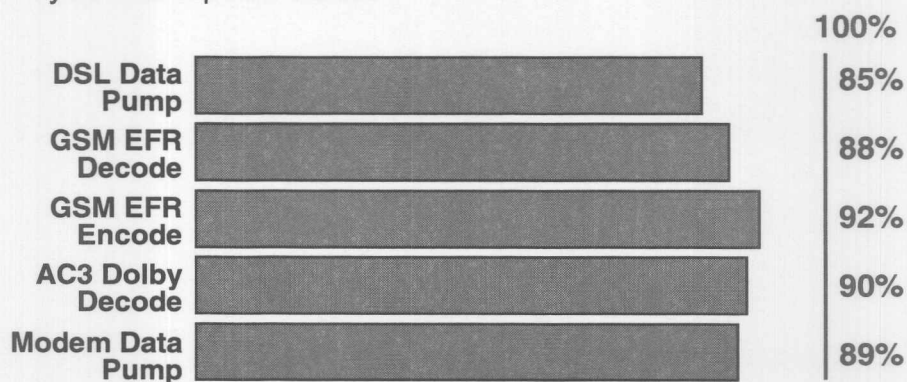
THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

'C6211: L1/L2 cache benchmarks

Performance relative to 'C62x infinite on-chip memory

Cycle count performance



71

THE WORLD LEADER IN DSP SOLUTIONS

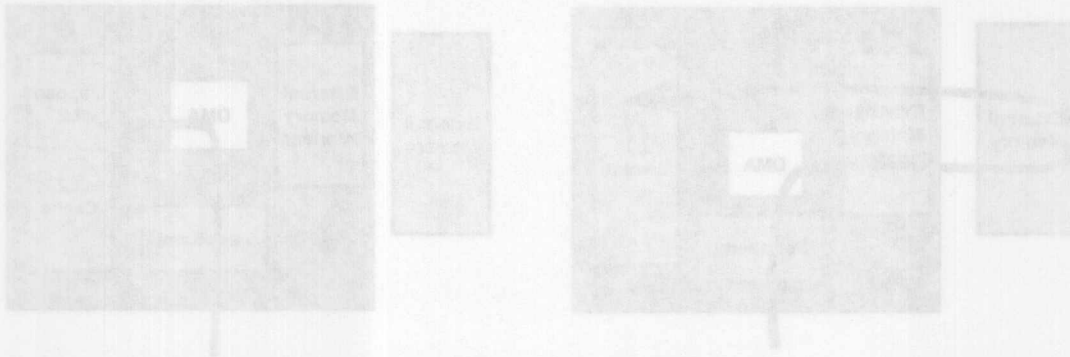
TEXAS
INSTRUMENTS

For a list of related application reports, white papers, and Designer Notebook Pages, see the Appendix.

'C6211: L2 flexibility

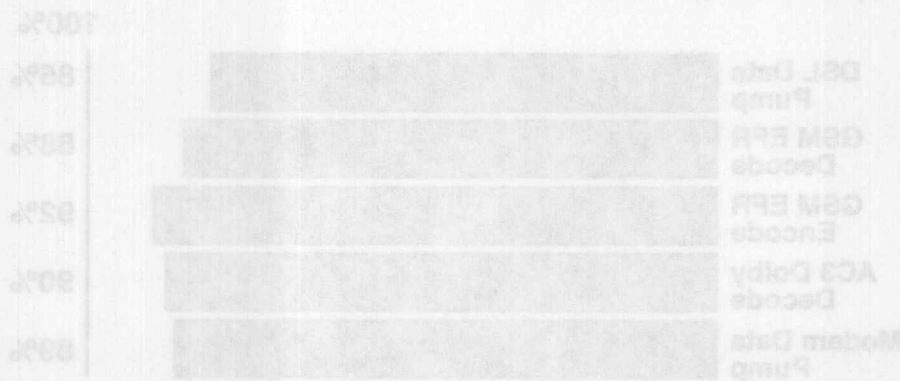
Typical cache architecture 'C6211

- Lacks non-cacheable regions
- Requires external storage of peripheral data
- Configurable as cache and direct mapped
- Allows peripheral data storage on-chip



'C6211: L1/L2 cache benchmarks

Performance relative to
'C62x infinite on-chip memory
Cycle count performance



For a list of related application reports, white papers, and Designer Notebook Pages, see the Appendix.



How do I work with TI's 'C6000?

What performance can I expect?

How do I get my performance?

How do I interface easily?

What are the new 'C6000 devices?

What is my power consumption?

How does TI enable maximum performance at lower cost?

72

THE WORLD LEADER IN DSP SOLUTIONS



'C6000: Power consumption

Power consumption is a product of:

- ✓ Internal memory accesses
- ✓ Functional units running per cycle
- ✓ External memory accesses
- ✓ Efficient process technology

... 'C6000 produces up to 10x the industry's highest raw performance with industry-standard or better consumption levels.

73

THE WORLD LEADER IN DSP SOLUTIONS





<1.9 W at industry-standard activity

Industry-standard power measurements

- 50/50 activity
- CPU & memory only

		50% High 50% Low 'C6201B		75% High 25% Low 'C6201B	
		% of Total	W @ 200 MHz	% of Total	W @ 200 MHz
CPU and Memory	CPU	17%	0.42	18%	0.49
	Internal memory	8%	0.18	8%	0.22
	Clocking	44%	1.07	39%	1.07
	Total	69%	1.7	66%	1.8
Peripherals	DMA/EMIF	3%	0.07	3%	0.09
	DMA memory access	9%	0.21	12%	0.31
	Other	0%	0.01	0%	0.01
	Total	12%	0.3	15%	0.4
Core VDD (2.5 or 1.8V total)		81%	2.0	81%	2.2
I/O (DVDD) Total		19%	0.4	19%	0.5
TOTAL		100%	2.4	100%	2.7

74

THE WORLD LEADER IN DSP SOLUTIONS



'C6201B 1-2 Watt Power

- 1.7 W in industry-standard power measurements
 - 50/50 activity
 - CPU & Memory
- 2.0–2.2 W typical on-chip power
- 2.4–2.7 W typical total chip power with significant external access

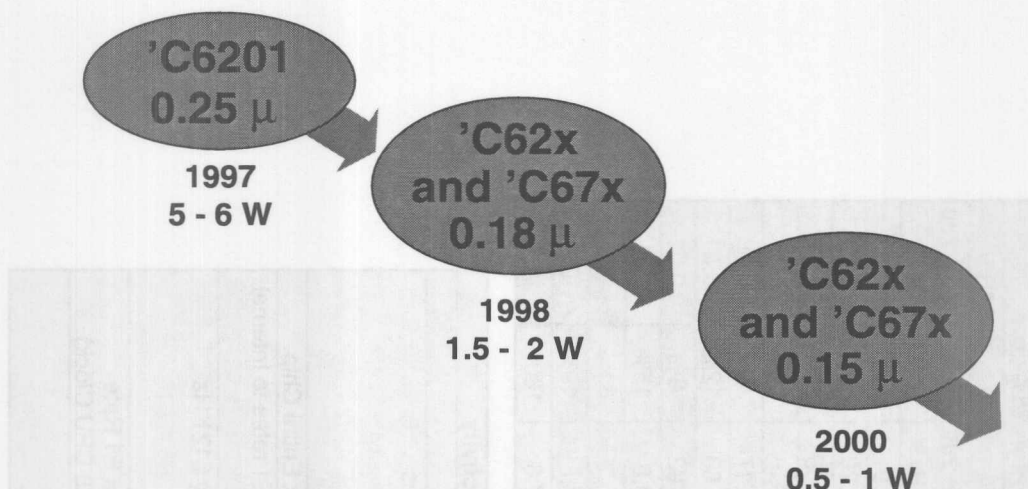
'C6201B 1-2 Watt Power

		50% High 50 % Low				75% High 25% Low			
		6201		6201B		6201		6201B	
		% of Total	W @ 200 MHz	% of Total	W @ 200 MHz	% of Total	W @ 200 MHz	% of Total	W @ 200 MHz
CPU and Memory	CPU	12%	0.81	17%	0.42	12%	0.94	18%	0.49
	Internal Memory	41%	2.73	8%	0.18	43%	3.29	8%	0.22
	Clocking	31%	2.05	44%	1.07	27%	2.05	39%	1.07
	Total	85%	5.6	69%	1.7	83%	6.3	66%	1.8
Peripherals	DMA/EMIF	2%	0.14	3%	0.07	2%	0.17	3%	0.09
	DMA Memory Access	6%	0.40	9%	0.21	8%	0.60	12%	0.31
	Other	0%	0.02	0%	0.01	0%	0.02	0%	0.01
	Total	8%	0.6	12%	0.3	10%	0.8	15%	0.4
Core VDD (2.5 or 1.8V total)		93%	6.1	81%	2.0	93%	7.1	81%	2.2
I/O (DVDD) Total		7%	0.4	19%	0.4	7%	0.5	19%	0.5
TOTAL		100%	6.6	100%	2.4	100%	7.6	100%	2.7

Module		High DSP Activity	Low DSP Activity
CPU + Memory	CPU	8 instructions/Cycle	2 instructions/cycle
	CPU	1 Program Fetch/Cycle	1 Program Fetch/4 Cycles
	Memory Access	(256 bits/cycle) 2 Loads/Cycle (64 bits/cycle)	(256 bits/4 cycles) 1 Load/Cycle (32 bits/cycle)
	Clocking	Constant Power to Clock Entire Chip	Constant Power to Clock Entire Chip
Peripherals	DMA/EMIF	Block Transfers to 1/2 Rate Sync. Mem 50% on-to-off/50% off-to-on	Servicing 2 McBSPs at E1 rates to Internal Memory
	DMA Memory Access	32-bits internal data mem/cycle	8 bits internal memory @ 512 KHz
	Other	2 McBSPs @ Full Duplex E1 Rate 2 timers @ Max Rate (1/8 CPU Clock)	2 McBSPs @ Full Duplex E1 Rate 2 timers @ Max Rate (1/8 CPU Clock)
IO		50% 100 MHz Reads 50% 100 MHz Writes	None



'C6000: Lower power consumption



Typical 200-MHz CPU and memory power consumption

75



THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



'C6000: Power down modes

- ◆ **Mode 1**
Shut off CPU clocks
 - Can be revived through peripheral or external interrupts
- ◆ **Mode 2**
Shut off all CPU clocks / Leave PLL on
 - Can be revived through reset
- ◆ **Mode 3**
Shut off all CPU clocks and PLL
 - Can be revived through reset

76

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

For a list of related application reports, white papers, and Designer Notebook Pages, see the Appendix.



How do I work with TI's 'C6000?

What performance can I expect?

How do I get my performance?

How do I interface easily?

What are the new 'C6000 devices?

What is my power consumption?

How does TI enable maximum performance at lower cost?

77

THE WORLD LEADER IN DSP SOLUTIONS



'C6202: Lowest \$ per channel

	'C6202 Channels @ 250 MHz	'C6202 @ \$130 ea \$/Chn	Typical Channels @ 100 MHz	Typical* @ \$30 ea \$/Chn
G.729A	36+	<\$ 3.61	6	\$ 5.00
G.723.1	28+	<\$ 4.64	5	\$ 6.00
G.726	60-100	\$ 2.16 - 1.30	10+	<\$ 3.00
Echo Canc. (32-msec tail)	60+	<\$ 2.17	10	\$ 3.00
GSM EFR	20+	<\$ 6.50	4-6	\$ 7.50
V.34/V.90	15-18	\$ 8.66	3	\$10.00

78

* Large on-chip RAM device



THE WORLD LEADER IN DSP SOLUTIONS

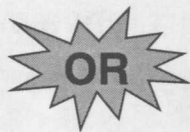




'C6701: Lowest \$ per MFLOPS

400 MMACS for \$300*

ADI-21160
667 MFLOPS



668 MMACS for \$165

'C6701
1 GFLOPS

'C6701 floating-point silicon available today:

- ◆ Ultra-high precision
- ◆ Development in C code, with highly efficient tools available today
- ◆ Assembly-source-code compatible with 'C62x fixed-point devices

79

TI and ADI sample pricing

*Source: ADI News Release 6/22/98.

THE WORLD LEADER IN DSP SOLUTIONS



'C6211: Greatest value per \$25

100-120 MMACS
for \$15 - 40

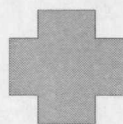
Typical
100 MIPS



300 MMACS for \$25

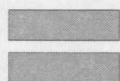
'C6211
1200 MIPS

**Longer
development**



**Efficient
C compiler**

???



**Faster
Time to Revenue**

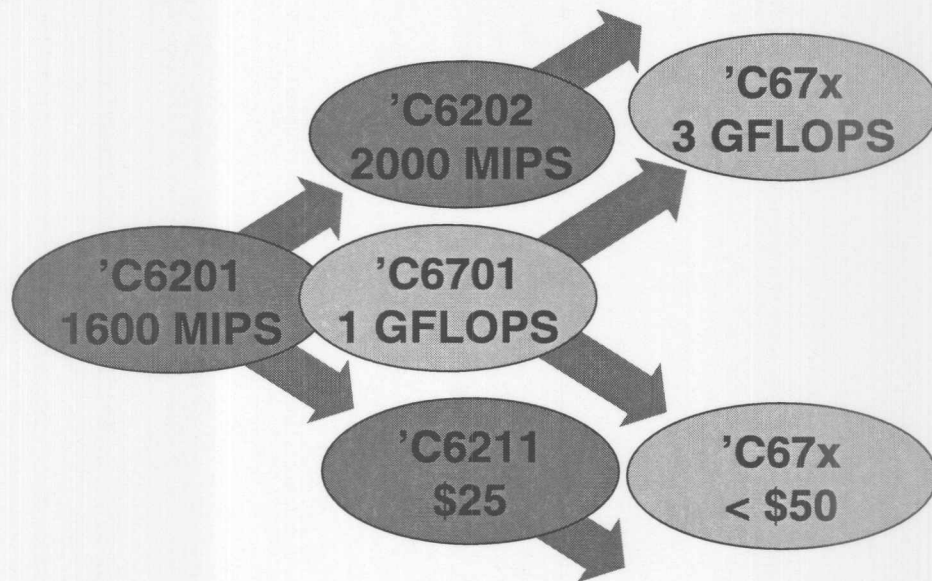
80

THE WORLD LEADER IN DSP SOLUTIONS





'C6000: Universal platform



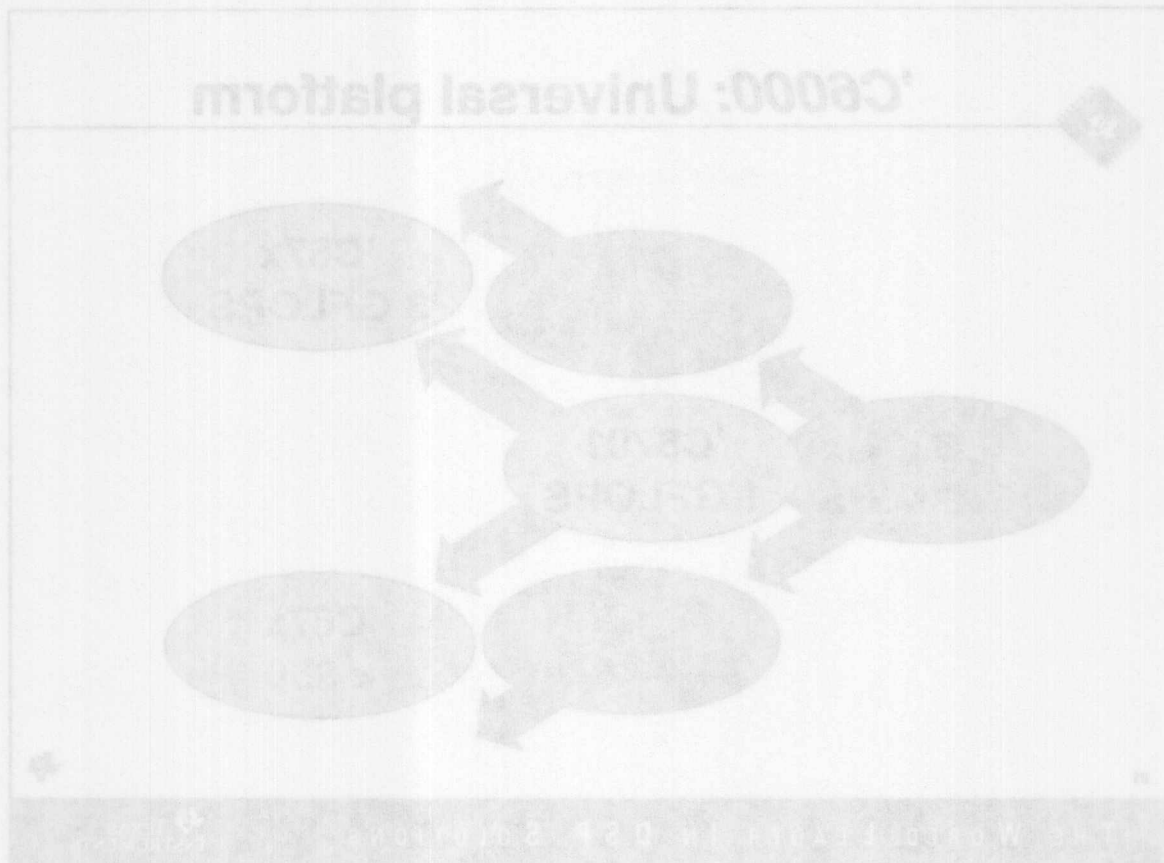
81



THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

For a list of related application reports, white papers, and Designer Notebook Pages, see the Appendix.



Appendix
For a list of related application reports, white papers, and Designer Notebook Pages, see the



Today's Agenda

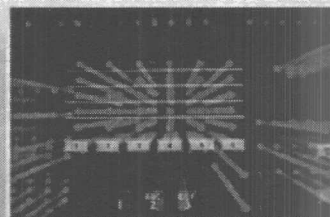
- ✓ What are my system requirements?
- ✓ How do I work with TI's 'C6000?
- ✓ How do I work with TI's 'C5000?

How do TI's tools make my development easier?

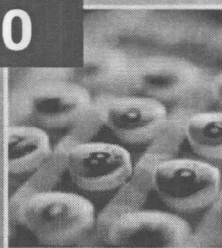
What support can I count on?

1

THE WORLD LEADER IN DSP SOLUTIONS



TMS320C5000



2

THE WORLD LEADER IN DSP SOLUTIONS





How do I work with TI's 'C5000?

How do I get my performance?

What performance can I expect?

How do I interface easily?

What are the new 'C5000 devices?

How do I minimize power consumption?

How does TI enable power-efficient performance at lower cost?

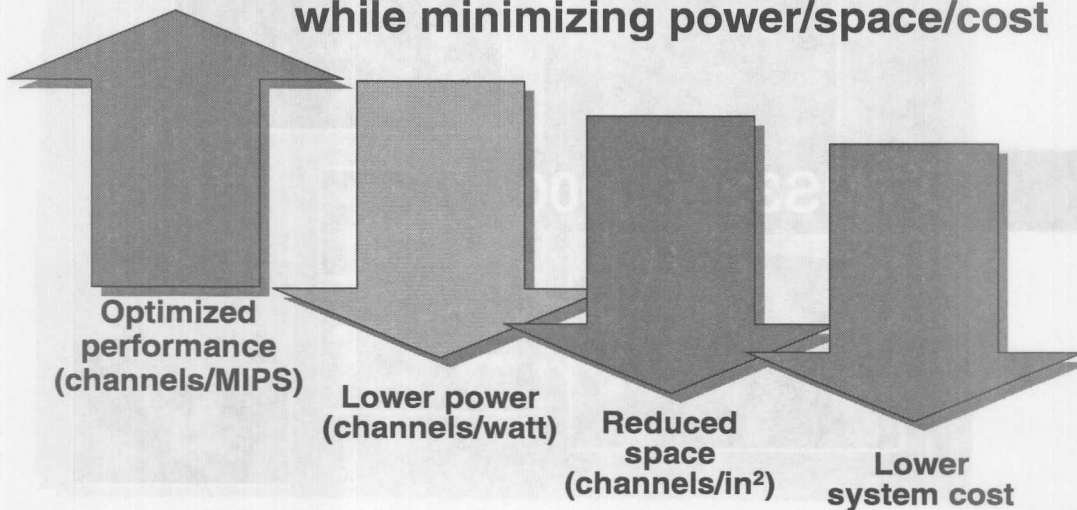
3

THE WORLD LEADER IN DSP SOLUTIONS



'C5000: Power-efficient performance

Efficient MIPS and on-chip memory/peripherals...
while minimizing power/space/cost



4

THE WORLD LEADER IN DSP SOLUTIONS





Architecture optimized for DSP

#1: CPU designed as a DSP engine

- An execution environment that handles 32-bit constructs in a 16-bit architecture

#2: Multiple busses for efficient data and program flow

- Four busses and large on-chip memory that result in sustained performance near peak

#3: Highly tuned instruction set for powerful DSP computing

- Sophisticated instructions that execute in fewer cycles, with less code and low power demands

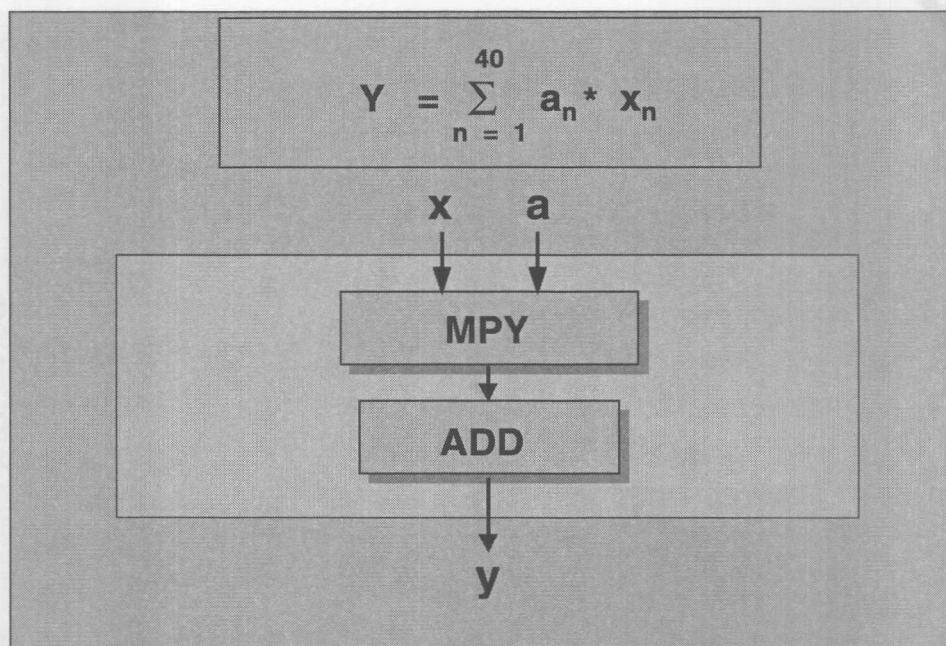
5



THE WORLD LEADER IN DSP SOLUTIONS



Key #1: DSP engine



6

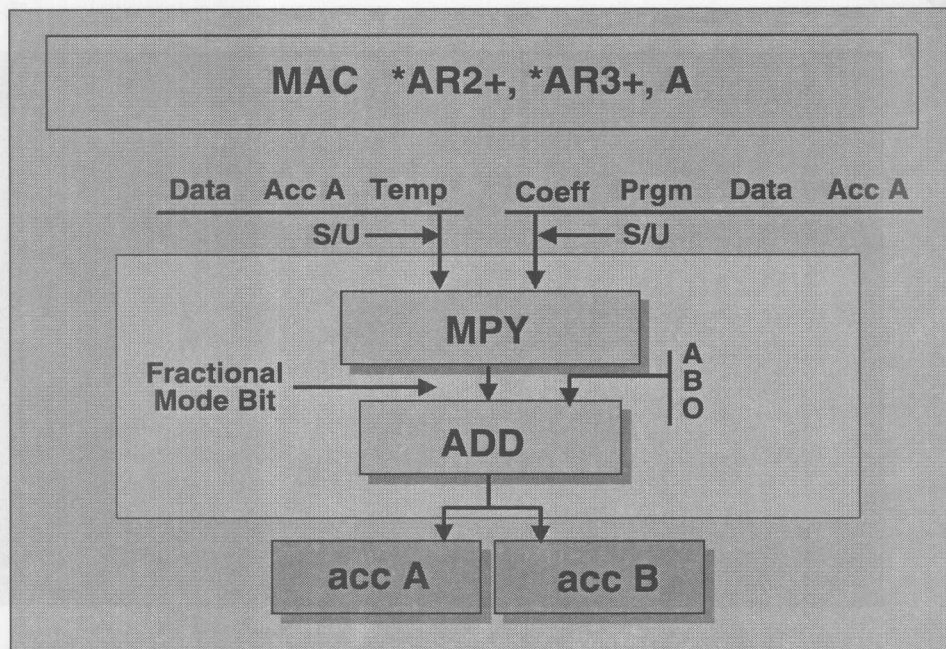


THE WORLD LEADER IN DSP SOLUTIONS





Key #1: MAC Unit



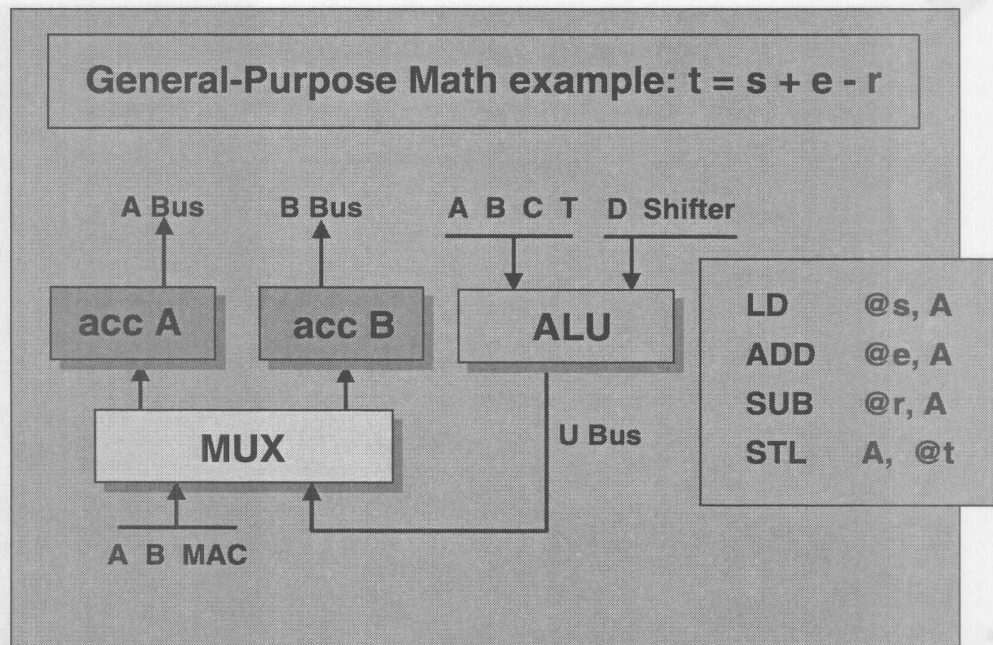
7

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



Key #1: Accumulators + Adder



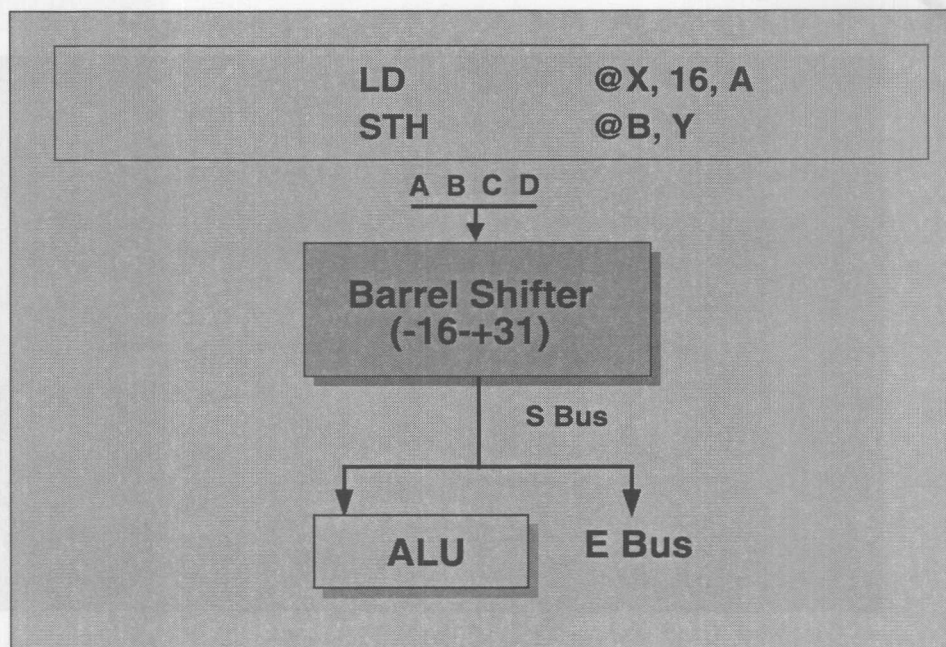
8

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



Key #1: Barrel shifter



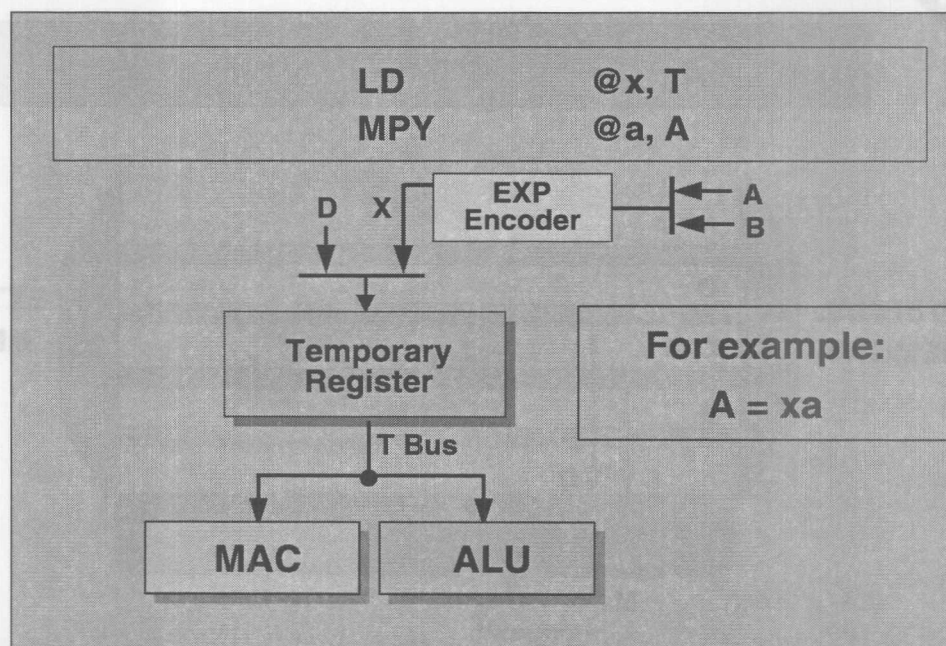
9

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



Key #1: Temporary register



10

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



Key #2: Efficient data/program flow

#1: CPU designed as a DSP engine

- An execution environment that handles 32-bit constructs in a 16-bit architecture

#2: Multiple busses for efficient data and program flow

- Four busses and large on-chip memory that result in sustained performance near peak

◆ #3: Highly tuned instruction set for powerful DSP computing

- Sophisticated instructions that execute in fewer cycles, with less code and low power demands

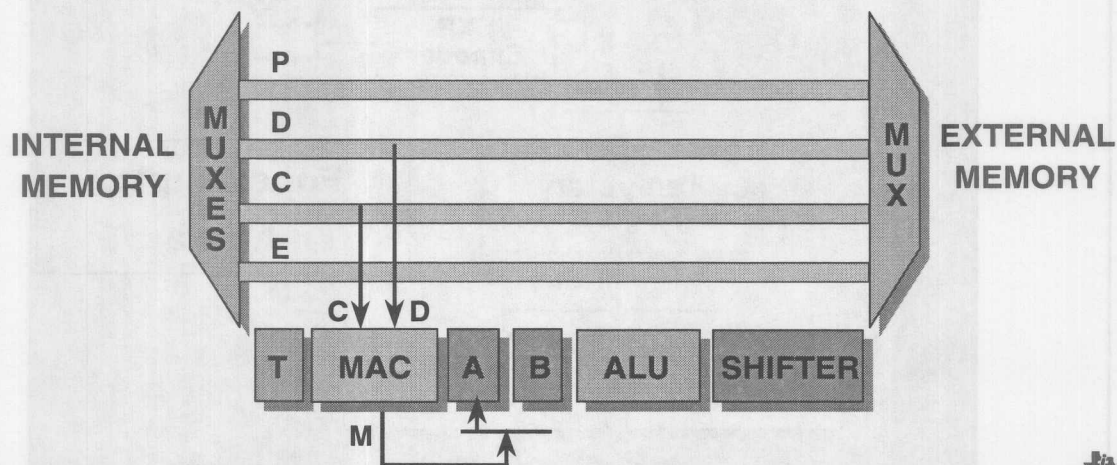
11

THE WORLD LEADER IN DSP SOLUTIONS



Key #2: Multiple busses

MAC *AR2+, *AR3+, A



12

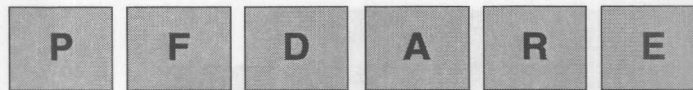
THE WORLD LEADER IN DSP SOLUTIONS





Key #2: Pipeline

Prefetch Fetch Decode Access Read Execute



- ◆ Prefetch: Calculate address of instruction
- ◆ Fetch: Collect instruction
- ◆ Decode: Interpret instruction
- ◆ Access: Collect address of operand
- ◆ Read: Collect operand
- ◆ Execute: Perform operation

13

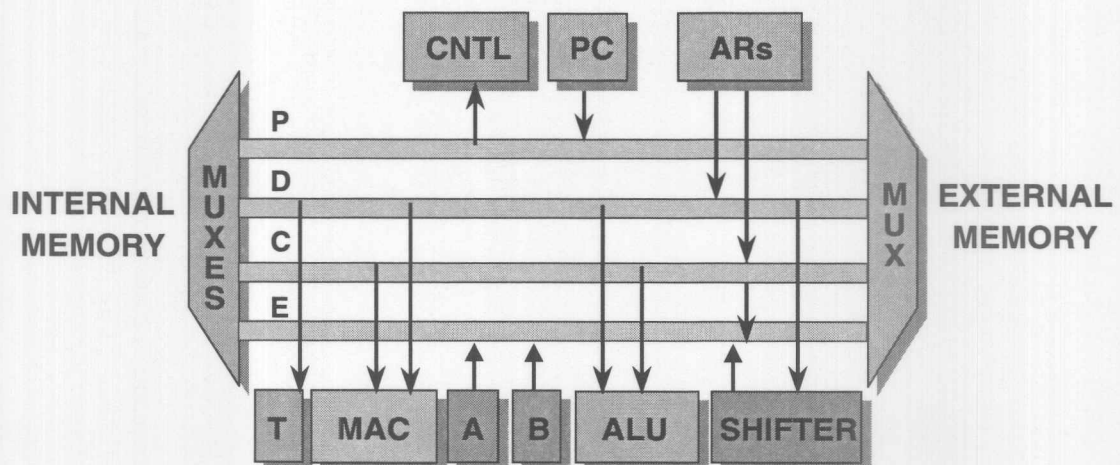


THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



Key #2: Bus usage



14

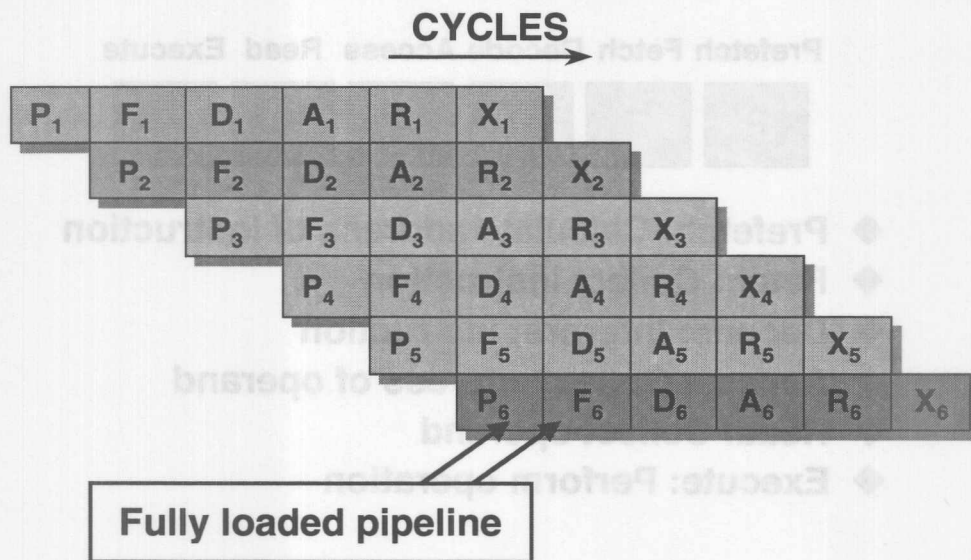


THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

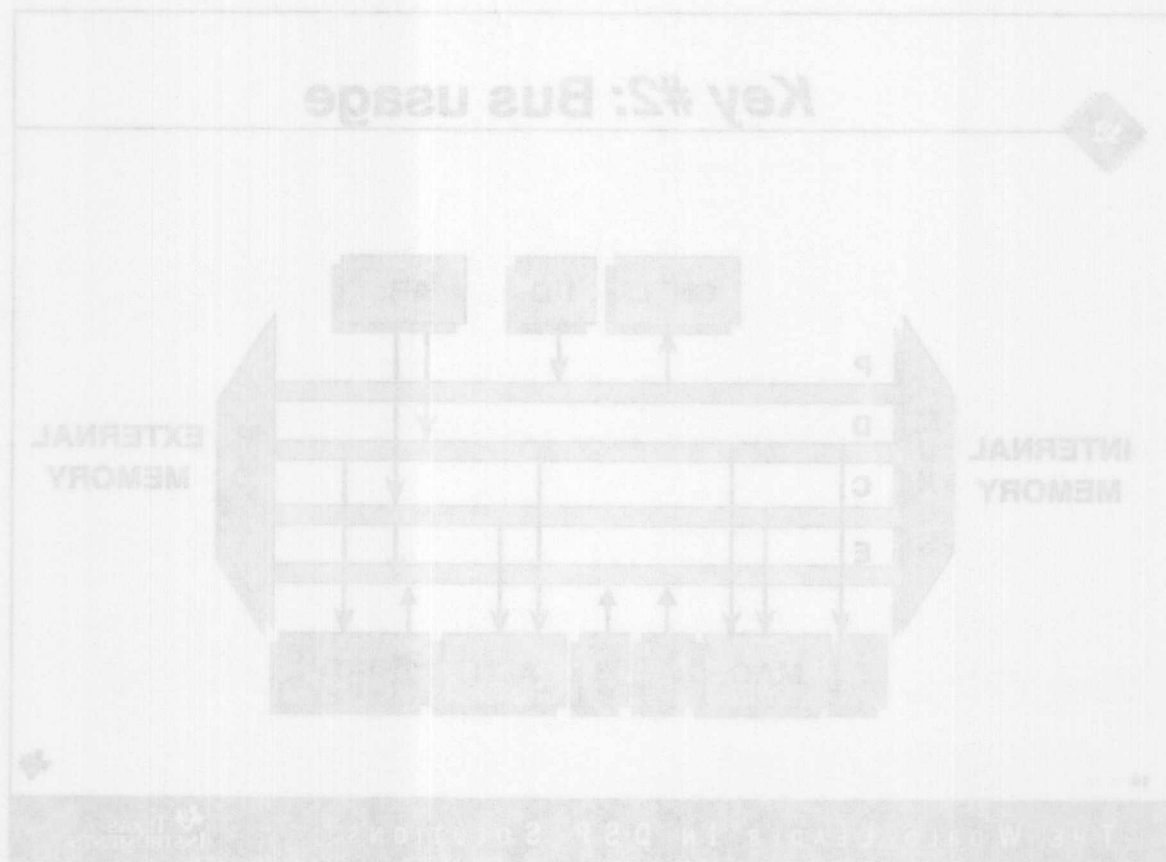


Key #2: Pipeline performance



15

THE WORLD LEADER IN DSP SOLUTIONS





Key #3: Powerful instructions

◆ #1: CPU designed as a DSP engine

- An execution environment that handles 32-bit constructs in a 16-bit architecture

◆ #2: Multiple busses for efficient data and program flow

- Four busses and large on-chip memory that result in sustained performance near peak

#3: Highly tuned instruction set for powerful DSP computing

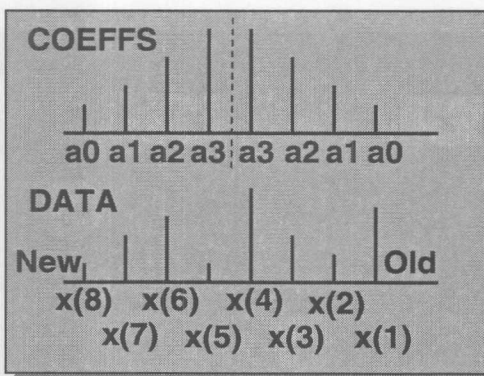
- Sophisticated instructions that execute in fewer cycles, with less code and low power demands

16

THE WORLD LEADER IN DSP SOLUTIONS



Key #3: Symmetric FIR Filter



Symmetric FIR Filters are commonly used in applications where phase distortion may degrade the signal quality, e.g.: modems.

The general form of this FIR equation is written using 8 Mults, 7 Adds

$$Y(n) = a_0x(8) + a_1x(7) + a_2x(6) + a_3x(5) + a_3x(4) + a_2x(3) + a_1x(2) + a_0x(1)$$

In the specific case of a Symmetric FIR we can use 4 Mults, 7 Adds

$$Y(n) = a_0(x(8) + x(1)) + a_1(x(7) + x(2)) + a_2(x(6) + x(3)) + a_3(x(5) + x(4))$$

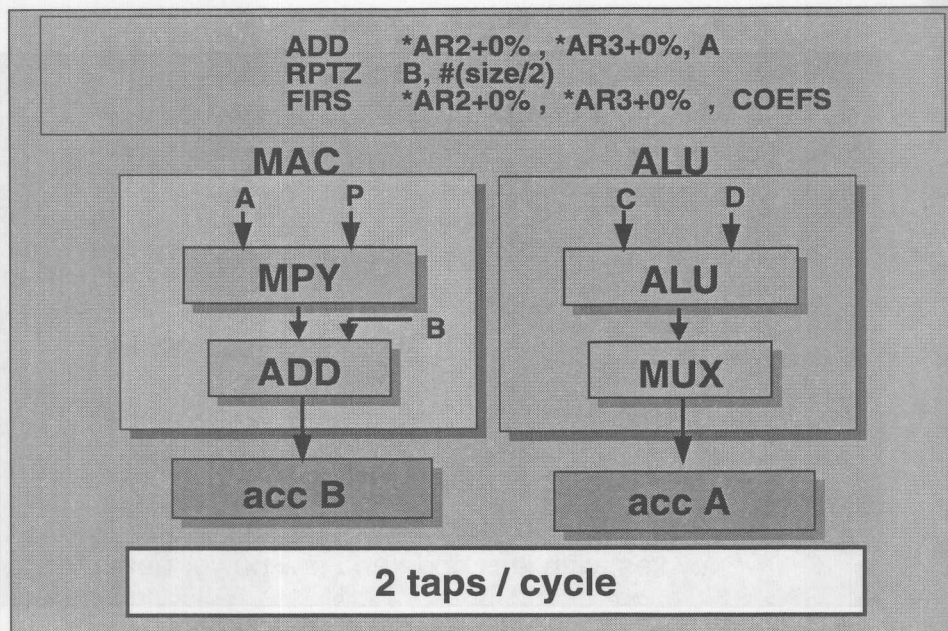
17

THE WORLD LEADER IN DSP SOLUTIONS





Key #3: FIRS



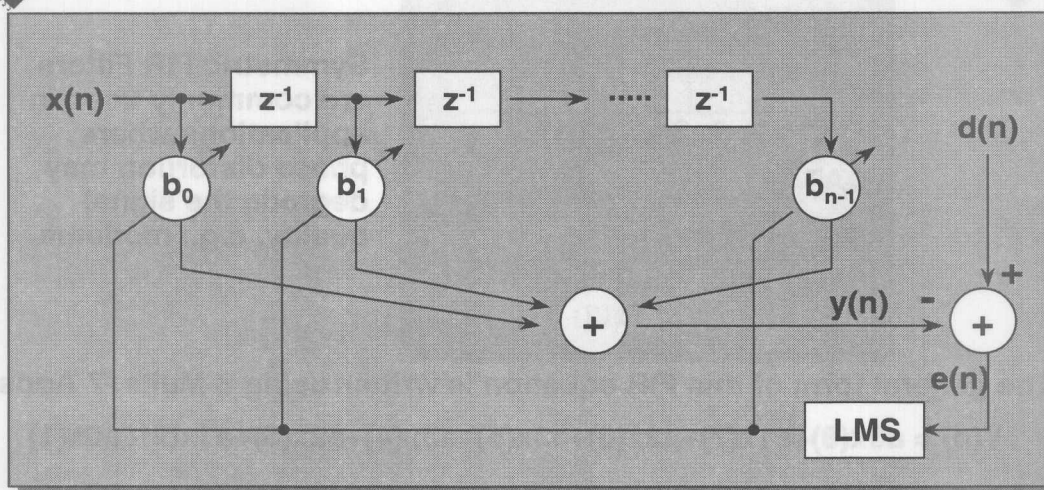
18

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



Key #3: Adaptive FIR filter using LMS



FIR type filters are usually used in an adaptive algorithm since they are more tolerant of non-optimal coefficients.

19

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



Key #3: LMS loading

Each Iteration (only once)

- 1 - determine error :
- 2 - scale by "rate" term B :

$$e(i) = d(i) - y(i)$$

$$e'(i) = 2*B*e(i)$$

Each Term (N sets)

- 3 - Qualify error with signal strength :
- 4 - Sum error with coefficient :
- 5 - Update coefficient :

$$e''(i) = x(i-k) * e'(i)$$

$$b(i+1) = b(i) + e''(i)$$

$$b(i) = b(i+1)$$

Analysis :

@100 tap: 200 cycles

LMS:	1	1	SUB
	2	1	MPY
	3	N	MPY
	4	N	ADD
	5	N	STH
FIR	a	N	MPY
	b	N	ADD
	c	1	STH

ST
|| MPY

LMS

20

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



Key #3: MAC + ALU enables LMS

LMS *AR2+0%, *AR3+0%

FIR

MAC

D

C

MPY

ADD

acc B

B

LMS

ALU

A

D

ALU

MUX

acc A

21

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



Key #3: Advanced applications

- | | |
|------------------------|------|
| ◆ Symmetric FIR filter | FIRS |
| ◆ Adaptive filtering | LMS |

Polynomial evaluation
Code book search

Viterbi

POLY
STRCD
SACCD
SRCCD
DADST
DSADT
CMPS

22

THE WORLD LEADER IN DSP SOLUTIONS



'C5000 Advanced Applications

For more information, please see *Mnemonic Instruction Set Reference Set* (Lit. # SPRU172)

POLY: Useful to generate signals via their polynomial approximation (for example, sine wave generations, trigonometric expressions, and any function that can be approximated as a polynomial series).

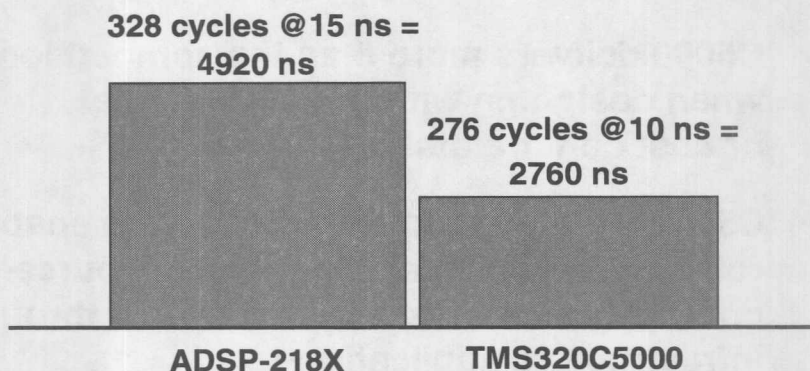
SRCCD, STRCD, SACCD: Used to implement fast searches (for example, the codebook search for excitation signal in vocoders (speech coding) such as CELP).

DADST, DSADT: Used together with the CMPS instruction to implement the Viterbi algorithm—used in convolutional encoding for error control (telecom).



Key #3: FIR Filter in fewer cycles

'C5000 is squeezing the work done by a 24-bit processor into less time on a 16-bit processor



Full source code is listed in your Seminar Guide

23 Source: TI internal testing on source code referenced in Seminar Guide.

THE WORLD LEADER IN DSP SOLUTIONS



Sample Code Example: FIR Filter (ADI 218X vs. 'C5000)

Sixteen-tap FIR filter source code used to evaluate performance:

ADSP-218X

```
13=^delay
L3=%delay
M3=1
l1=^coeff
L1=%coeff
l4=^output
L4=0
mr=0
ay0=pm(l1,M3)
cntr=15
do loop2 until ce;
ax0=dm(port)
dm(i3,m3)=ax0
  cntr=15
  do order until ce;
  order
mr=mr+ax0*ay0;ay0=pm(i1.m3),ax0=dm(i3,m3)
loop2  dm(i4,m3)=mr
```

TMS320C5000

```
Filter3:
rsbx  ovm
stm   #8,BK
stm   #delay,AR2
stm   #delay1,AR3
stm   #14,BRC
stm   #0,ar0
1d    #0,ASM
portr port1,*ar2
rptbd loop3-1
stm   #output,ar4
rptz  B,#order/2
firs  *ar2+0%,*ar3+0%,coeff
ll1d  *ar2,A
portr port1,*ar2
mar   *ar3-%
sth   A,*ar3-%
loop3:
```



- 24



TEXAS
INSTRUMENTS



How do I work with TI's 'C5000?

How do I get my performance?

What performance can I expect?

How do I interface easily?

What are the new 'C5000 devices?

How do I minimize power consumption?

How does TI enable power-efficient performance at lower cost?

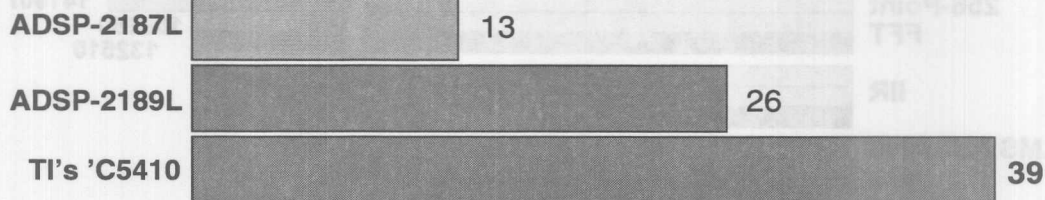
25

THE WORLD LEADER IN DSP SOLUTIONS



'C5000: More performance per Watt

Less power consumption = Up to 3x channels



1 Channel = G.723.1 + Echo Cancellation + VOP processing
Power budget = 2 Watts

26

Source: Analog Devices news releases and web site

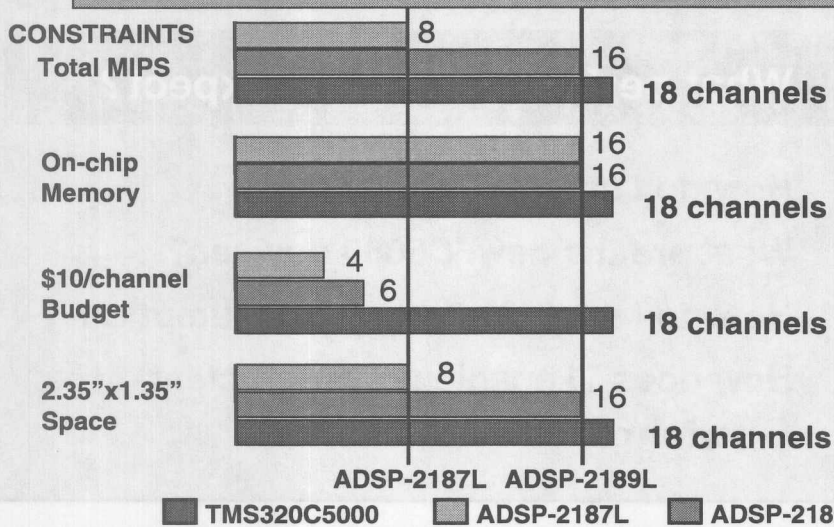
THE WORLD LEADER IN DSP SOLUTIONS





'C5000: Performance per constraint

Competitors are limited by available MIPS
(1 Channel = G.723.1 + Echo Cancellation + VOP processing)



Source:
Analog Devices
news releases
and web site

27

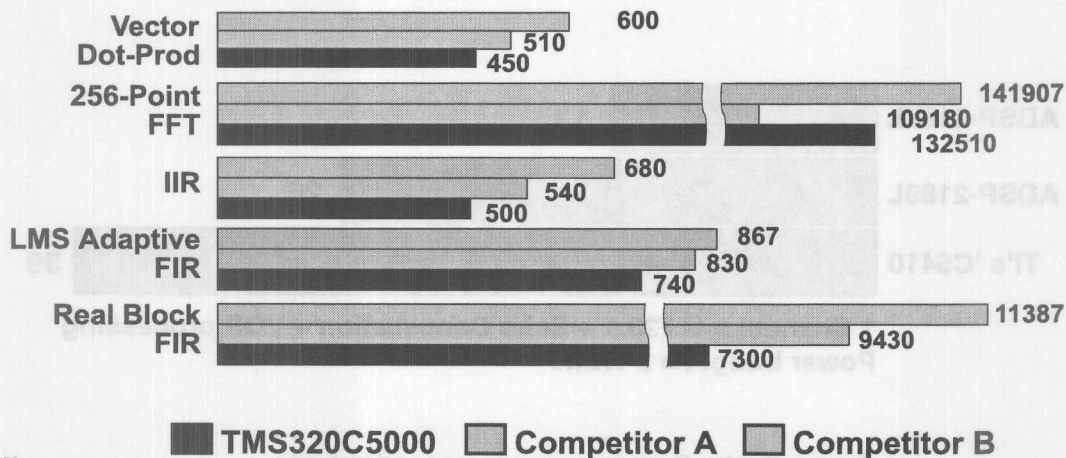
THE WORLD LEADER IN DSP SOLUTIONS



'C5000: DSP functions

Execution Time vs. Major Competitors (in ns.)

Source: *Buyer's Guide to DSP Processors*, ©1999 BDTI



28

THE WORLD LEADER IN DSP SOLUTIONS



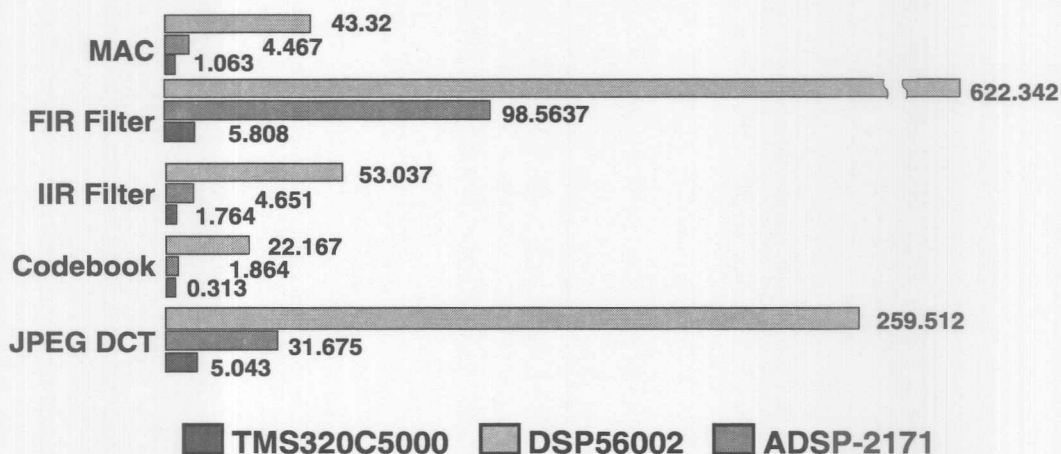
Source: *Buyer's Guide to DSP Processors*, ©1999 Berkeley Design Technology, Inc.



'C5000 Compiler: Lowest cycle count

Compiler Performance vs. Competition

Cycles per task measured over 1000 cycles



29 Source: TI internal testing on source code referenced in Seminar Guide.

THE WORLD LEADER IN DSP SOLUTIONS



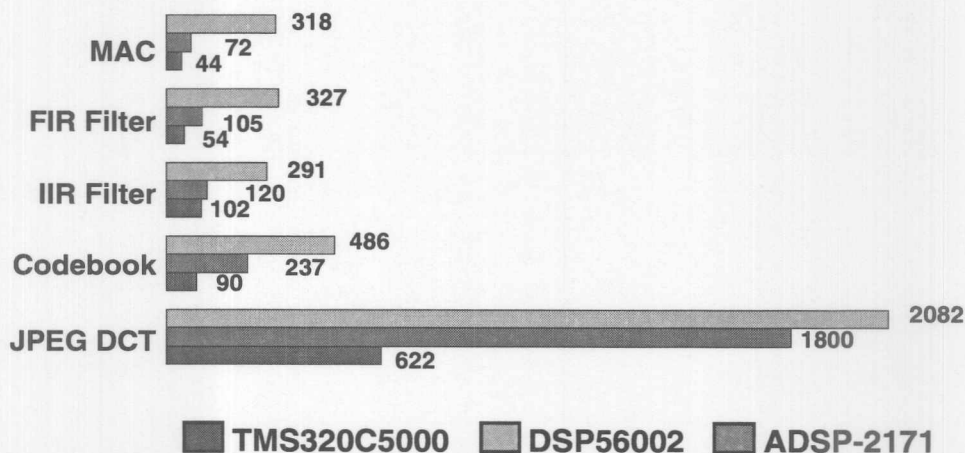
Reference: Public Domain C Source Code
www.ednmag.com/reg/1997/060597/12df.02.cfm



'C5000 Compiler: Smallest code size

Compiler Performance vs. Competition

Measured in bytes



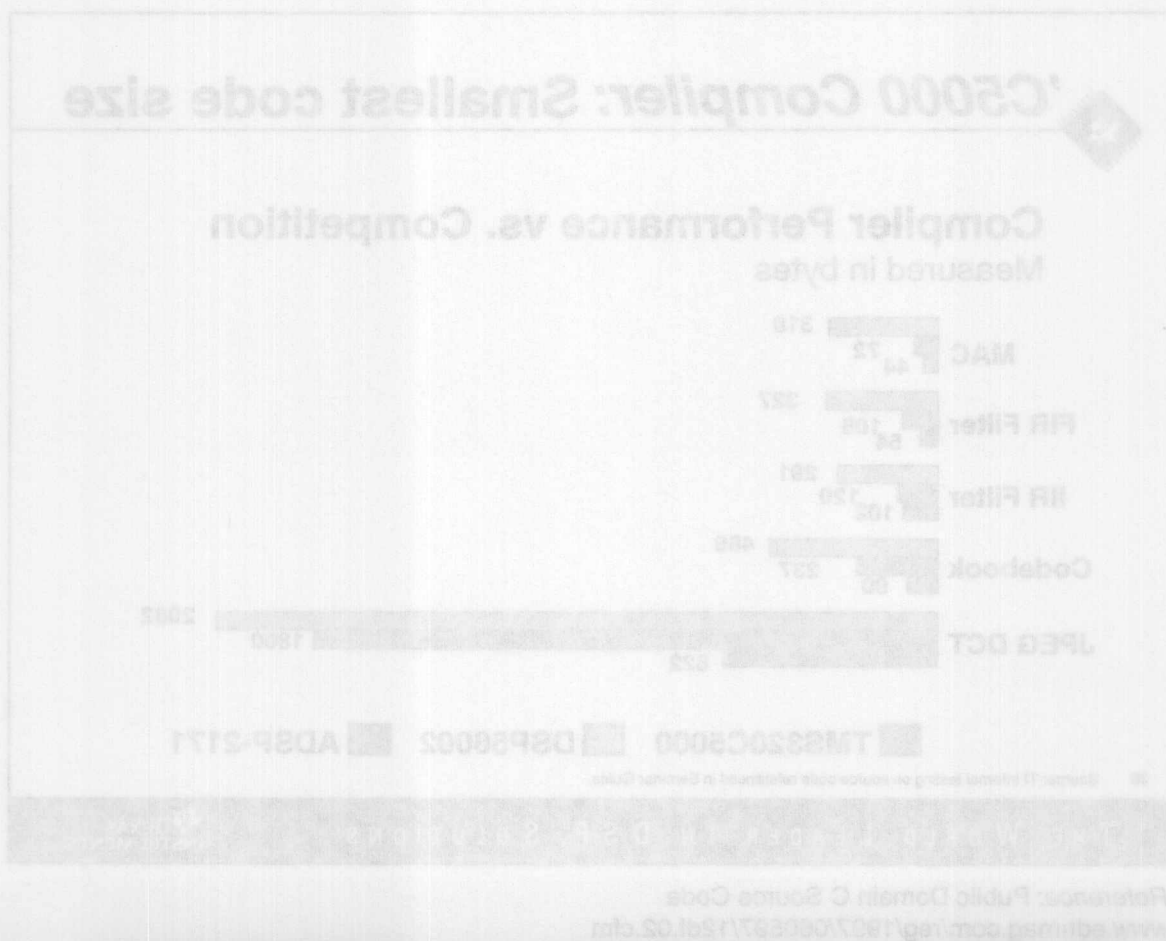
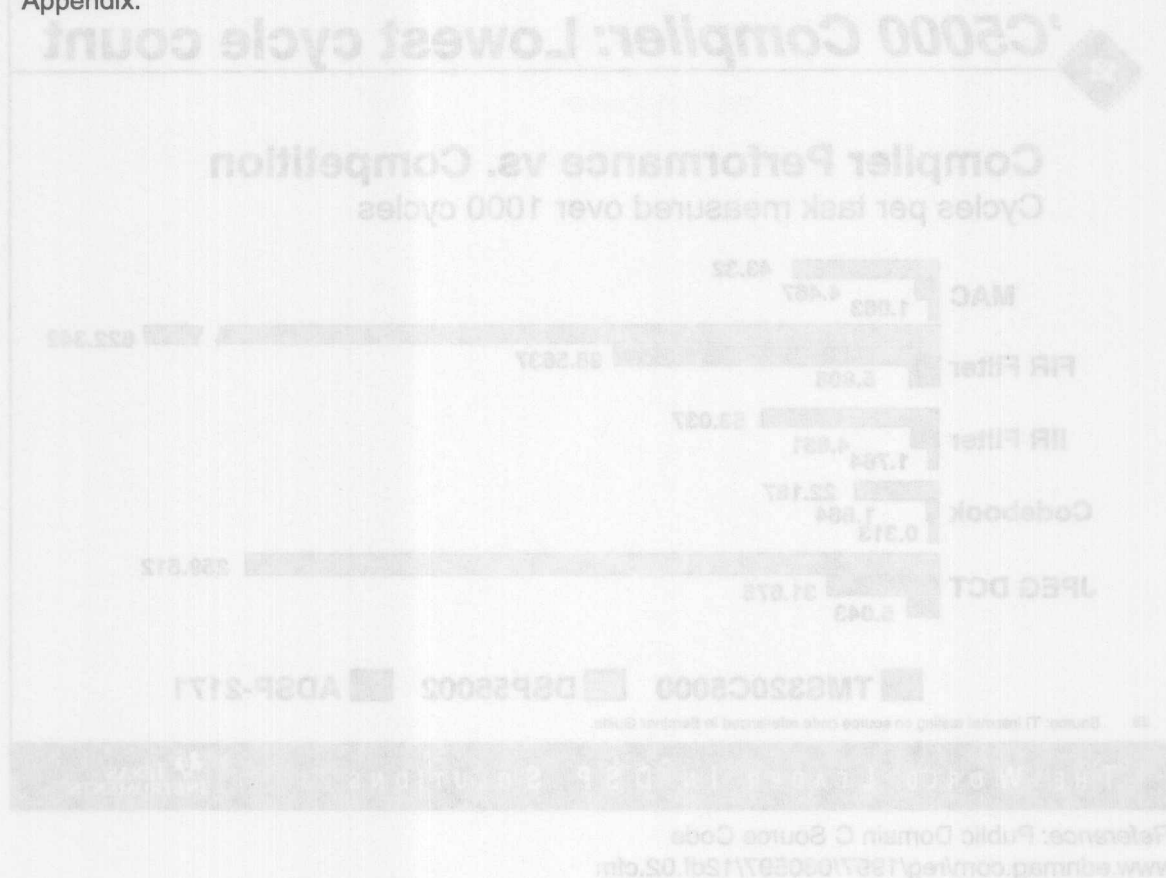
30 Source: TI internal testing on source code referenced in Seminar Guide.

THE WORLD LEADER IN DSP SOLUTIONS



Reference: Public Domain C Source Code
www.ednmag.com/reg/1997/060597/12df.02.cfm

For a list of related application reports, white papers, and Designer Notebook Pages, see the Appendix.





How do I work with TI's 'C5000?

How do I get my performance?

What performance can I expect?

How do I interface easily?

What are the new 'C5000 devices?

How do I minimize my power consumption?

How does TI enable power-efficient performance at lower cost?

31

THE WORLD LEADER IN DSP SOLUTIONS



'C5000: Interfacing

Variety of sources for easy interfacing

- ✓ Internal Memory
- ✓ External Memory Interface (EMIF)
- ✓ Serial Ports:
 - Standard Serial Port
 - Buffered (BSP)
 - Multi-channel (McBSP)
- ✓ Host Port Interface (HPI)
- ✓ Direct Memory Access (DMA)

32

THE WORLD LEADER IN DSP SOLUTIONS

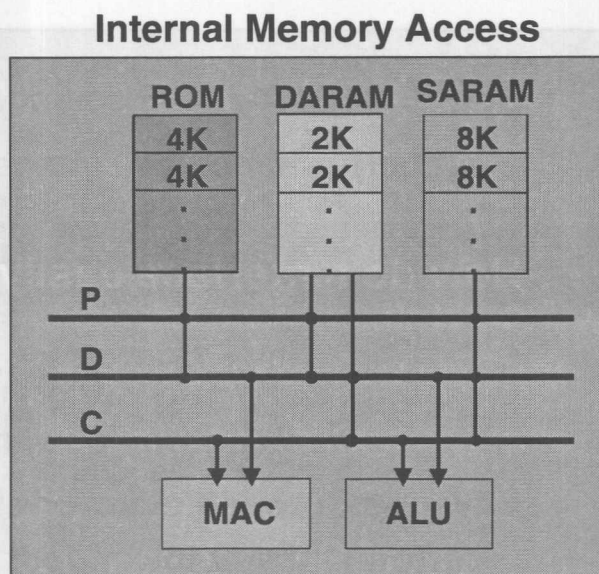




Interfacing: Internal memory access

ROM & RAM:
One access
per block
per cycle

DARAM:
Two accesses
per block
per cycle



33

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



Interfacing: Memory

'C5000	DARAM	SARAM	ROM
'C5420	32 K	168 K	--
'C5402	16 K	--	4 K
'C5410	8 K	56 K	16 K
'C549	8 K	24 K	16 K
'C548	8 K	24 K	2 K
'C545/6	6 K	--	48 K
'C542/3	10K	--	2 K
'C541	5 K	--	28 K

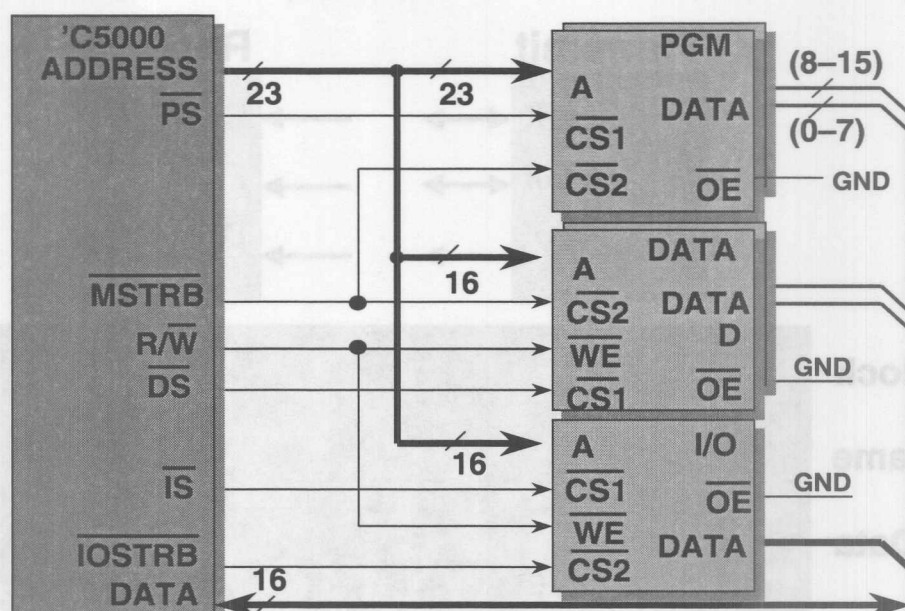
16-bit words

34

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

Interfacing: External Memory I/F



35

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

EMIF: Flexible memory I/F

- ◆ Typical asynchronous parallel interface
- ◆ Separate strobes for program, data and I/O spaces
- ◆ 24-bit address range for external program space
- ◆ 0-14 software programmable wait states
- ◆ Simplified bank switching -- programmable ability to insert wait states when crossing bank boundaries

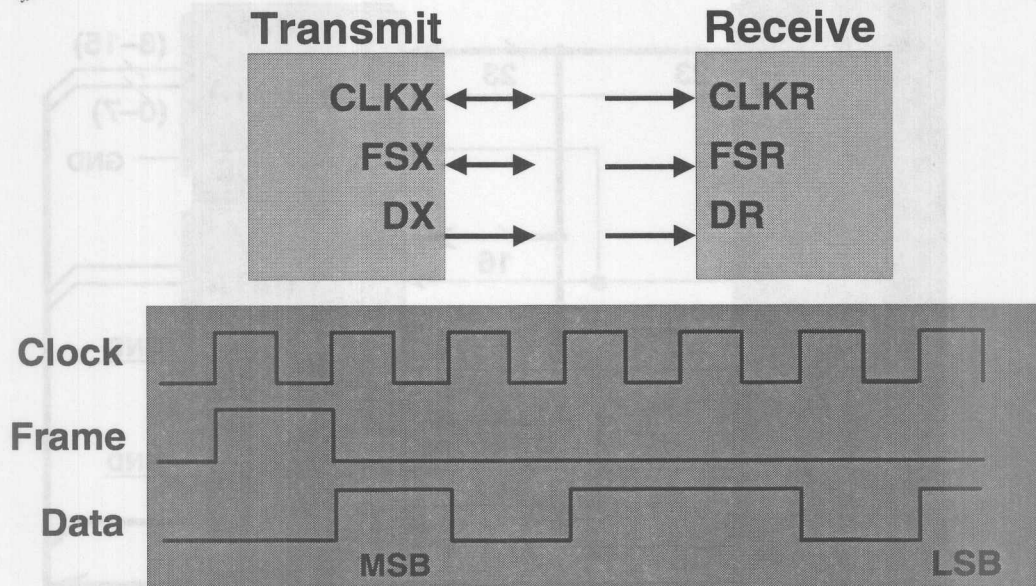
36

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



Standard Serial Port: Pins & signals

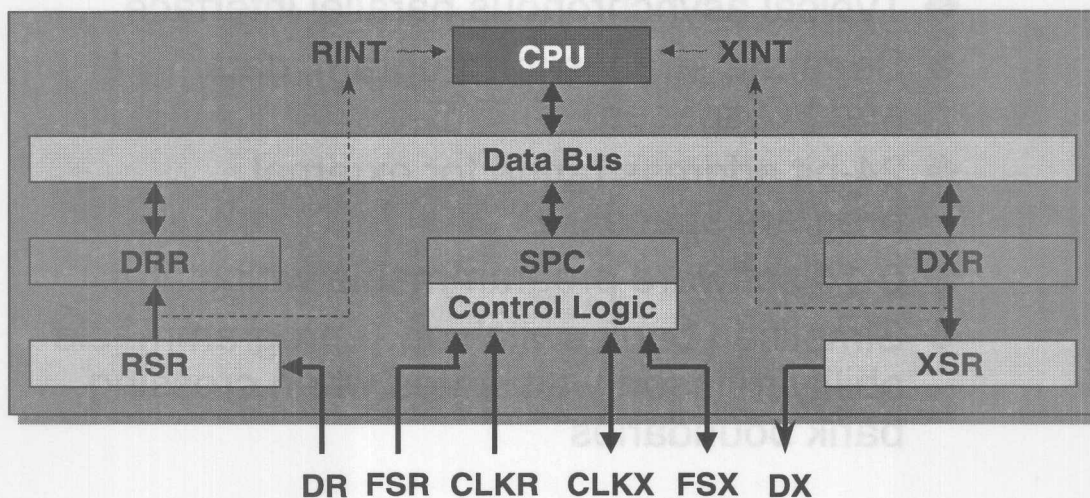


37

THE WORLD LEADER IN DSP SOLUTIONS



Standard Serial Port: Architecture



38

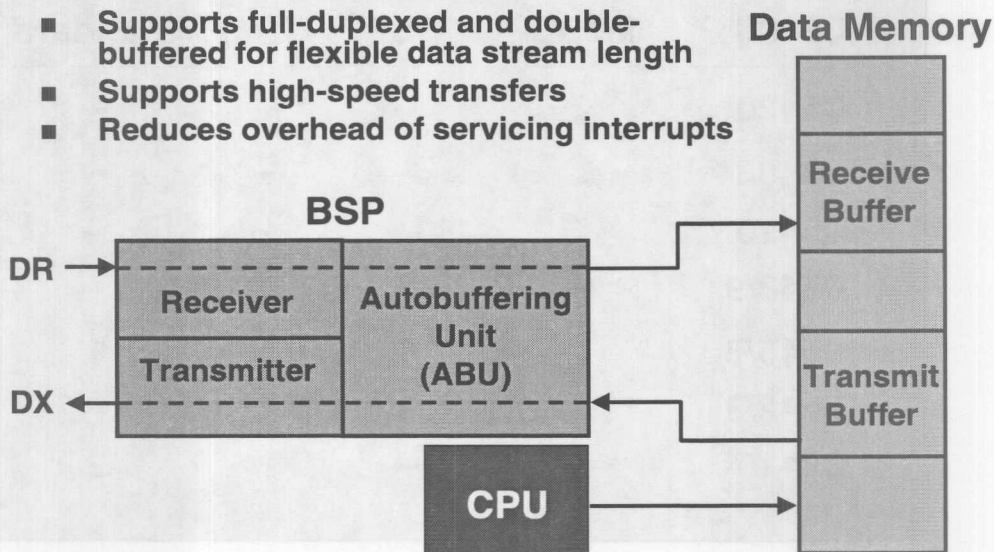
THE WORLD LEADER IN DSP SOLUTIONS





Buffered Serial Port: Autobuffering

- Clocks at full CLKOUT rate
- Supports full-duplexed and double-buffered for flexible data stream length
- Supports high-speed transfers
- Reduces overhead of servicing interrupts

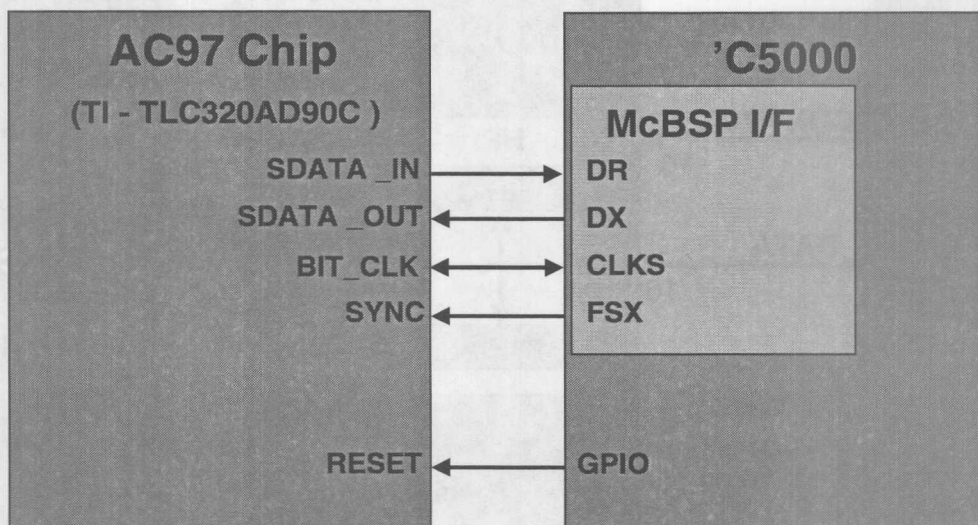


39

THE WORLD LEADER IN DSP SOLUTIONS



McBSP: Glueless I/F with AC97



40

THE WORLD LEADER IN DSP SOLUTIONS



41

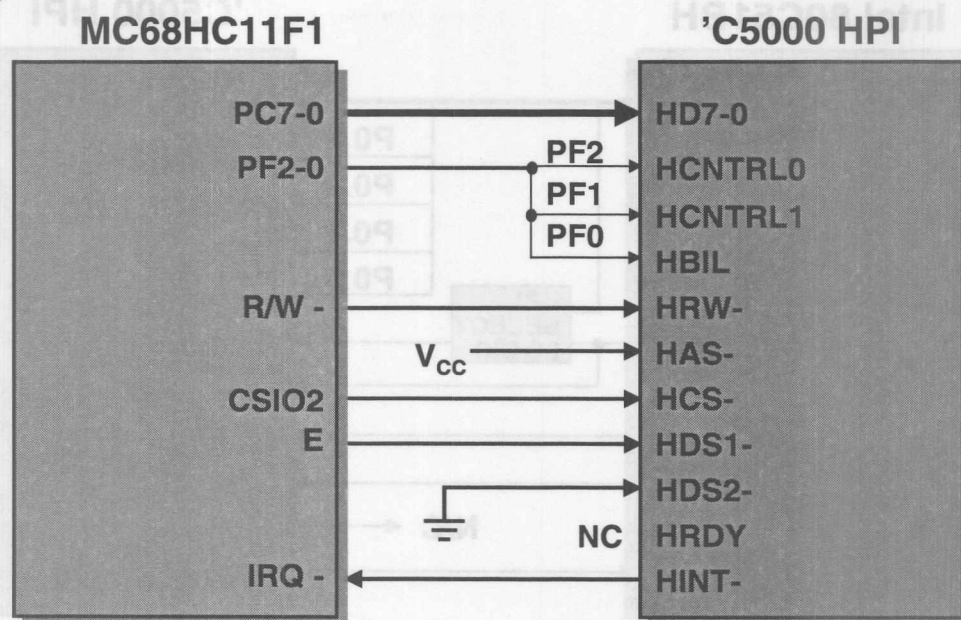
TEXAS
INSTRUMENTS



TEXAS
INSTRUMENTS



Motorola 68HC11F1 to 'C5000 HPI

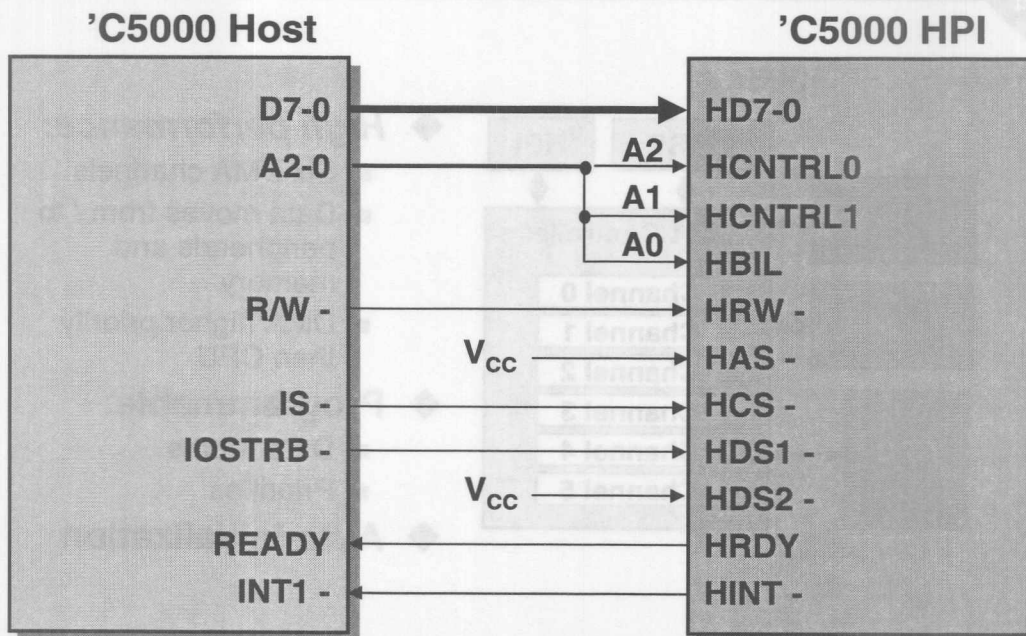


43

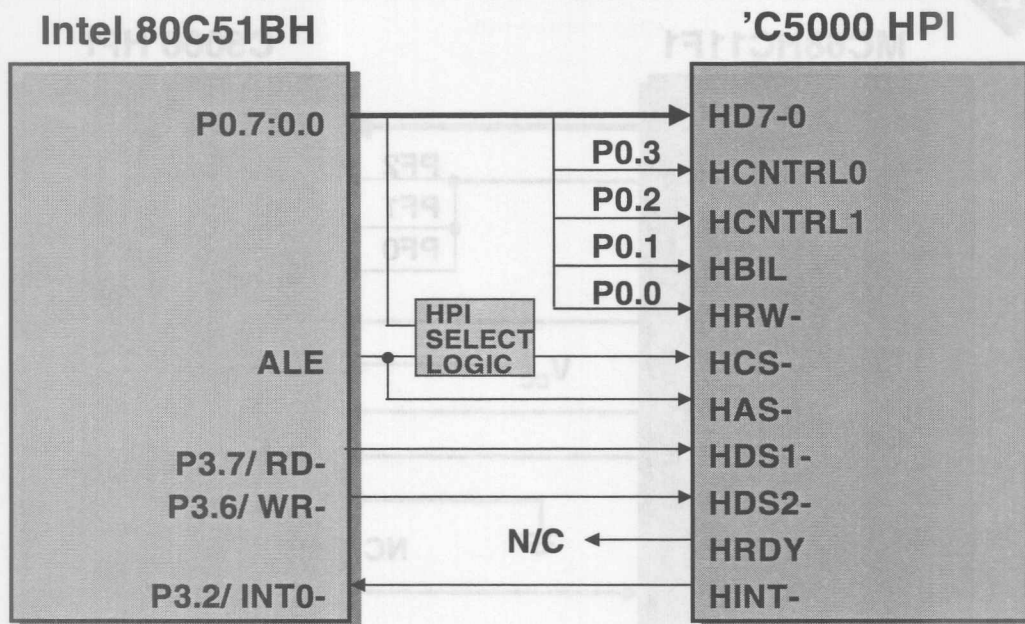
THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

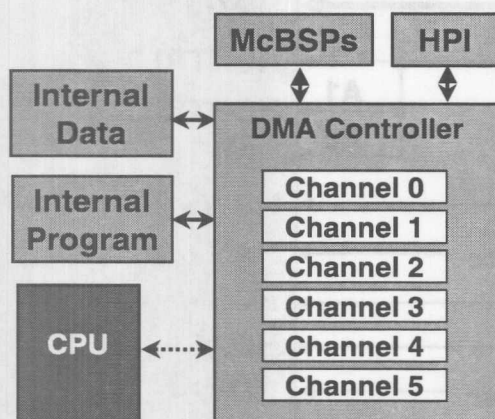
'C54x-Host-to-'C54x HPI



Intel 80C51 to 'C5000 HPI



DMA: Transfers transparent to CPU



◆ High performance:

- Six DMA channels
- Data moves from / to peripherals and memory
- DMA higher priority than CPU

◆ Programmable:

- Data widths
- Priorities

◆ Auto-initialization

44

THE WORLD LEADER IN DSP SOLUTIONS





'C5000: Peripherals

'C5000	RAM/ROM	HPI	DMA	Serial Port
'C5420	200 K / --	16-bit	12-ch	6 McBSP
'C5402	16 K / 4 K	8-bit	6-ch	2 McBSP
'C5410	64 K / 16 K	8-bit	6-ch	3 McBSP
'C548/9	32 K / 16 K	8-bit	--	2 BSP/ 1 TDM
'C545/6	6 K / 48 K	8-bit	--	1 BSP/ 1 Std
'C542/3	10K / 2 K	8-bit	--	1 BSP/ 1 TDM
'C541	5 K / 28 K	8-bit	--	2 Std

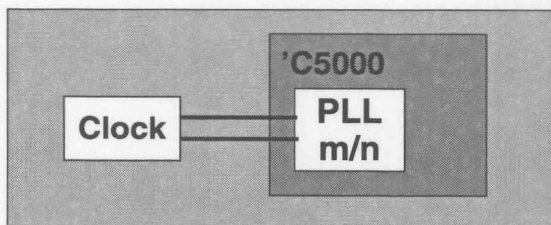
45

THE WORLD LEADER IN DSP SOLUTIONS



Interfacing: PLL clock

- Instruction rate clock can be derived from slower external clock.
- 'C548 and above are programmable on the fly (32 ratios possible; no device reset required)
- PLL clock reduces EMI issues by lowering board-level clock rate.
- Lower cost/frequency oscillator (crystal) are multiplied internally.
- Device supports programmable delay for PLL lock time.



46

THE WORLD LEADER IN DSP SOLUTIONS



For a list of related application reports, white papers, and Designer Notebook Pages, see the Appendix.



How do I work with TI's 'C5000?

How do I get my performance?

What performance can I expect?

How do I interface easily?

What are the new 'C5000 devices?

How do I minimize power consumption?

How does TI enable power-efficient performance at lower cost?

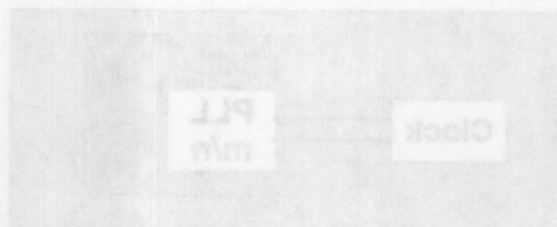
47

THE WORLD LEADER IN DSP SOLUTIONS



Interfacing: PLL clock

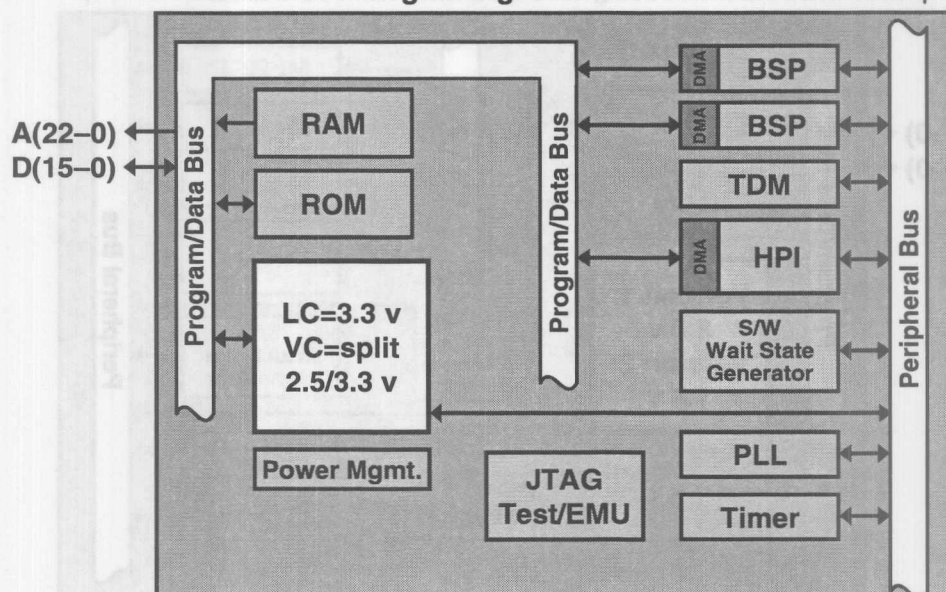
- Instruction rate clock can be derived from slower external clock.
- 'C548 and above are programmable on the fly (32 ratios possible; no device reset required)
- PLL clock reduces EMI issues by lowering board-level clock rate.
- Lower cost frequency oscillator (crystal) are multiplied internally.
- Device supports programmable delay for PLL lock time.





'C549: 100 MIPS in production

TMS320C549 Digital Signal Processor: 100 MHz at .25 μ



48

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

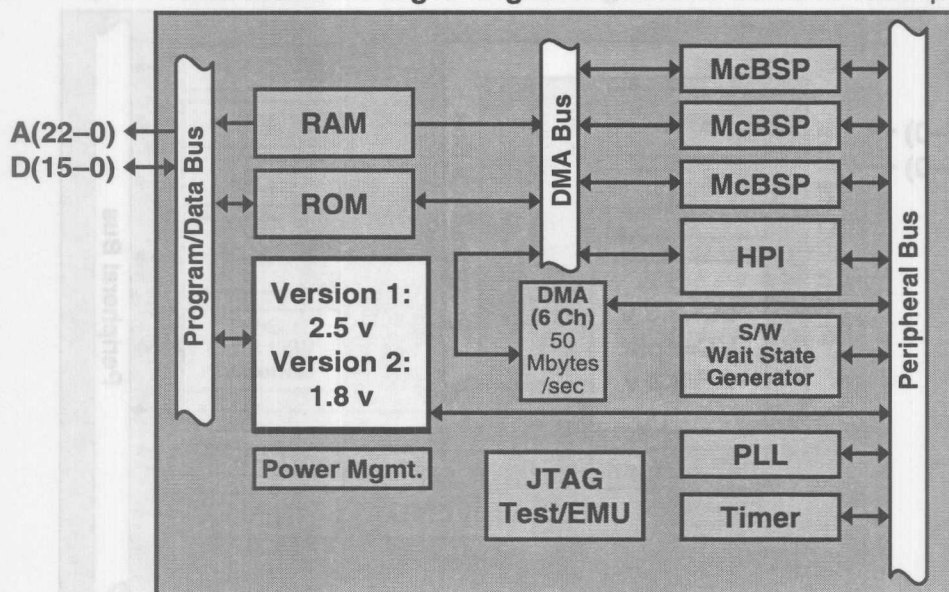
TMS320C549

- 90–113 mW typical internal active power
- 32 K words on-chip SRAM
- 8 Kx16-bit DA
- 24 Kx16-bit SA



'C5410: Increasing on-chip integration

TMS320C5410 Digital Signal Processor: 100 MHz at .25μ



49

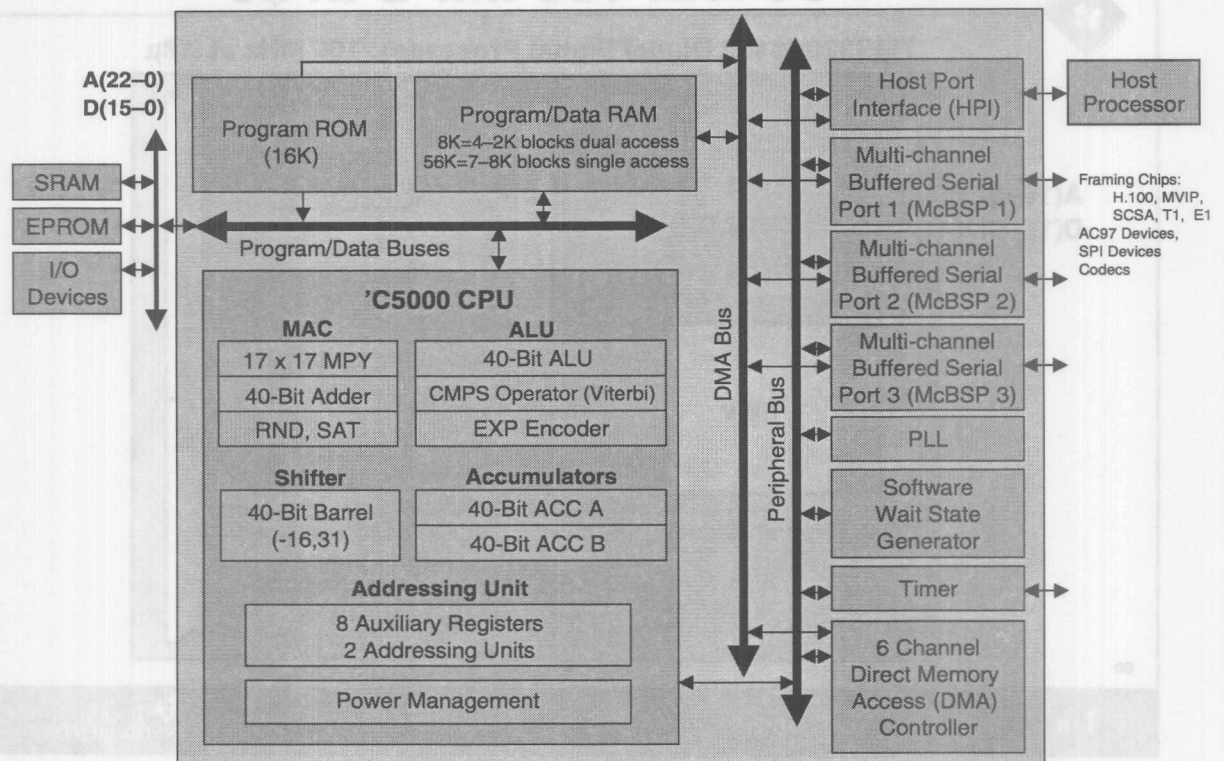
THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

TMS320C5410

- 113 mW typical internal active power
- 64 K words on-chip SRAM
 - 8 Kx16-bit DA
 - 56 Kx16-bit SA
- 3 McBSPs
- 6-channel DMA interfacing with Host Port and McBSPs
- 144-pin TQFP or
- Size of a dime
176 μ*BGA

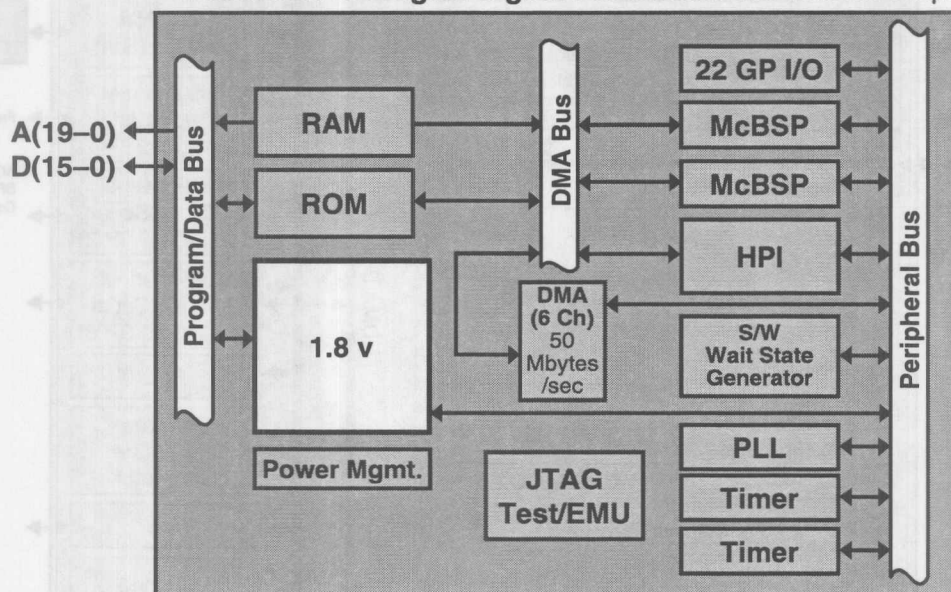
TMS320C5410 Detailed Block Diagram





'C5402: 100 MIPS at \$5

TMS320C5402 Digital Signal Processor: 100 MHz at .18 μ



50

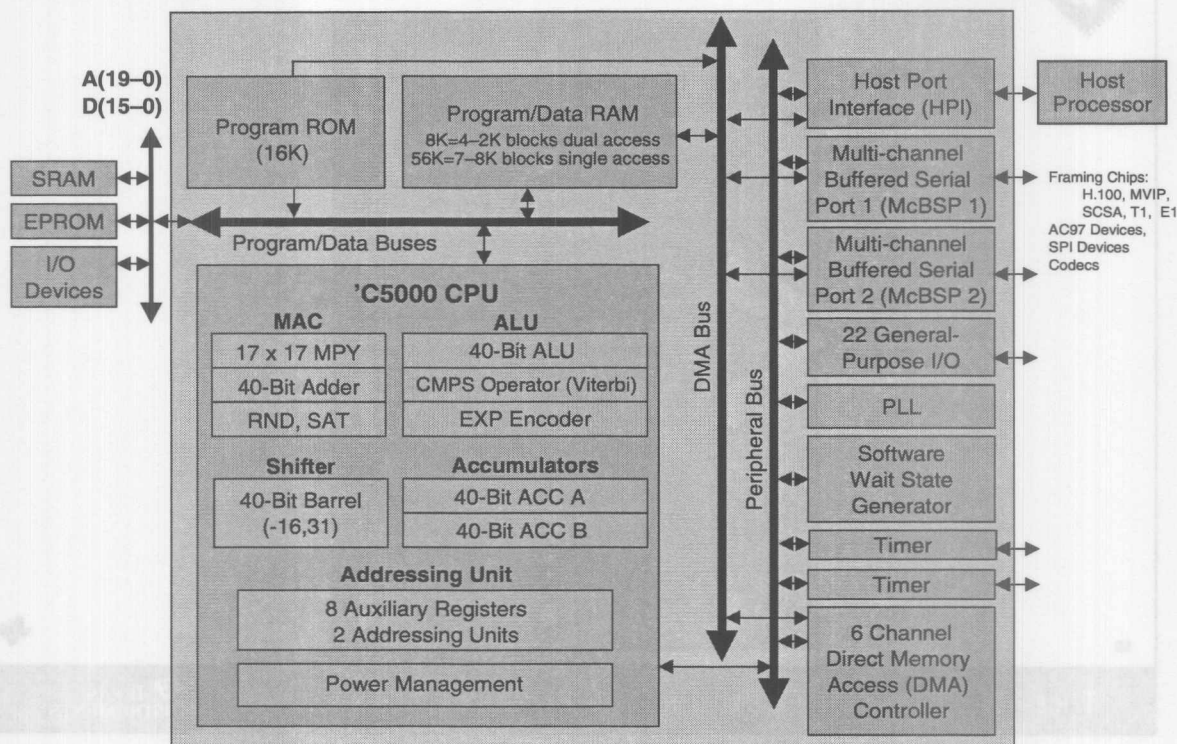
THE WORLD LEADER IN DSP SOLUTIONS



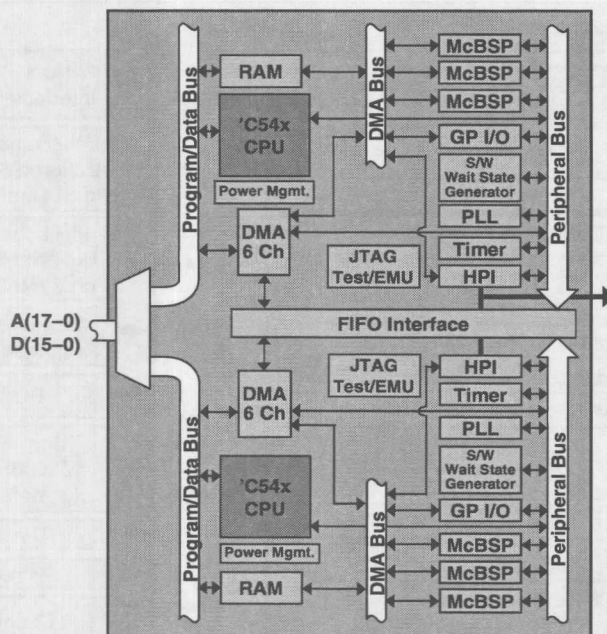
TMS320C5402

- <60 mW typical internal active power
- Significant integration / \$5
- 16 K words on-chip SRAM
- 2 McBSPs
- 6-channel DMA interfacing with Host Port and McBSPs
- 144-pin TQFP or
- Size of a dime
- 144 μ *BGA

TMS320C5402 Detailed Block Diagram



'C5420: Dual core 200 MIPS



52

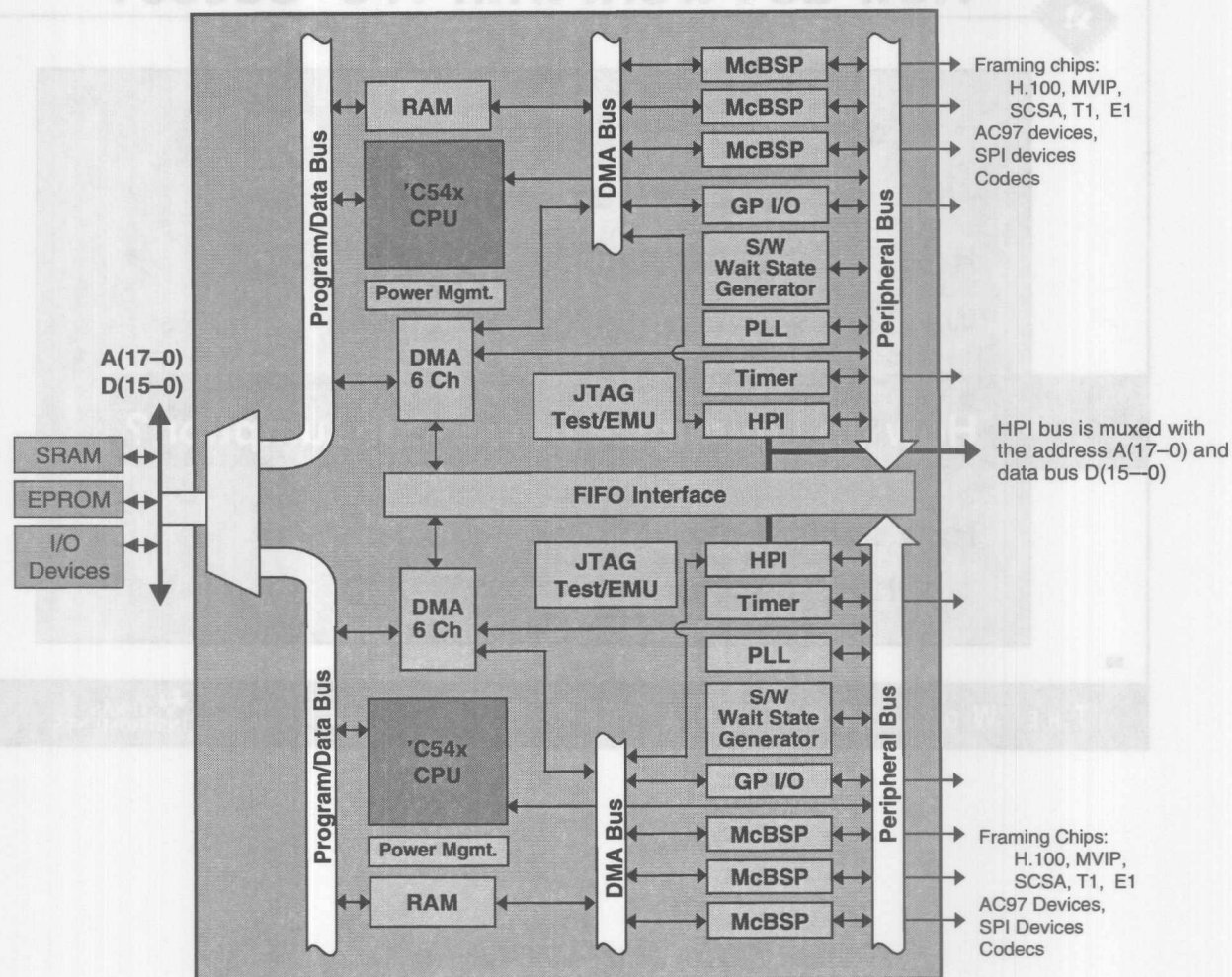
THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

TMS320C5420

- Two cores joined by FIFO I/F and HPI
- 200 K words on-chip SRAM (3.2 Mbits)
- 6 McBSPs
- 12-channel DMA interfacing with 16-bit HPI and McBSPs
- 144-pin TQFP or
- Size of a dime
144 μ BGA

TMS320C5420 Detailed Block Diagram



For a list of related application reports, white papers, and Designer Notebook Pages, see the Appendix.



How do I work with TI's 'C5000?

How do I get my performance?

What performance can I expect?

How do I interface easily?

What are the new 'C5000 devices?

How do I minimize power consumption?

How does TI enable power-efficient
performance at lower cost?

53

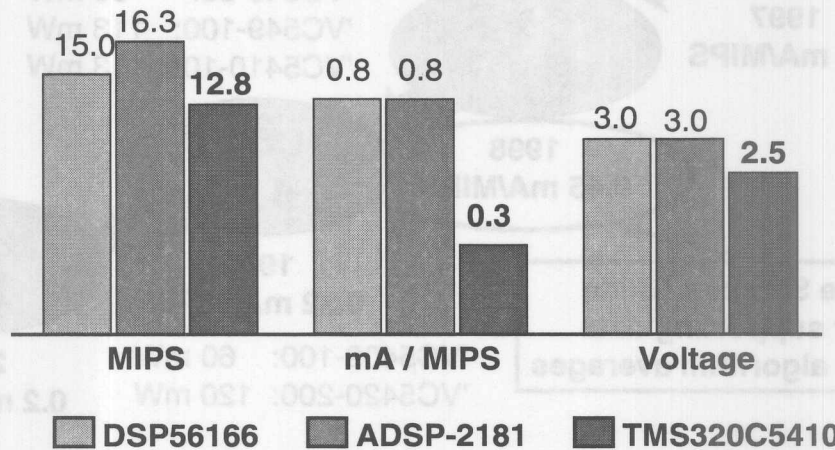
THE WORLD LEADER IN DSP SOLUTIONS





'C5000: mW per IS-54 VSELP

True measure of power consumption is:
 $(\text{MIPS/algorithm}) \times (\text{mA / MIPS}) \times (\text{V}) = \text{mW / function}$



54

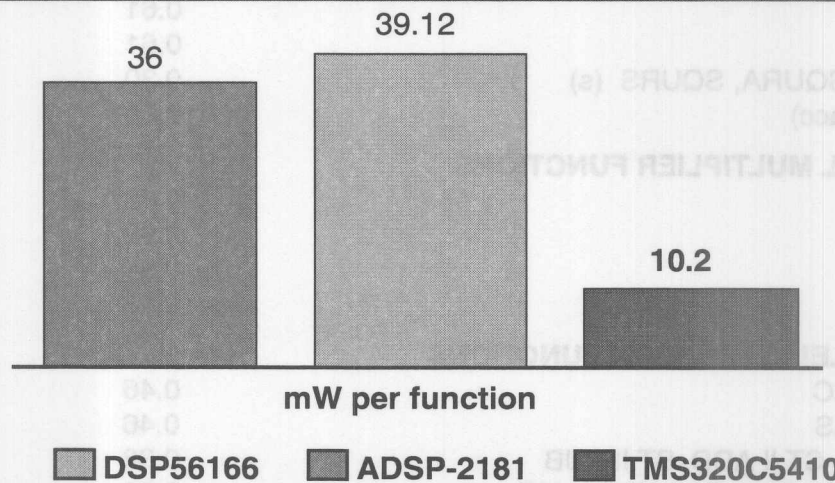
THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



'C5000: mW per IS-54 VSELP

True measure of power consumption is:
 $(\text{MIPS/algorithm}) \times (\text{mA / MIPS}) \times (\text{V}) = \text{mW / function}$



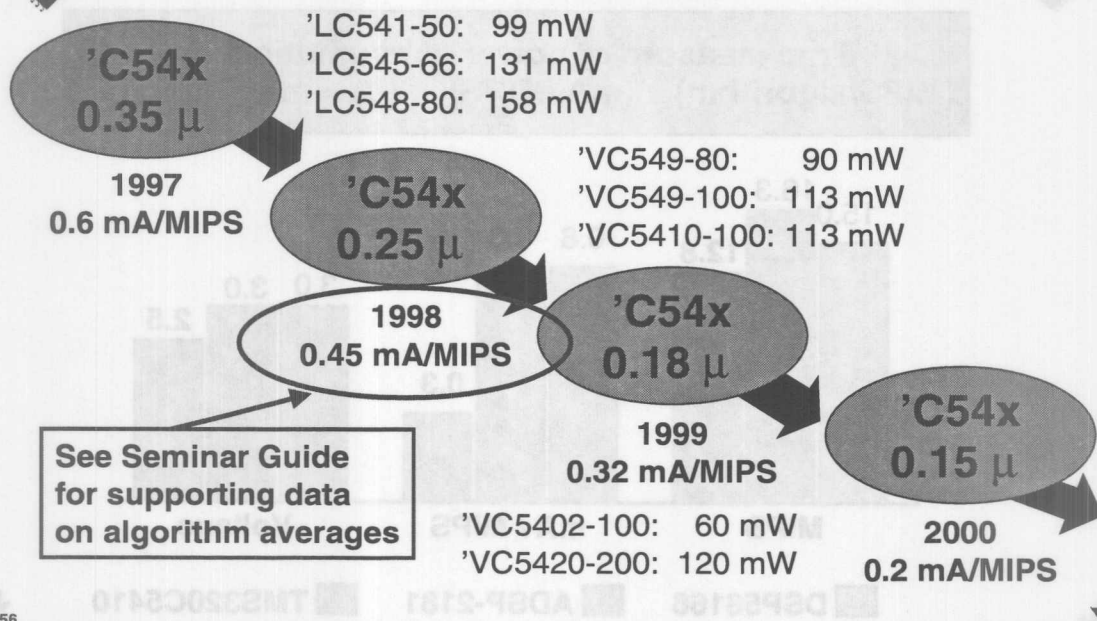
55

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



'C5000: Process technology



56

THE WORLD LEADER IN DSP SOLUTIONS



TMS320C5000 Power Analysis Table

Instruction

Power Consumption @ 2.5 V (mA)

MULTIPLIER FUNCTIONS

MAC[R], MACA, MAS, MPY, MPYA, MPYU (s)	0.38
MAC[R], MACSU, MAS, MPY (xy)	0.46
MAC[R], MPY (lk)	0.30
MAC[R], MPY (s, lk)	0.30
MACD	0.61
MACP	0.61
SQUR, SQURA, SQURS (s)	0.30
SQUR (acc)	0.30

SPECIAL MULTIPLIER FUNCTIONS

SQDST	0.36
FIRS	0.68
LMS	0.53
POLY	0.68

PARALLEL OPERATION FUNCTIONS

LD MAC	0.46
LD MAS	0.46
ST LD, ST ADD, ST SUB	0.38
ST MPY, ST MAC, ST MAS	0.38

DOUBLE-PRECISION FUNCTIONS

DLD, DADD, DADST, DSADT, DRSUB, DSUB, DSUBT	0.38
---------------------------------------------	------

0.45 mA/MIPS average for 2.5 V



'C5000: Lowest power consumption

Mechanisms used on the 'C5000:

- ◆ **Bus keepers / Holders**
maintain state of external bus
- ◆ **External Bus off control**
disables the external bus
- ◆ **Static design**
lower clock to DC
- ◆ **IDLE 1, 2, 3 modes**
drop into various power-down modes
- ◆ **PLL options**
use lower system clock
- ◆ **MIPS efficiency**
requiring fewer MIPS

57

THE WORLD LEADER IN DSP SOLUTIONS



'C5000: Idle pin options

IDLE n	n =	1	2	3
Effect :				
CPU Halted		x	x	x
Peripherals Halted			x	x
Clock Suspended				x
Resume on:				
Reset		x	x	x
External Interrupt		x	x	x
Internal Interrupt		x		

Register	Field	Function, if set to 1	on RS
PMST	CLKOFF	CLKOUT pin inactive	0
BSCR	EXIO	External Interface Off	0
BSCR	BH	Hold previous value on Bus	0

'C5000: Mixed-mode power supplies

- For greater speed and lower power, new DSPs are designed to run at 3.3 volts and/or 2.5 volts.
- However, most systems are based on a 5-volt bus, requiring the addition of regulators
- Designers need low voltage regulators that:
 - Have 3.3-V or 2.5-V outputs
 - Provide enough current for the DSP core and I/O
 - Operate with very little headroom from the supply (a minimum input to output differential)
- These TI voltage regulators are recommended:

TPS7133	3.3V	500mA
TPS7233	3.3V	250mA
TPS71025	2.5V	500mA

For a list of related application reports, white papers, and Designer Notebook Pages, see the Appendix.



How do I work with TI's 'C5000?

How do I get my performance?

What performance can I expect?

How do I interface easily?

What are the new 'C5000 devices?

How do I minimize power consumption?

How does TI enable power-efficient performance at lower cost?

58

THE WORLD LEADER IN DSP SOLUTIONS

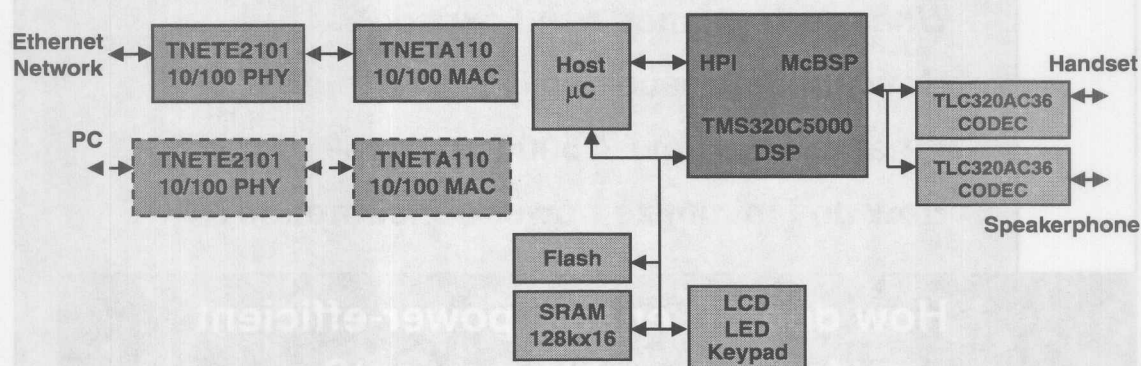


Internet Phone Example - Part Numbers

Description	Manufacturer	Part Number	Approx. 1KU Price	Function
PHY	Texas Instruments	TNETA101A28		Physical interface
MAC	Texas Instruments	TNETE110A19		Receive voice packet
DSP	Texas Instruments	TMS320C50A157.50		Voice buffer management between SRAM and CODEC, sampling and decimating E-net packets, polling MD, DTMF, call setup, call answer, caller ID, call progress plus phone functions.
SRAM	IDT	Varied		128K x 16, 12 ns, pip-stream and data buffer for packetizing voice data.
CODEC	Texas Instruments	TLCS20A036A25.50		Handset
CODEC	Texas Instruments	TLCS20A036A25.50		Speakerphone
Host	Varied	Varied		Communications



Value per \$: Internet phone example



59

THE WORLD LEADER IN DSP SOLUTIONS



Internet Phone Example – Part Numbers

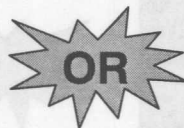
Description	Manufacturer	Part Number/Approx 1KU Price	Function
PHY	Texas Instruments	TNETA2101/\$8	Physical interface
MAC	Texas Instruments	TNETE110/\$19	Receive voice packet
DSP	Texas Instruments	TMS320C54x/\$7.50	Voice buffer management between SRAM and CODEC, assembling and dismantling E-Net packets, polling I/O, DTMF, call setup, call answer, caller ID, call progress plus phone functions.
SRAM	IDT	Varied/\$10	128k x 16, 12 ns, program and data buffer for packetizing voice data.
CODEC	Texas Instruments	TLC320AC36/\$2.50	Handset
CODEC	Texas Instruments	TLC320AC36/\$2.50	Speakerphone
Host	Varied	Varied/\$10–\$15	Control/communications



'C5402: Internet phone example

100 MIPS @\$5.00*

'C5402



50 MIPS @\$10.00**

ADI 2186

G.723.1 Vocoder
Echo Cancellation
DTMF
Voice Activity Detection
Full Duplex Speakerphone
Voice Packet Management

TOTAL 40 MIPS

60

* 25 KU pricing.

**Source: Minimum pricing on www.ednmag.com



THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

IP Phone DSP Software Requirements

Algorithm	MIPS	Program Memory (Words)	Data Memory (Words)
G.723.1 Vocoder	17	18K	4K
G.165	4.2	12K	1.2K
DTMF	4	3K	3.5K
Voice Activity Detection	0.3	0.8K	0.4K
Full-Duplex Speakerphone	10	3K	1.5K
Voice Packet Management	3	6K	1K
TOTAL	38.5	42.8K	11.6K



'C5402: Internet phone example

100 MIPS @\$5.00*

50 MIPS @\$10.00**

'C5402



ADI 2186

Plus... at half the cost, 'C5402 delivers:

- ◆ Lower power, less space
- ◆ Glueless I/F to μ C/Host, to multiple CODECs, and to fast or slow SRAM and Flash
- ◆ Expandable system for product differentiation, increased application functionality and seamless upgrades

61

* 25 KU pricing. **Source: Minimum pricing on www.ednmag.com



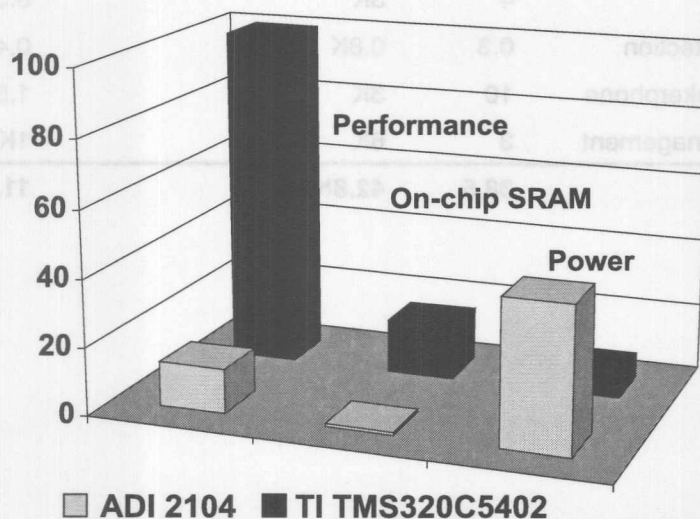
THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



Competitor: What do you get for \$5?

1/7th the performance, 1/20th on-chip SRAM,
6x the power consumption



62

Source: Analog Devices data sheet and web site

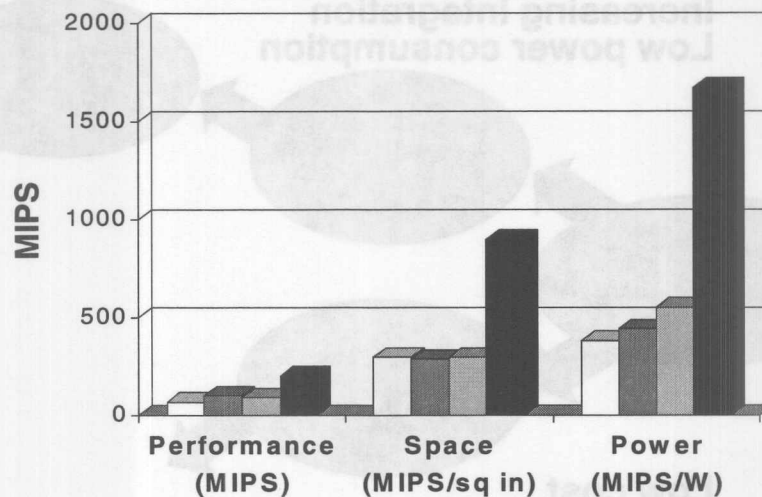
THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS



'C5420: More MIPS per careabout

Up to 3x performance per Watt
and 3x performance per square inch



Based on application of
BDTmark to competitor data
sheets, press releases, and
web sites.

63

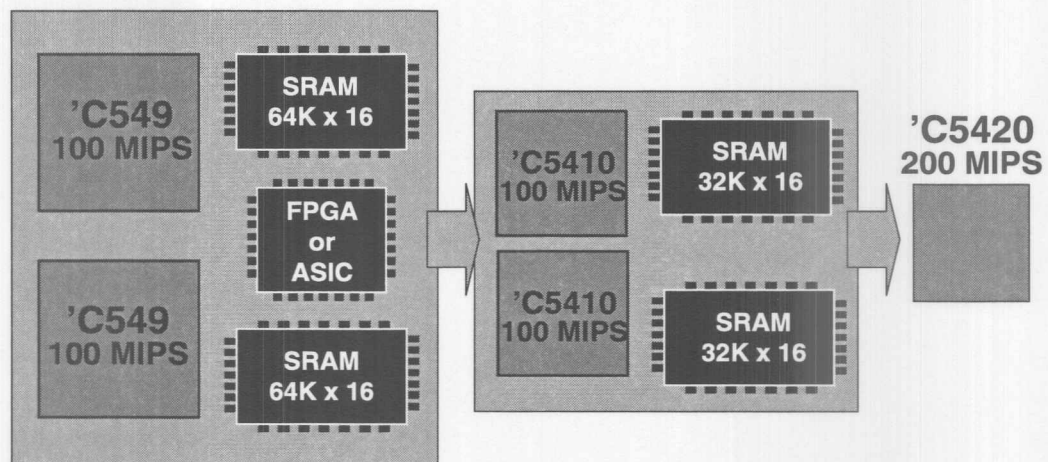
□ ADI2189L ■ Mot 56307 ■ Lu 1620 ■ TITMS320C5420

THE WORLD LEADER IN DSP SOLUTIONS



'C5420: Decreasing system costs

...through board space reduction



64

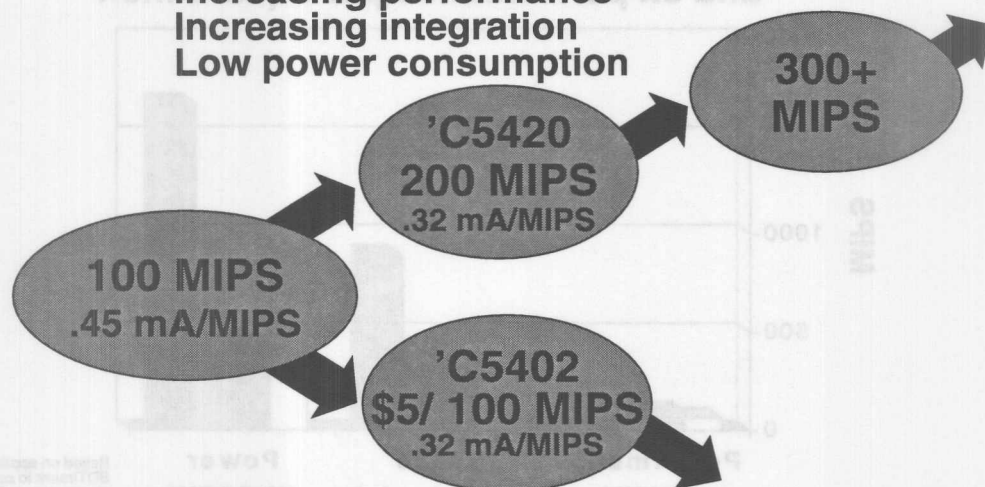
THE WORLD LEADER IN DSP SOLUTIONS





'C5000: Future directions

Increasing performance
Increasing integration
Low power consumption



Low cost
Power-efficient performance

65

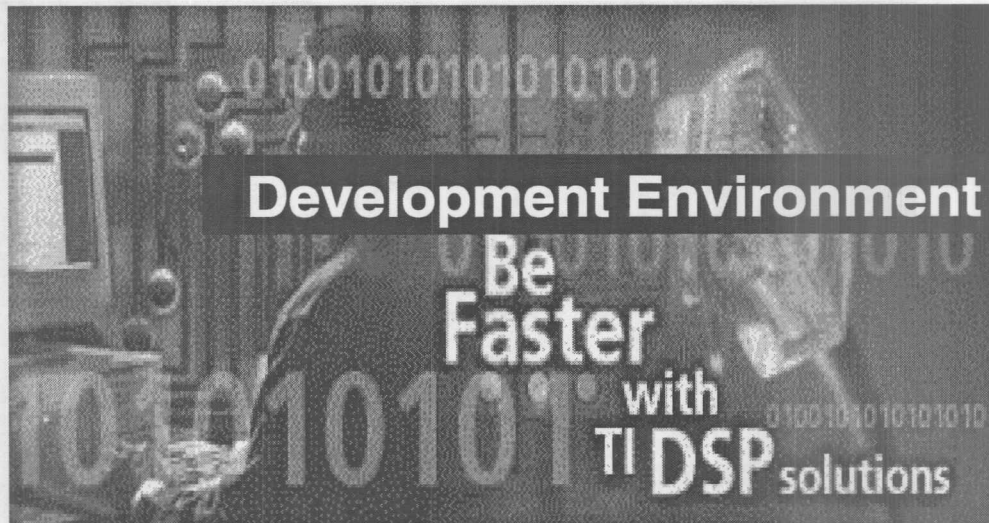
THE WORLD LEADER IN DSP SOLUTIONS

TEXAS
INSTRUMENTS

For a list of related application reports, white papers, and Designer Notebook Pages, see the Appendix.



How do tools make it easier?



1

THE WORLD LEADER IN DSP SOLUTIONS



Today's Agenda

- ✓ What are my system requirements?
- ✓ How do I work with TI's 'C6000?
- ✓ How do I work with TI's 'C5000?
- ✓ How do TI's tools make my development easier?

What support can I count on?

2

THE WORLD LEADER IN DSP SOLUTIONS





How do tools make it easier?

What is the development cycle?

What happens when I run the code?

What does real-time analysis bring?

How does DSP/BIOS help me?

What tools are available?

3

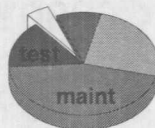
THE WORLD LEADER IN DSP SOLUTIONS



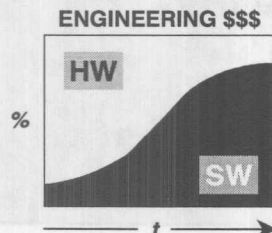
Barriers: Impact TTM, product quality

Software roadblocks

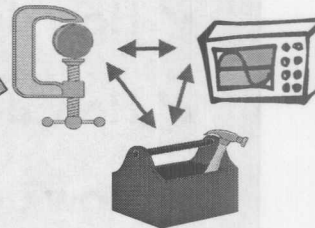
Rising life-cycle costs



Increasing complexity



Tool integration



Minimal re-use



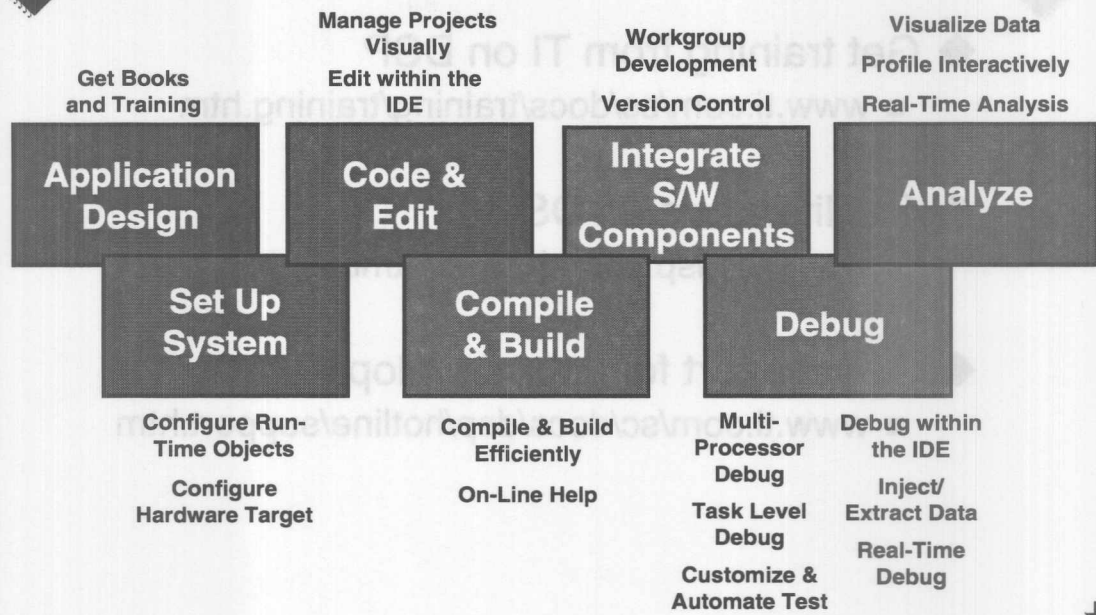
4

THE WORLD LEADER IN DSP SOLUTIONS





The Steps: Development cycle



5

THE WORLD LEADER IN DSP SOLUTIONS



Introduction: The elements

- ◆ **Code Composer** is an Integrated Development Environment (IDE) similar to MS Visual C++ and built specifically for DSP
- ◆ **DSP/BIOS** is a library of scheduling, instrumentation, and communications functions that provides real-time analysis and RTDX™ (Real-Time Data Exchange)
- ◆ **Hardware Emulation and Evaluation tools** allow code debug on actual silicon and low-cost analysis of performance in early stages of development cycle
- ◆ **Code Composer Studio** (1Q99) provides an extensible tool plug-in and seamless integration between the host and target DSP tools

6

THE WORLD LEADER IN DSP SOLUTIONS





Application Design: First step

- ◆ Get training from TI on DSP
 - www.ti.com/sc/docs/training/training.htm
- ◆ Get literature on DSP
 - www.go-dsp.com/dspinfo/html/dspinfo.htm
- ◆ Get support for your development
 - www.ti.com/sc/docs/dsp/hotline/support.htm

7

THE WORLD LEADER IN DSP SOLUTIONS



Set up System: Configuration tool

Configuration Tool - [C:\bios5x\work\audio\audio.cdb]

File Edit Object View Tools Help

Project Manager

- Global Settings
- CLK - Clock Manager
 - PRD_clock
- HST - Host Channel Manager
- HWI - Hardware Interrupt Service Routine Manager
- IDL - Idle Function Manager
 - HST_dataPump
 - IDL_cpuLoad
- LOG - Event Log Manager
 - LOG_system
 - trace
- MEM - Memory Section Manager
- PIP - Buffered Pipe Manager
 - DSS_rxPipe
 - DSS_txPipe
- PRD - Periodic Function Manager
- SIG - Signal Manager
 - PRD_signal
 - audioSig
- STS - Statistics Object Manager

CLK - Clock Manager properties

Property	Value
Object Memory	EDATA
Enable CLK Manager	True
Use high resolution time for internal timings	False
Microseconds/Int	1000
Directly configure on-chip timer registers	True
Fix TDDR	False
TDDR Register	0
PRD Register	19999
Instructions/Int	20000

Static Configuration for maximum efficiency
Visual edit of system resources
Objects are statically configured and bound to the executable program

- Early error detection
- Automatic data and stack size estimation

Minimizes target memory footprint
Only the necessary parts of the kernel and objects are built into the target program

Optimizing internal data

Estimated Data Size: 688 Estimated Minimum Stack Size: 103

8

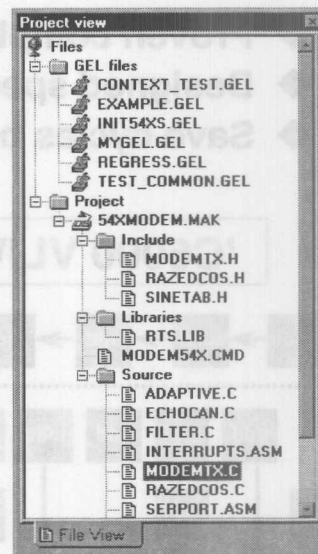
THE WORLD LEADER IN DSP SOLUTIONS





Code & Edit: Manage projects visually

- ◆ Intuitive organization
 - Drag & drop
 - Fast access
 - Easy file manipulation
- ◆ Graphically configure build options
 - Saved with each project



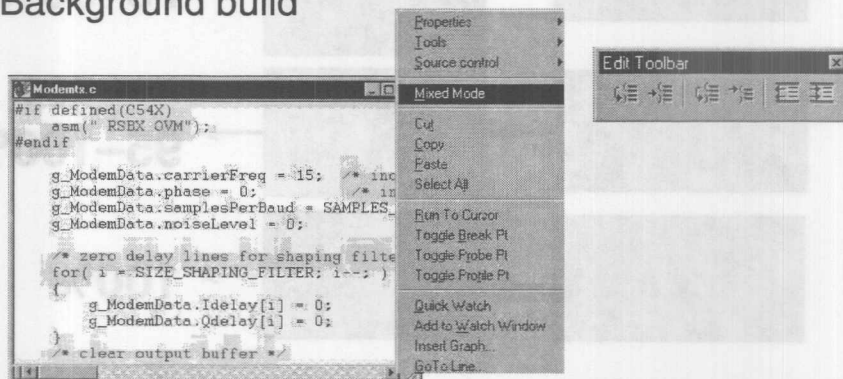
9

THE WORLD LEADER IN DSP SOLUTIONS



Code & Edit: ... within the IDE

- ◆ Editor integrated in IDE, like MS Visual C++
 - Familiar environment reduces learning curve
 - DSP tuned
 - Syntax highlighting for C and assembly
 - Background build



10

THE WORLD LEADER IN DSP SOLUTIONS

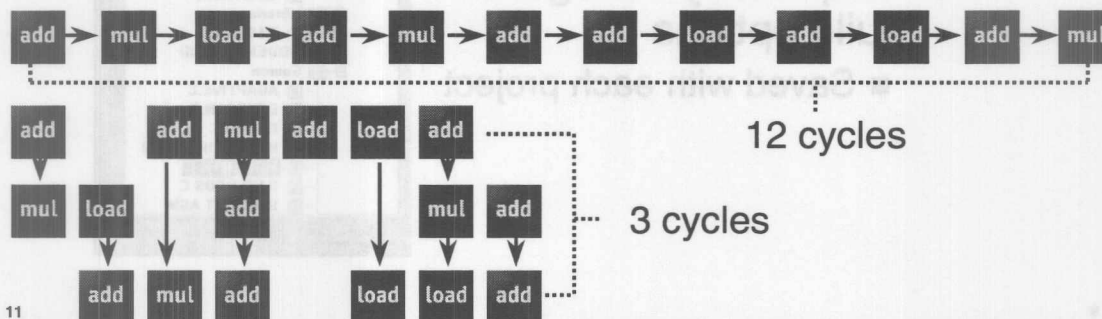




Compile & Build: Advanced compiler

- ◆ Proven compiler and optimizer
- ◆ Designed specifically for DSP
- ◆ Save cycles by working in parallel

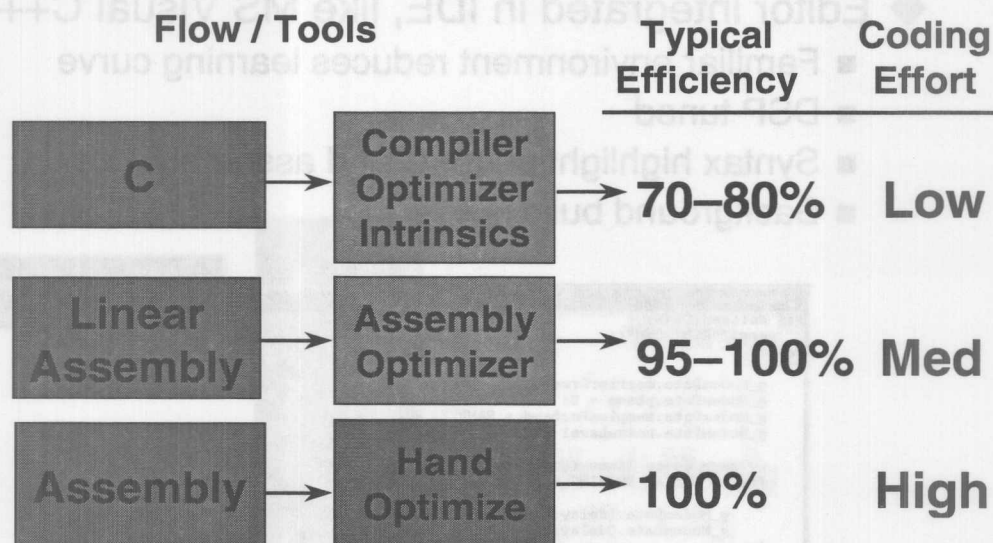
'C6000 VLIW Architecture



THE WORLD LEADER IN DSP SOLUTIONS



Compile & Build: Efficient build tools



12

THE WORLD LEADER IN DSP SOLUTIONS



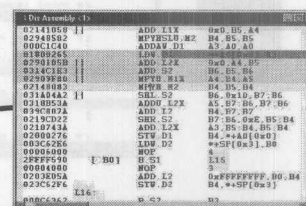
- | F54x Code Composer Help | |
|--------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| File Edit Bookmark Window Help | |
| Contents | Index |
| LDU | Load Unsigned Memory Value |
| Syntax | LDU SrcImm, dst |
| Operands | SrcImm: Single data-memory operand
dst: A (accumulator A)
B (accumulator B) |
| Opcode | 0001 0010 IAAA AAAA |
| Execution | (SrcImm) → d15-0
00 0000 → d2 (35-16) |
| Status Bits | None |
| Description | <p>The LDU instruction loads the data-memory value into the low part of the destination accumulator (bits 15-0).</p> <p>The guard bits and the high part of the accumulator (bits 31-16) are cleared to 0. Data is then treated as an unsigned 16-bit number. There is no sign extension, regardless of the status of the S0M bit.</p> |
| Words | 1 word |

13



TEXAS
INSTRUMENTS

- ```
Build Window
C:\> cd %~dp0 -> asfsc\COMPUSER\CACEM\ROBERT.C
[modext.c]
The Intel C Compiler Version 1.68
Copyright (c) 1994-1997 Texas Instruments Incorporated
**= SineLookup
**+= CosineLookup
**-= Modulation
***= ShapeFilter
**/= ModeTransmitter
**%= Initialize
**< ReadDataFile
**> ReadConstellations
**<< AdjustBaseSignal
**>> main
**>>> line 212: [F801] syntax error at or near
Build Complete.
Errors: 0 Warnings: 0
```



14



TEXAS  
INSTRUMENTS



## Debug: within the IDE

### ■ Debugging is optimized for DSP

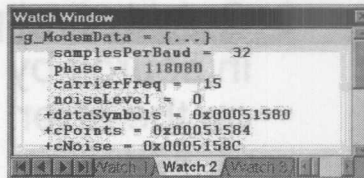
- ◆ Advanced breakpoints
- ◆ C expression based conditional breakpoints
- ◆ View source and dis-assembly simultaneously

### ■ C and Assembly debugging

### ■ Advanced Watch Window

### ■ Multi-processor debug

- ◆ Global breakpoints
- ◆ Synchronized control over groups



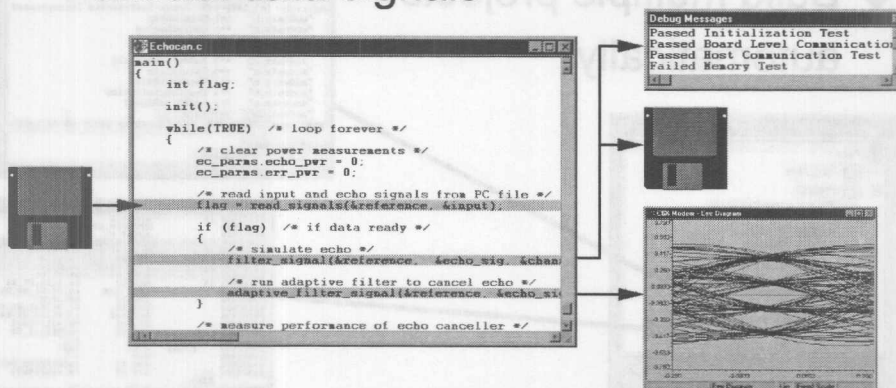
15

THE WORLD LEADER IN DSP SOLUTIONS



## Debug: Inject/extract data signals

- ◆ Probe Points provide oscilloscope-like functions
- ◆ File I/O with advanced triggering to inject or extract data signals



16

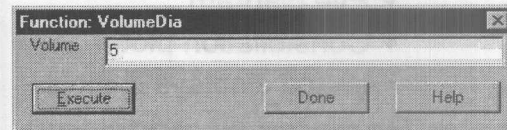
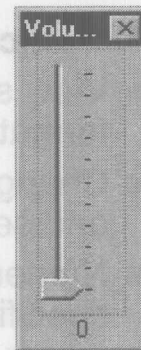
THE WORLD LEADER IN DSP SOLUTIONS





## Debug: Customize & automate testing

- ◆ GEL C-based scripting language
  - Easy to learn
  - Controls the target DSP application
  - Supports numerous built-in high level functions
- ◆ Customize the GUI
  - Add menu items
  - Create dialogs
- ◆ Automate testing
  - Automate repetitive functions
  - Regression test control



17

THE WORLD LEADER IN DSP SOLUTIONS



## Analyze: Profile interactively

- ◆ Use Profile Points
  - Measure performance
  - Identify hotspots
  - Optimize code
  - Gather profile information on one part of the code while debugging another

| Profile Statistics |     |       |         |        |         |         |  |
|--------------------|-----|-------|---------|--------|---------|---------|--|
| Location           |     | Count | Average | Total  | Maximum | Minimum |  |
| MODEMTX.C line     | 342 | 13    | 34824.7 | 452721 | 34827   | 34817   |  |
| MODEMTX.C line     | 338 | 14    | 45.0    | 630    | 45      | 45      |  |
| MODEMTX.C line     | 335 | 14    | 1032.6  | 14456  | 14456   | 0       |  |

18

THE WORLD LEADER IN DSP SOLUTIONS

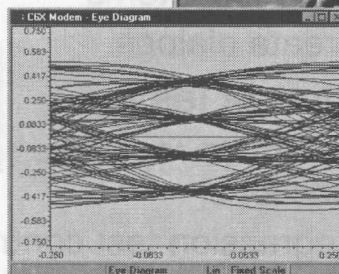
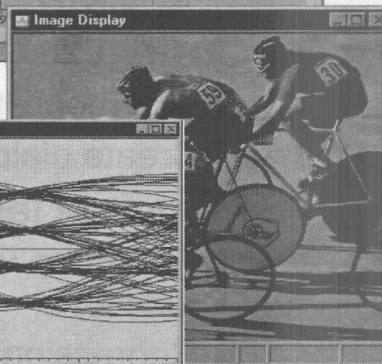
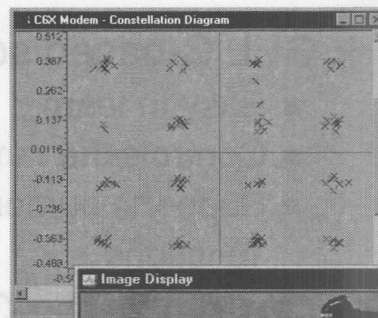




## Analyze: Visualize data

### Graphical Signal Analysis:

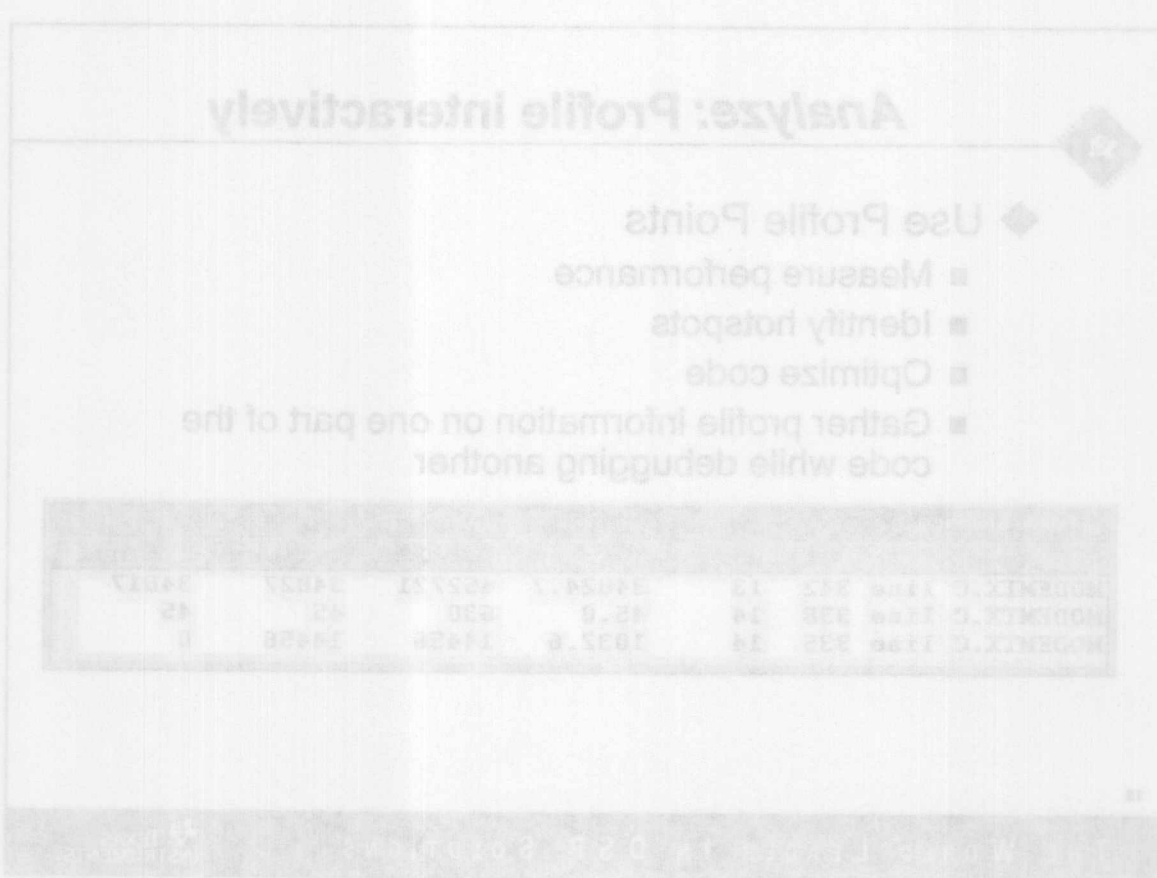
- View signals in native format
- Change variables on the fly and see their effects
- Numerous application-specific graphical plots
  - ◆ FFT waterfall
  - ◆ Eye diagram
  - ◆ Constellation plot
  - ◆ Image displays & more
- Requires no additional code



19

THE WORLD LEADER IN DSP SOLUTIONS

TEXAS  
INSTRUMENTS





## How do tools make it easier?

What is the development cycle?

**What happens when I run the code?**

What does real-time analysis bring?

How does DSP/BIOS help me?

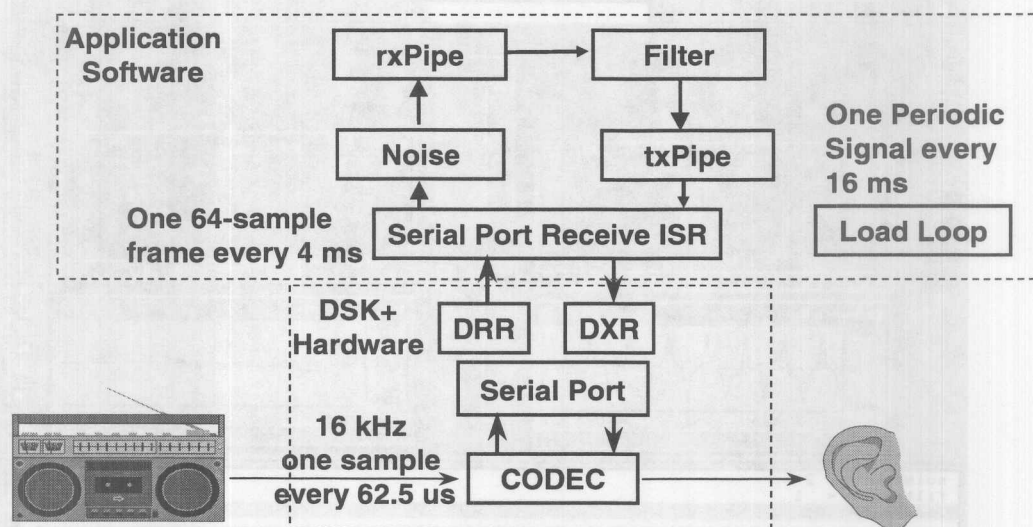
What tools are available?

20

THE WORLD LEADER IN DSP SOLUTIONS



## Audio Demo: Block diagram



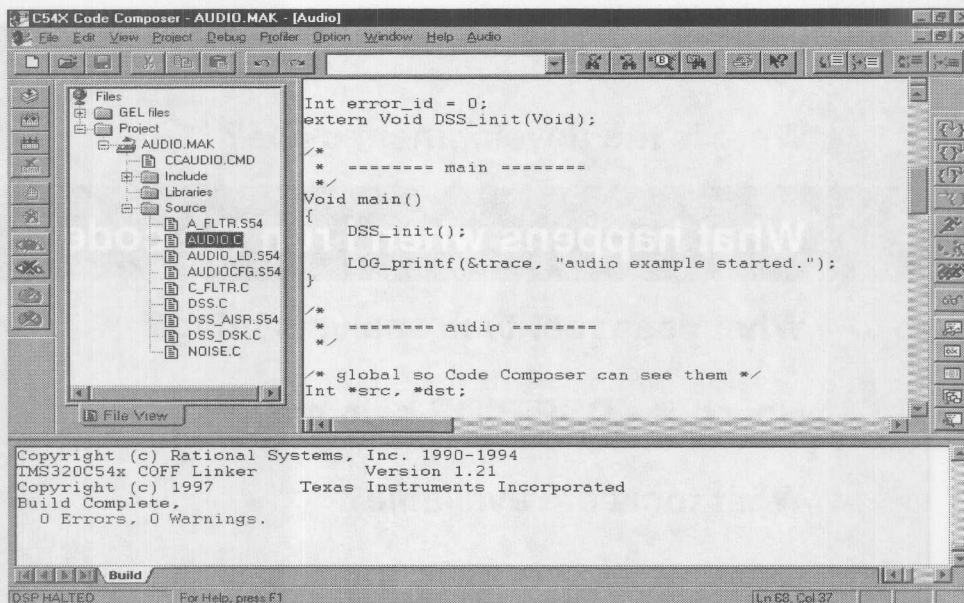
21

THE WORLD LEADER IN DSP SOLUTIONS





## Thread: Edit and build a thread

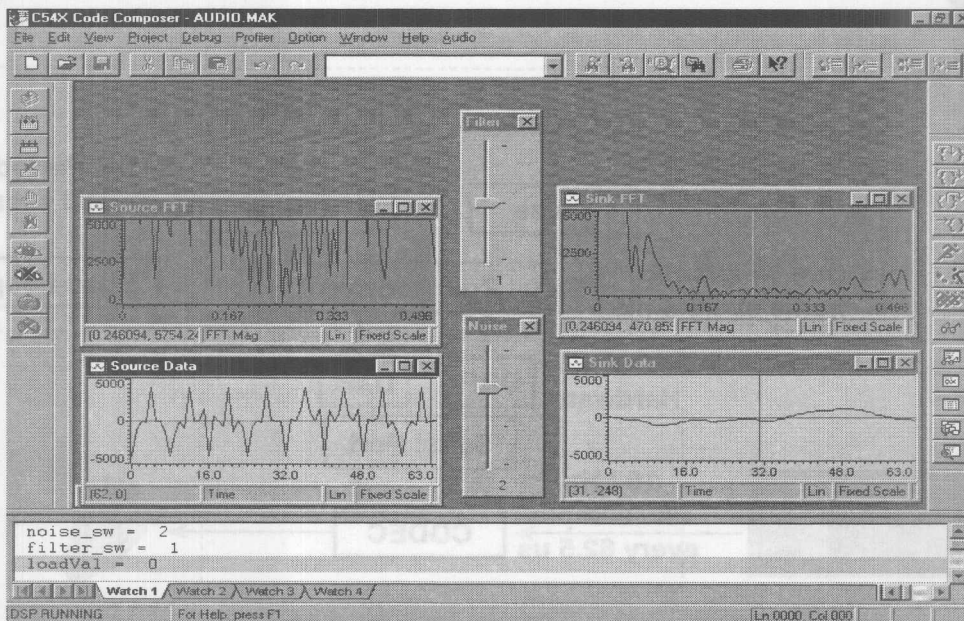


22

THE WORLD LEADER IN DSP SOLUTIONS



## Audio Debug: via Code Composer



23

THE WORLD LEADER IN DSP SOLUTIONS





## How do tools make it easier?

What is the development cycle?

What happens when I run the code?

**What does real-time analysis bring?**

How does DSP/BIOS help me?

What tools are available?

24

THE WORLD LEADER IN DSP SOLUTIONS



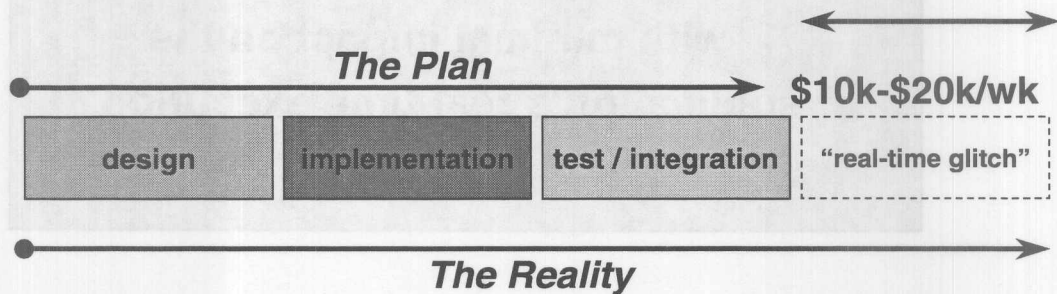
## Visualize: See the problem; then fix it

### TOOLS

PROGRAM  
GENERATION

PROGRAM  
DEBUGGER

VISUAL  
ANALYSIS



25

THE WORLD LEADER IN DSP SOLUTIONS





## ***Real-time Analysis: During execution***

- ◆ Analysis of data in real-time during execution of system software
  - A software logic analyzer
- ◆ Useful in software development by providing:
  - Real-time performance analysis information
  - Metrics for measuring performance and optimizations
  - Insight into the real-time behavior of our design
- ◆ Must be low overhead to be of real value

26

THE WORLD LEADER IN DSP SOLUTIONS



## ***Real-time Analysis: Impact?***

**How is real-time analysis implemented  
with minimal impact on the  
application's real-time execution?**

27

THE WORLD LEADER IN DSP SOLUTIONS





## Real-time Analysis: Keys

- ◆ User defined and embedded instrumentation
  - User defined and controlled instrumentation
    - ◆ Conditional instrumentation
    - ◆ Control mechanism (on/off) to the instrumentation
  - Imbedded fundamental instrumentation in system
    - ◆ Lead to less interference in execution
    - ◆ Deterministic and optimized
- ◆ Pass data to the host automatically as a background (idle) thread
- ◆ Use a real-time interface between the host and target
  - RTDX, JTAG

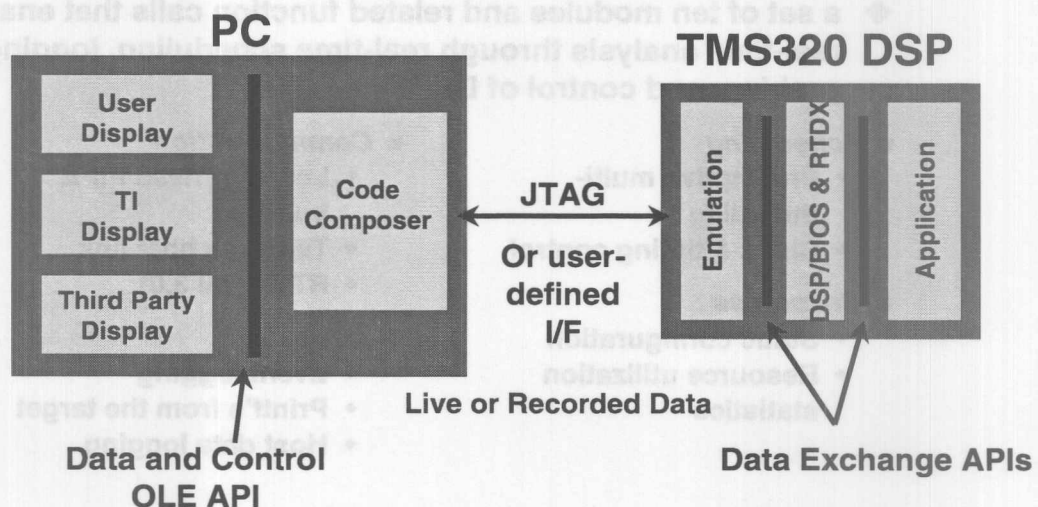
28

THE WORLD LEADER IN DSP SOLUTIONS



## RTDX: Real-time data transfer

### Host Communications



29

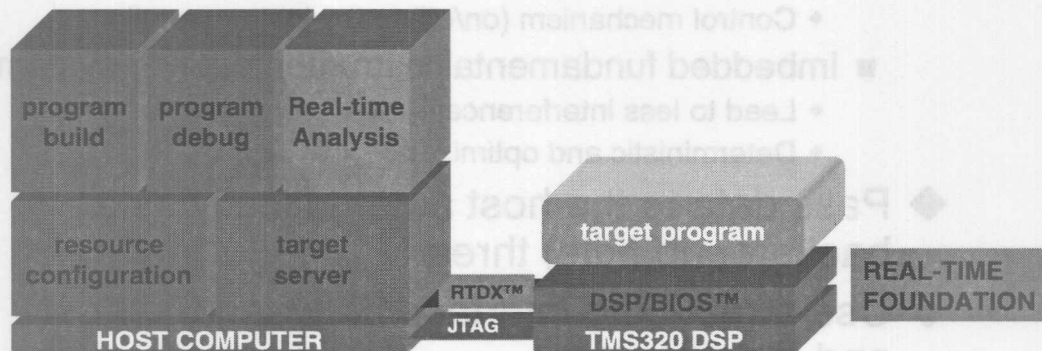
THE WORLD LEADER IN DSP SOLUTIONS





## Concept: Real-time analysis

Host real-time analysis enabled by target intrinsic instrumentation and communications functions



30

THE WORLD LEADER IN DSP SOLUTIONS



## DSP/BIOS: Real-time analysis library

**DSP/BIOS is simply...**

- ◆ a set of ten modules and related function calls that enable real-time analysis through real-time scheduling, logging, probing, and control of DSP threads.

- **Scheduling**

- ◆ Preemptive multi-threading
- ◆ Clock & timing control

- **Resources**

- ◆ Static configuration
- ◆ Resource utilization statistics

- **Communication**

- ◆ Low overhead PIPE buffers
- ◆ Target to host link
- ◆ RTDX (rel 3.0)

- **Analysis**

- ◆ Event logging
- ◆ Printf's from the target
- ◆ Host data logging

31

THE WORLD LEADER IN DSP SOLUTIONS

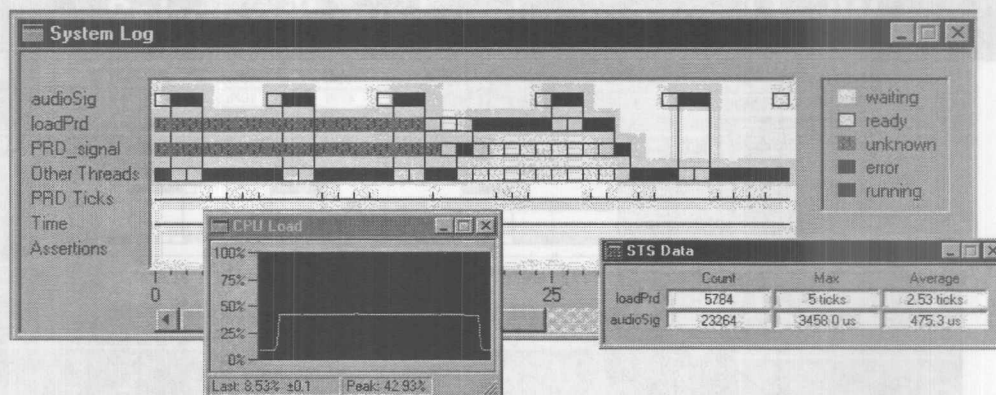




## DSP/BIOS: Visual real-time analysis

Implicit diagnostics DSP/BIOS performs *automatically*:

- ◆ Monitor CPU load percentage
- ◆ Monitor worst-case task execution time
- ◆ Provide “software logic analyzer” display of task execution

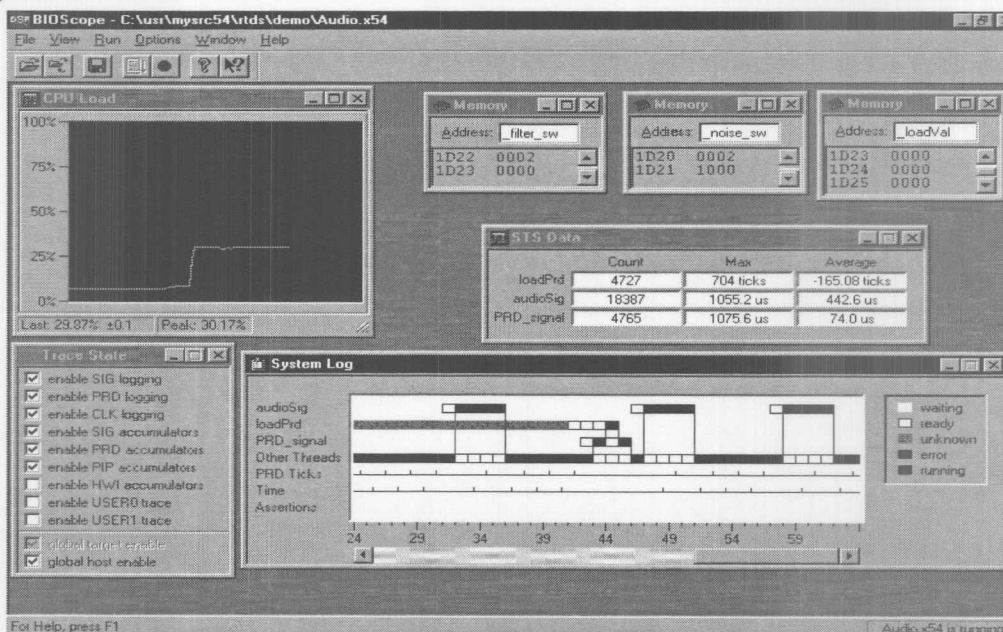


32

THE WORLD LEADER IN DSP SOLUTIONS



## Analysis Tool: BIOScope

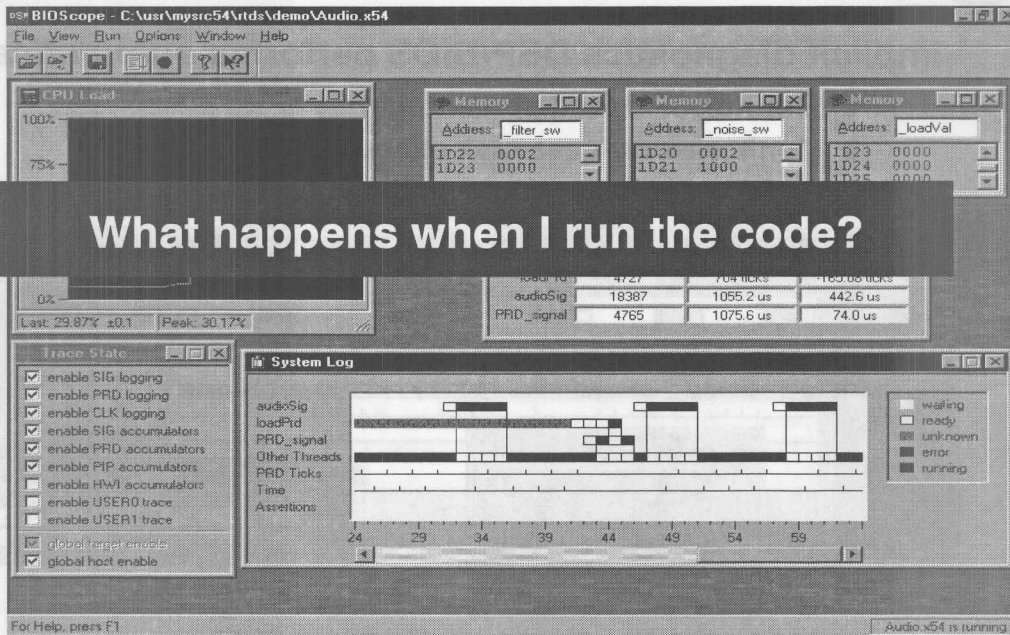


33

THE WORLD LEADER IN DSP SOLUTIONS



## Demo: Audio demo #2



What happens when I run the code?

THE WORLD LEADER IN DSP SOLUTIONS





## How do tools make it easier?

What is the development cycle?

What happens when I run the code?

What does real-time analysis bring?

**How does DSP/BIOS help me?**

What tools are available?

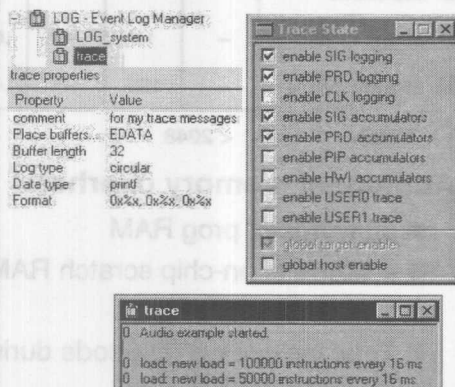
35

THE WORLD LEADER IN DSP SOLUTIONS

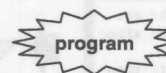


## DSP/BIOS: Event logging

- configurable log buffers
- host or target control
- < 1µs per event logged on 80-MHz 'C54x
- output console display

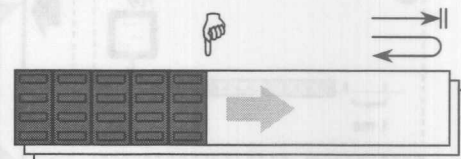


36



TRC\_enable, TRC\_disable  
LOG\_write, LOG\_printf

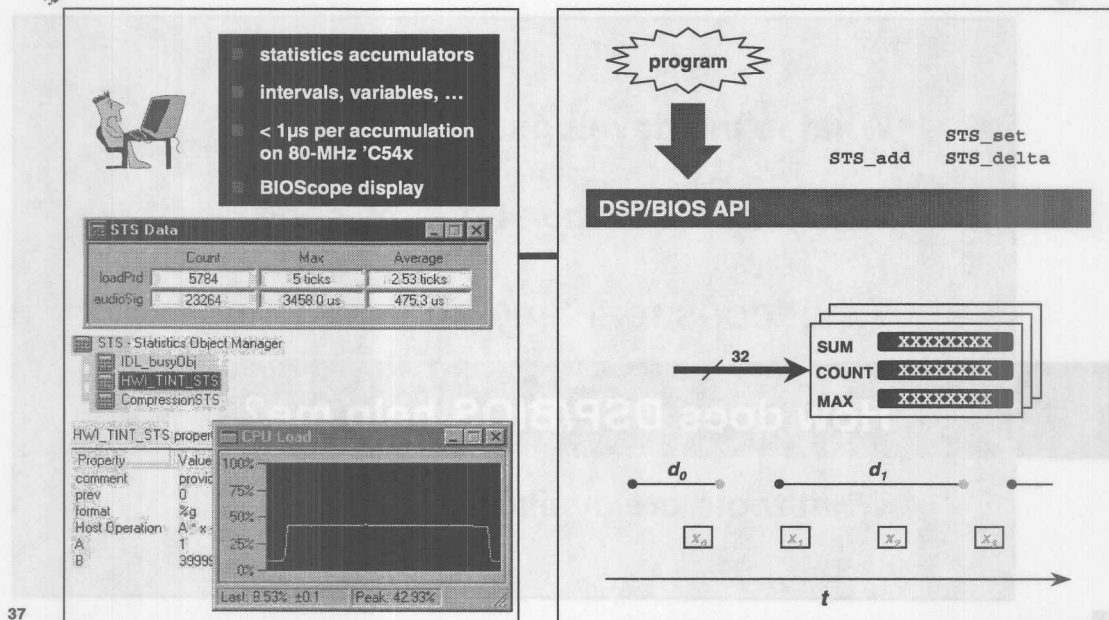
**DSP/BIOS API**



THE WORLD LEADER IN DSP SOLUTIONS



## DSP/BIOS: Resource utilization

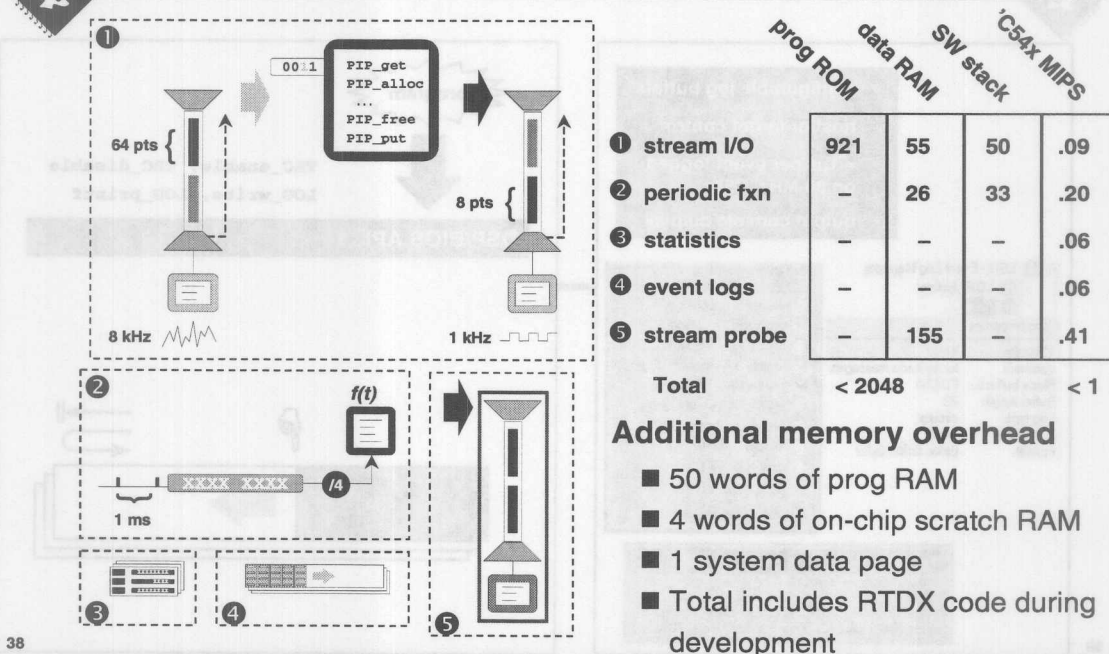


37

THE WORLD LEADER IN DSP SOLUTIONS



## Example: System performance



38

THE WORLD LEADER IN DSP SOLUTIONS





## Summary: Code Composer, DSP/BIOS

### ◆ Code Composer

- DSP industry's first IDE
- Easy to use
- Unique features: probe points, data visualization, GEL
- Thousands of customers worldwide

### ◆ DSP/BIOS

- Real-time analysis
- RTDX (Real-Time Data Exchange)
- Make parametric changes to system while running
- Low overhead instrumentation or real-time tasks

39



THE WORLD LEADER IN DSP SOLUTIONS

TEXAS  
INSTRUMENTS

## Availability: Hardware tools

### ◆ Evaluation Module (EVM)

- Device evaluation, benchmarking & system debug

■ 8K x 32 SRAM

■ 2M x 32 SDRAM

### ◆ Multi-channel telephony apps

- 18-bit stereo codec, mic,

input/output audio jacks

### ◆ Code Composer, Code Gen

tools, drivers & sample apps

On sale for a limited time: only \$295!



## How do tools make it easier?

What is the development cycle?

What happens when I run the code?

What does real-time analysis bring?

How does DSP/BIOS help me?

**What tools are available?**

40

THE WORLD LEADER IN DSP SOLUTIONS



## Availability: Hardware tools

### ◆ Evaluation Module (EVM)

- Device evaluation, benchmarking & system debug
- 64K x 32 SBSRAM
- 2M x 32 SDRAM

### ◆ Multi-channel telephony apps

- 16-bit stereo codec, mic, in/out audio jacks

### ◆ Code Composer\*, Code Gen tools, drivers & sample apps



**On sale for a limited time: only \$995!**

41

THE WORLD LEADER IN DSP SOLUTIONS





## **Availability: XDS510 Emulator**

### ◆ **XDS510 Emulator**

- Scan based using JTAG serial interface
- Global run/stop/breakpoint of parallel processing DSP
- Software breakpoint trace on all program and data addresses
- Single step execution
- Performance analysis

42

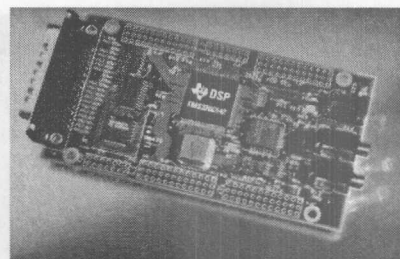
THE WORLD LEADER IN DSP SOLUTIONS



## **Availability: Other tools**

### ◆ **'C54x DSKPlus**

- DSP Starter Kit
- Code Explorer debugger
- PC assembly language tools
- **Start now for only \$149!**



### ◆ **Instruction Set Architecture Simulator**

- Use instruction set simulator to jump-start your application when hardware is scarce or not yet available
- Develop software & hardware simultaneously

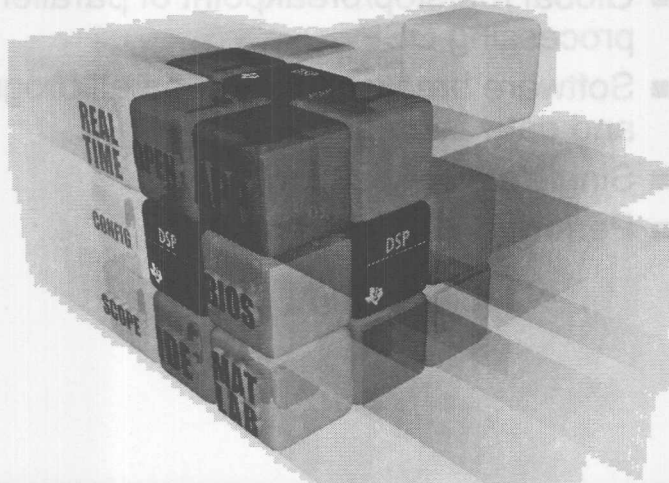
43

THE WORLD LEADER IN DSP SOLUTIONS





# CODE Composer studio

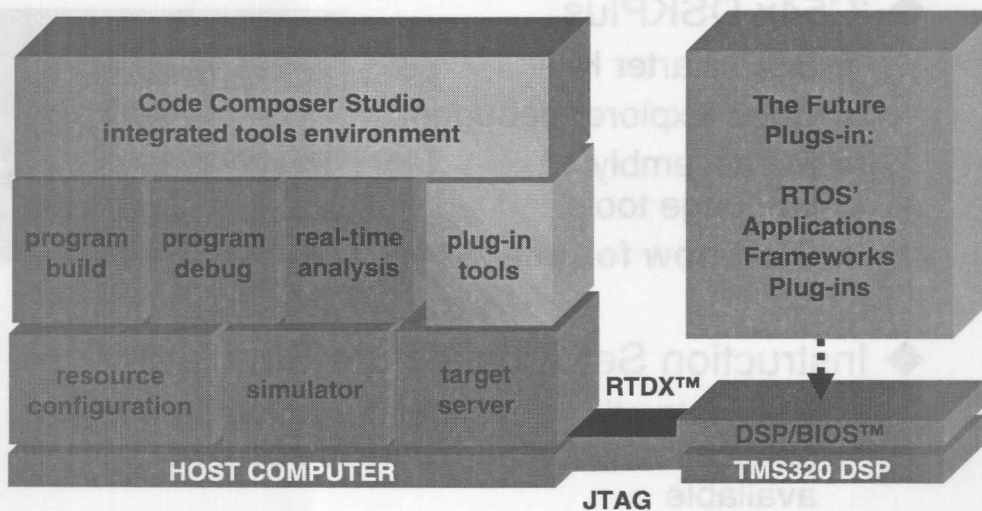


44

THE WORLD LEADER IN DSP SOLUTIONS



## New: Code Composer Studio



45

THE WORLD LEADER IN DSP SOLUTIONS





## Features: Code Composer Studio

- ◆ Integrates IDE, DSP/BIOS, RTDX and Code Gen tools together

- ◆ Open plug-in architecture for third-party host and target tools

- ◆ 'C6000 in 1Q99

- ◆ 'C5000 in 2Q99



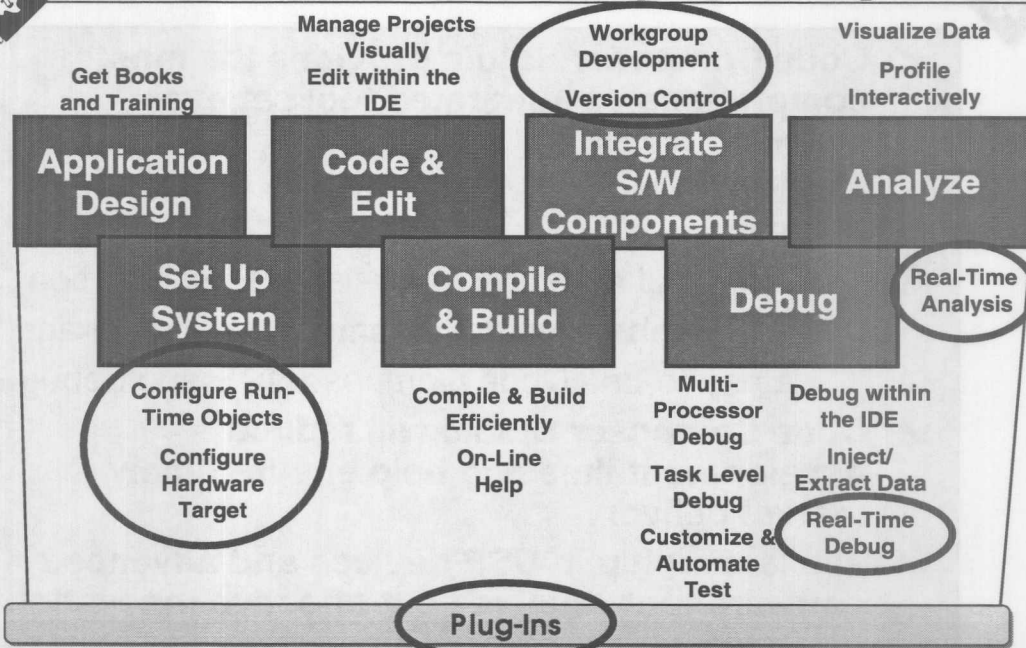
- Real-time analysis & debugging
- Real-time data visualization
- Visual configuration of run-time facilities
- Multi-target functionality
- Workgroup development
- A truly visual environment

46

THE WORLD LEADER IN DSP SOLUTIONS



## The Steps: Development cycle



47

THE WORLD LEADER IN DSP SOLUTIONS





## Plug-ins

- ◆ Leverage DSP's largest third-party network tools to reduce development time
- ◆ Mix & match host/target plug-ins to facilitate each phase of the code development cycle
- ◆ Seamlessly extend and customize your own environment
- ◆ Focus your innovation on creating new applications
- ◆ For a current list of third-party plug-in partners
  - [www.ti.com/sc/docs/dsp/develop/3party.htm](http://www.ti.com/sc/docs/dsp/develop/3party.htm)

48

THE WORLD LEADER IN DSP SOLUTIONS



## Summary: Cost-effective innovation

- ✓ **Code Composer Studio provides the most comprehensive integrated tool set ever provided for DSP:**
  - Extensible system with third-party plug-in tools
  - Powerful real-time analysis and visualization
  - Comprehensive development cycle coverage
  - Easy-to-use Code Composer IDE and debug
- ✓ **Code Composer Studio will reduce development time and help ensure timely market delivery**
- ✓ **TI's leadership in DSP devices and advanced software tools enable cost-effective innovation**

49

THE WORLD LEADER IN DSP SOLUTIONS





## 'C5000: How to order tools

| Part Number           | Description                      |     | Price (US\$) |
|-----------------------|----------------------------------|-----|--------------|
| <b>Tools for PC</b>   |                                  |     |              |
| TMDS32000L0           | DSP Starter Kit DSKplus          | H+S | \$149        |
| TMDX3260051           | Evaluation Module (EVM)          | H+S | \$1,000      |
| TMDS324L850-02        | Assembler/Linker for PC          | S   | \$250        |
| TMDS324L855-02        | C Code Generation Tools          | S   | \$1,495      |
| TMDS324L851-02        | TI Simulator Debugger            | S   | \$500        |
| CCSIM54XWIN           | Code Composer Simulator Debugger | S   | \$1,000      |
| TMDS32401L0           | TI Emulator Debugger             | S   | \$2,000      |
| CCMSP54XWIN           | Code Composer Emulator Debugger  | S   | \$2,000      |
| TMDS00510             | XDS510 Emulator + JTAG cable     | H   | \$4,000      |
| <b>Tools for UNIX</b> |                                  |     |              |
| TMDS324L555-09        | C Code Generation Tools          | S   | \$3,600      |
| TMDS324L551-09        | TI Simulator Debugger            | S   | \$3,600      |
| TMDS32406L0           | TI Emulator Debugger             | S   | \$3,000      |
| TMDS00510WS           | XDS510WS Emulator + JTAG cable   | H   | \$6,000      |

50

THE WORLD LEADER IN DSP SOLUTIONS



## 'C6000: How to order tools

| Part Number           | Description                      |     | Price (US\$) |
|-----------------------|----------------------------------|-----|--------------|
| <b>Tools for PC</b>   |                                  |     |              |
| TMDX326006201         | EVM plus code gen tools          | H+S | \$1,995      |
| TMDX3260A6201         | EVM                              | H+S | \$995        |
| TMDS3246855-07        | C Code Generation Tools          | S   | \$1,495      |
| TMDX4356851-07        | TI Simulator Debugger            | S   | \$495        |
| CCSIM6XWIN            | Code Composer Simulator Debugger | S   | \$1,000      |
| TMDX3240160-07        | TI Emulator Debugger             | S   | \$1,995      |
| CCMSP6XWIN            | Code Composer Emulator Debugger  | S   | \$2,000      |
| TMDS00510             | XDS510 board + JTAG cable        | H   | \$4,000      |
| <b>Tools for UNIX</b> |                                  |     |              |
| TMDS3246555-07        | C Code Generation Tools          | S   | \$2,995      |
| TMDX3246551-07        | TI Simulator Debugger            | S   | \$995        |

51

THE WORLD LEADER IN DSP SOLUTIONS

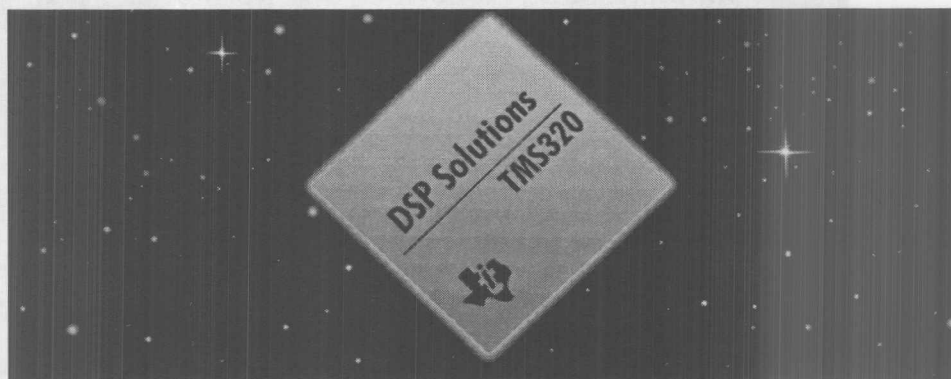






## **DSP Solution: Total capabilities**

**DSP Cores + Analog/Mixed Signal Products  
+ Software Libraries  
+ ASICs + Systems Knowledge  
+ Support Technologies**



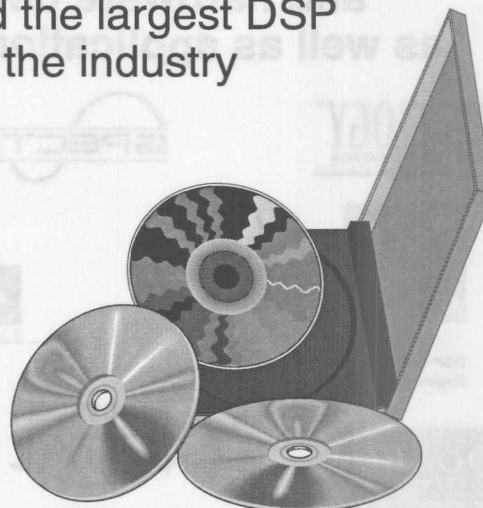
1

THE WORLD LEADER IN DSP SOLUTIONS



## **Support: Software libraries**

- ◆ Over 200 software algorithms available to customers and the largest DSP software base in the industry



2

THE WORLD LEADER IN DSP SOLUTIONS





## Support: Customer Choice Program

Worldwide network of more than 250 third-party companies providing the most extensive support available.

- Committed to TI's devices and new tools environment
- Offering cutting-edge technology tools
- Providing off-the-shelf or custom software algorithms optimized for performance and efficiency on our 'C5000/'C6000 platforms
- Innovative products for development and production
- Consultation services to aid in design and decrease time-to-market

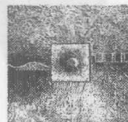
3

THE WORLD LEADER IN DSP SOLUTIONS



## Support: Customer Choice Program

A sampling of companies offering software and hardware development tools, as well as application software includes:



DSP Software  
Engineering, Inc.



4

THE WORLD LEADER IN DSP SOLUTIONS





## ***Support: Technical training***

### **Technical Training Organization**

- ◆ Expert instructors provide step-by-step training to help you program for optimum performance.
- ◆ See your Seminar Guide for training schedule



5

THE WORLD LEADER IN DSP SOLUTIONS



See the training schedule in the "For More Information" section.



## ***Support: Answering questions***

### **TI Hotline/Product Information Center**

- Well-trained specialists to assist any customer regardless of size
- Literature
- Technical documentation
- Information -- from tools updates to detailed design questions
- Response within 48 hours

6

THE WORLD LEADER IN DSP SOLUTIONS





## For more information...

- ◆ See “Appendix” and “For More Information” sections in your Seminar Guide for:
  - Related application notes and white papers
  - Web site URLs for technical documentation
  - Distributor contact information
  - TI Field Sales contact information
  - Product information

7

THE WORLD LEADER IN DSP SOLUTIONS



## Support: Answering questions

### TI Hotline/Product Information Center

- Well-trained specialists to assist any customer, regardless of size
- Literature
- Technical documentation
- Information – from tools updates to detailed design questions
- Response within 48 hours

## For more information

1. **For information about TI's DSP Solutions:**  
DSP Solutions Home Page:  
[www.ti.com/sc/docs/dsps/dsphome.htm](http://www.ti.com/sc/docs/dsps/dsphome.htm)  
  
'C6000 Platform Home Page:  
[www.ti.com/sc/docs/dsps/products/c6000/index.htm](http://www.ti.com/sc/docs/dsps/products/c6000/index.htm)  
  
'C5000 Platform Home Page:  
[www.ti.com/sc/docs/dsps/products/c5000/c54x/index.htm](http://www.ti.com/sc/docs/dsps/products/c5000/c54x/index.htm)  
  
Mixed Signal and Analog Products Home Page:  
[www.ti.com/sc/docs/msp/msphome.htm](http://www.ti.com/sc/docs/msp/msphome.htm)
2. **To contact Texas Instruments:**  
TI Product Information (USA)  
Product Information Center  
(972) 644-5580  
[www.ti.com/sc/docs/pic/home.htm](http://www.ti.com/sc/docs/pic/home.htm)  
  
TI Literature Response Center (USA)  
(800) 477-8924  
  
TMS320 DSP Hotline  
(281) 274-2320  
[www.ti.com/dsps](http://www.ti.com/dsps)  
  
TI Semiconductor Support  
[www.ti.com/sc/docs/support/support.htm](http://www.ti.com/sc/docs/support/support.htm)
3. **TI&ME Internet Information Service:**  
Personalized weekly email newsletter and a custom web page for information on the interests you specify.  
[www-a.ti.com/apps/ti\\_me/signin.asp](http://www-a.ti.com/apps/ti_me/signin.asp)
4. **For a complete list of TI Distributors near you, please visit:**  
[www.ti.com/sc/docs/distmenu.htm](http://www.ti.com/sc/docs/distmenu.htm)
5. **For a complete list of TI's Third Parties, please visit:**  
[www.ti.com/sc/docs/dsps/develop/3party.htm](http://www.ti.com/sc/docs/dsps/develop/3party.htm)

(continued)

**6. To contact a sampling of the Third-Party companies supporting TI's high-performance 'C6000 and 'C5000 Platforms:**

Blue Wave Systems  
Loughborough Park, Ashby Road  
Loughborough Leicester LE11 3NE  
United Kingdom  
Tel: +44 1509 634300; Fax: +44 1509 634333  
e-mail: sales@lsi-dsp.com  
www: <http://www.lsi-dsp.com>

D2 Technologies, Inc.  
104 West Anapamu Street  
Santa Barbara, CA 93101 USA  
Tel: (805) 564-3424; Fax: (805) 966-2144  
e-mail: sales@d2tech.com  
www: <http://www.d2tech.com>

DSP Research, Inc.  
1095 E. Duane Ave., Suite 203  
Sunnyvale, CA 94086 USA  
Tel: (408) 773-1042; Fax: (408) 736-3451  
e-mail: info@dspr.com  
www: <http://www.dspr.com>

DSP Software Engineering, Inc.  
175 Middlesex Turnpike  
Bedford, MA 01730 USA  
Tel: (781) 275-3733; Fax: (781) 275-4323  
e-mail: info@dspse.com  
www: <http://www.dspse.com>

Eonic Systems, Inc.  
C.I.T. Building, 2214 Rock Hill Road, Ste. 120  
Herndon, VA 20170-4200 USA  
Tel: (703) 707-9500; Fax: (703) 707-9525  
e-mail: info@eonic.com  
www: <http://www.eonic.com>

HotHaus Technologies, Inc.  
170 - 6651 Fraserwood Place  
Richmond, British Columbia, Canada, V6W 1J3  
Tel: (604) 278-4300; Fax: (604) 278-4317  
e-mail: info@hothaus.com  
www: <http://www.hothaus.com>

*(continued)*

Pentek, Inc.  
One Park Way  
Upper Saddle River, NJ 07458-2311 USA  
Tel: (201) 818-5900; Fax: 201-818-5904  
e-mail: [info@pentek.com](mailto:info@pentek.com)  
www: <http://www.pentek.com>

Spectrum Digital, Inc.  
10853 Rockley Road  
Houston, TX 77099 USA  
Tel: (281) 561-6952; Fax: (281) 561-6037  
e-mail: [sales@spectrumdigital.com](mailto:sales@spectrumdigital.com)  
www: <http://www.spectrumdigital.com>

Spectrum Signal Processing Inc.  
100-8525 Baxter Place  
Burnaby, BC V5A 4V7 Canada  
Tel: (604) 421-5422; Fax: (604) 421-1764  
e-mail: [Sales@SpectrumSignal.com](mailto:Sales@SpectrumSignal.com)  
www: <http://www.spectrumsignal.com>

Telogy Networks  
20250 Century Boulevard  
Germantown, MD 20874 USA  
Tel: (301) 515-6690; Fax: (301) 515-7954  
e-mail: [gginquiry@telogy.com](mailto:gginquiry@telogy.com)  
www: <http://www.telogy.com>

Traquair Data Systems, Inc.  
114 Sheldon Road  
Ithaca, NY 14850 USA  
Tel: (607) 266-6000; Fax: (607) 266-8221  
e-mail: [traquair@traquair.com](mailto:traquair@traquair.com)  
www: <http://www.traquair.com>

White Mountain DSP, Inc.  
20 Cotton Road, Suite 101  
Nashua, NH 03063 USA  
Tel: (603) 883-2430; Fax: (603) 882-2655  
e-mail: [info@wmdsp.com](mailto:info@wmdsp.com)  
www: <http://www.wmdsp.com>

7. **For Technical Documentation for all of TI's DSPs, please visit:**  
[www.ti.com/sc/docs/dsps/literatu.htm](http://www.ti.com/sc/docs/dsps/literatu.htm)
8. **For a listing of related application notes, please visit:**  
[www.ti.com/sc/docs/psheets/app\\_dsp.htm](http://www.ti.com/sc/docs/psheets/app_dsp.htm) (*scroll to: 'C6000 or 'C5000 platform sections*)
9. **To learn more about designing with 'C6000 and 'C5000 for high-performance applications:**

Technical Training  
[www.ti.com/sc/training](http://www.ti.com/sc/training)

Courses scheduled for the remainder of 1998:

**TMS320C5000**

10/06/98 - Boston  
11/17/98 - Dallas

**TMS320C6000**

10/06/98 - San Jose  
10/20/98 - Boston  
10/27/98 - Dallas  
11/03/98 - Chicago  
12/01/98 - Boston  
12/08/98 - San Jose  
12/15/98 - Dallas

**DSP/BIOS**

11/12/98 - Santa Barbara

## ***Table of Contents:***

# **Appendix**

- List of Application Reports and White Papers
- *TMS320C6211 Cache Analysis*
- *Guidelines for Software Development Efficiency on the TMS320C6000 VelociTI Architecture*
- *Designing Low-Power Applications with the TMS320LC54x*
- *TMS320C54x DSP Programming Environment*

## Table of Contents

# Appendix

- List of Application Reports and White Papers
- TMS320C6211 Cache Analysis
- Guidelines for Software Development Efficiency on the TMS320C6000 Velocity Architecture
- Designing Low-Power Applications with the TMS320LC54x
- TMS320C54x DSP Programming Environment

## 'C5000 Reference Material

### How Do I Get My Performance:

|                                                         |         |
|---------------------------------------------------------|---------|
| 'C54x Extended Addressing                               | SPRA184 |
| Digital Signal Processors vs. Universal Microprocessors | SPRA344 |
| Extending Fixed-Point Dynamic Ranges                    | DNP53   |

### How Do I Interface Easily:

|                                                            |         |
|------------------------------------------------------------|---------|
| A TDM Interface for the TMS320C54x DSP                     | SPRA453 |
| Accessing TMS320C54x Memory-Mapped Registers in C          | SPRA260 |
| Implementing Circular Buffers with Bit-Reversed Addressing | SPRA292 |
| IOM-2 Interfacing on the TMS320C54x                        | BPRA074 |
| Shared Memory Interface with TMS320C54x DSP                | SPRA441 |
| The TMS320C54x DSP HPI and PC Parallel Port Interface      | SPRA151 |
| Using VRAMS and DSPS for System Performance                | SPRA224 |

### How Do I Minimize Power Dissipation:

|                                                       |           |
|-------------------------------------------------------|-----------|
| Calculation of TMS320LC54x Power Dissipation          | SPRA164   |
| Designing Low-Power Applications with the TMS320LC54x | SPRA281** |
| Dual Power Supply Management for the TMS320VC549 DSP  | SPRA280   |

### How Do TI's Tools Make My Development Easier:

|                                                        |           |
|--------------------------------------------------------|-----------|
| Sharing Header Files in C and Assembly                 | SPRA205   |
| TMS320C54x DSP Programming Environment                 | SPRA182** |
| TMS320C5x to TMS320C54x Translator                     | BPRA075   |
| Interfacing a DSKPlus with Flash Memory Daughter Board | SPRA456   |
| Initializing the Fixed-Point EVM's AIC                 | DNP10     |

### What Support Can I Count On:

|                                                                      |          |
|----------------------------------------------------------------------|----------|
| DSP Solutions for Telephony and Data/Facsimile Modems                | SPRA073  |
| DTMF Tone Generation and Detection on the TMS320C54x                 | SPRA096  |
| Echo Cancellation S/W for 'C54x                                      | BPRA054  |
| The Implementation of G.726 ADPCM on the TMS320C54x DSP              | BPRA053  |
| A-law and $\mu$ -law Companding Implementations Using the TMS320C54x | SPRA163A |
| High-Density Design with Microstar BGAs                              | SPRA471A |
| IIR Filter Design on the TMS320C54x DSP                              | SPRA079  |
| Implementing a Line-Echo Canceller Using Block Update and NLMS       | SPRA188  |

\*\*Included in the appendix

## 'C6000 Reference Material

### How Do I Get My Performance:

|                                    |                |
|------------------------------------|----------------|
| Direct CPU Data Access Wait States | Please request |
| TMS320C6201 DMA Applications       | Please request |
| TMS320C6211 Cache Analysis         | SPRA472**      |

### How Do I Interface Easily:

|                                                              |                |
|--------------------------------------------------------------|----------------|
| 'C6x McBSP as a TDM Highway                                  | Please request |
| McBSP Initialization                                         | Please request |
| McBSP Interface to a Voice-Band Audio Processor              | Please request |
| McBSP Interface to a Single Rate ST Bus                      | Please request |
| SPI ROM Interface to McBSP                                   | Please request |
| HPI to Popular Hosts and PCI Bridge Chips                    | Please request |
| EMIF to SDRAM                                                | Please request |
| EMIF to Flash Memory                                         | Please request |
| EMIF to FIFOs                                                | Please request |
| 'C6202 Expansion Bus Interfaces                              | Please request |
| TMS320C6x EMIF to External SDRAM/SGRAM Interface             | SPRA433        |
| Using the TMS320C6x McBSP as a High Speed Communication Port | SPRA455        |
| TMS320C6201/6701 DSP Host Port Interface Performance         | SPRA449        |

### What Is My Power Consumption:

|                                         |                |
|-----------------------------------------|----------------|
| 'C62x Power Consumption Summary         | Please request |
| TMS320C6201 Power Supply                | SPRA444        |
| TMS320C6x Thermal Design Considerations | SPRA432        |

### How Do TI's Tools Make My Development Easier:

|                                                                                         |           |
|-----------------------------------------------------------------------------------------|-----------|
| Guidelines for Software Development Efficiency on the TMS320C6000 VelociTI Architecture | SPRA434** |
| How to Begin Development Today with the TMS320C6202 DSP                                 | SPRA473   |
| How to Begin Development Today with the TMS320C6211 DSP                                 | SPRA474   |

### What Support Can I Count On:

|                                                                                 |                |
|---------------------------------------------------------------------------------|----------------|
| TMS320C6x Manufacturing with the BGA Package                                    | SPRA429        |
| Loop Partitioning on the 'C6x                                                   | Please request |
| Bit-Reverse/Digit-Reverse: Linear-Time Small Lookup Table Implementation        | SPRA440        |
| Implementation of G.726 ADPCM on the TMS320C62xx DSP                            | BPRA066        |
| Performance Analysis of Line Echo Cancellation Implementation Using TMS320C6201 | SPRA421        |

\*\*Included in the appendix

***Application Report:***  
**TMS320C6211**  
**Cache Analysis**



# ***TMS320C6211 Cache Analysis***

## **Abstract**

The TMS320C6211's caches deliver high performance without the cost of large arrays of on-chip memory. The efficiency of the TMS320C6211 caches makes low cost, high-density external memory, such as SDRAM, as effective as on-chip memory.

## **Contents**

|          |                                            |           |
|----------|--------------------------------------------|-----------|
| <b>1</b> | <b>Cache Architecture Overview .....</b>   | <b>2</b>  |
| 1.1      | Level-one Program Cache (L1P) .....        | 3         |
| 1.2      | Level-one Data Cache (L1D) .....           | 4         |
| 1.3      | Level-two Cache/Unified Memory (L2) .....  | 4         |
| <b>2</b> | <b>Cache Performance .....</b>             | <b>7</b>  |
| 2.1      | Price / Performance .....                  | 7         |
| 2.2      | Two-Level Cache Benefits .....             | 7         |
| 2.2.1    | L2 reduces latency due to cache miss ..... | 8         |
| 2.2.2    | Unifying program and data in L2 .....      | 8         |
| 2.3      | Real-time operation .....                  | 8         |
| 2.3.1    | Predictability .....                       | 8         |
| 2.3.2    | Interrupt Latency .....                    | 8         |
| <b>3</b> | <b>Efficient I/O Capability .....</b>      | <b>9</b>  |
| 3.1      | Ease of use .....                          | 10        |
| <b>4</b> | <b>Summary .....</b>                       | <b>10</b> |

## **Figures**

|                  |                                                     |          |
|------------------|-----------------------------------------------------|----------|
| <b>Figure 1.</b> | <b>TMS320C6211 Block Diagram .....</b>              | <b>2</b> |
| <b>Figure 2.</b> | <b>TMS320C6211 Two-level cache fetch flow .....</b> | <b>3</b> |
| <b>Figure 3.</b> | <b>L2 Memory Configurations, Diagram 1 .....</b>    | <b>5</b> |
| <b>Figure 4.</b> | <b>L2 Memory Configurations, Diagram 2 .....</b>    | <b>5</b> |
| <b>Figure 5.</b> | <b>Data Allocation in Multiple Cache Ways .....</b> | <b>6</b> |
| <b>Figure 6.</b> | <b>Typical processor peripheral data flow .....</b> | <b>9</b> |
| <b>Figure 7.</b> | <b>TMS320C6211 peripheral data flow .....</b>       | <b>9</b> |

## **Tables**

|                 |                                                |          |
|-----------------|------------------------------------------------|----------|
| <b>Table 1.</b> | <b>TMS320C6211 Benchmark Performance .....</b> | <b>7</b> |
|-----------------|------------------------------------------------|----------|

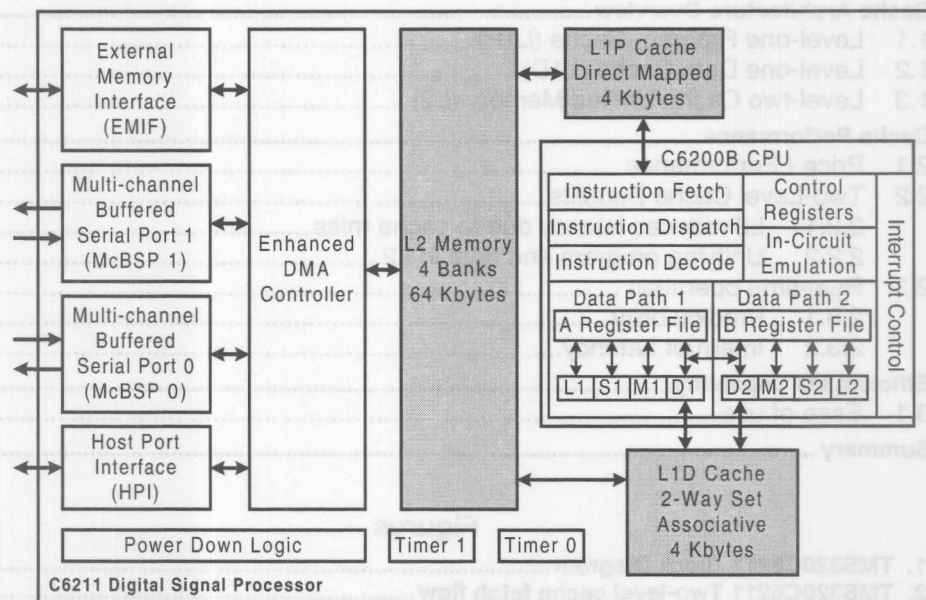


## 1 Cache Architecture Overview

The TMS320C6211 ('C6211) utilizes a highly efficient two-level real-time cache for internal program and data storage (See Figure 1). The 'C6211's caches deliver high performance without the cost of large arrays of on-chip memory. The efficiency of the TMS320C6211 caches makes low cost, high-density external memory, such as SDRAM, as effective as on-chip memory. The 'C6211 executes over 99.5% of all CPU cycles without going off-chip. This leads to greater than 80% of the cycle count performance of a C62x device with infinite internal memory.

The TMS320C6211 employs a two-level memory architecture for on chip program and data accesses. The first level has dedicated 4 Kbyte program and data caches, L1P and L1D respectively. The second level memory is a 64 Kbyte memory-block that is shared by both the program and data, designated L2. Dedicated L1 caches eliminate conflicts for the memory resources between the program and data busses. A unified L2 memory provides flexible memory allocation between program and data for accesses that do not reside in L1. Since data is frequently resident in L1, flexibility is more important at the L2 level than conflict reduction.

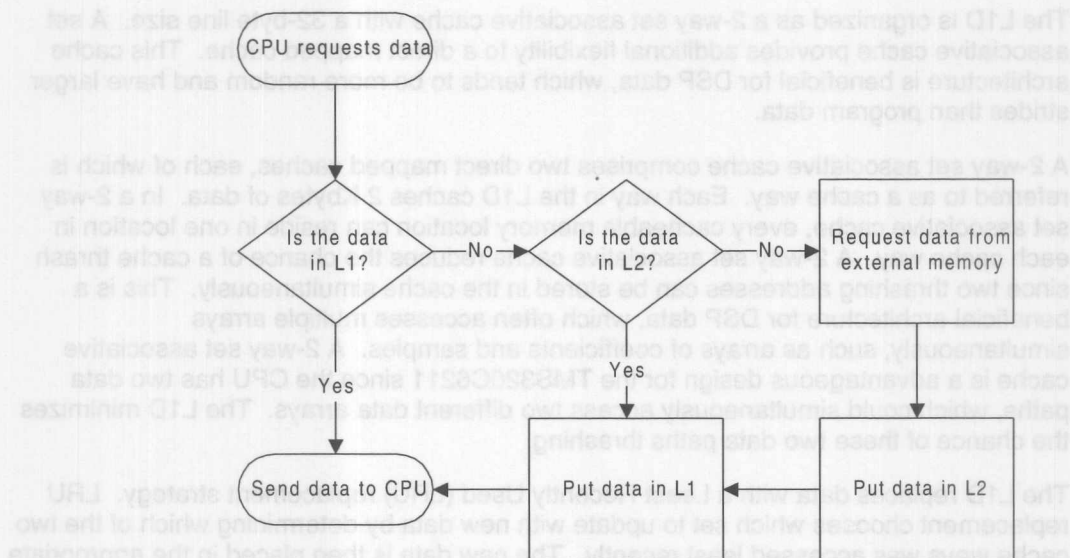
Figure 1. TMS320C6211 Block Diagram



Each cache consists of cache memory, a smaller block of memory to save the state of the cache known as a tag RAM, and a cache controller. When an access is initiated by the CPU, the cache controller checks its tag RAM to determine if that data resides in the cache. If that data does reside in the cache a cache hit occurs and that data is sent to the CPU. If the CPU data does not reside in the cache, then a cache miss occurs. On a cache miss, the controller requests the data from the next level memory. In the case of an L1P or L1D miss, the next level memory is the L2. In the case of an L2 miss, the next level memory is the external memory. The amount of data that a cache requests on a miss is referred to as the cache's line size. Figure 2 illustrates the decision process used by the 'C6211 memory system to fetch the correct data on a CPU request.



Figure 2. TMS320C6211 Two-level cache fetch flow



By using a cache, which dynamically allocates memory to reduce the latency to slower memory, a processor's performance is dramatically increased. A cache's performance can be affected by a situation known as thrashing. For thrashing to occur, data must be read into the cache. Subsequently, another location is cached whose data overwrites the first data. When the first data is requested again, the cache must again fetch it from the slow memory.

## 1.1 Level-one Program Cache (L1P)

The L1P is organized as a direct mapped cache with a 64-byte line size. A direct mapped cache is well suited for DSP algorithms, which tend to consist of small, tight loops that rarely thrash. The L1P line size provides a modest prefetch of the next fetch packet, eliminating the startup latency for fetching that packet.

In direct mapped cache, every cacheable memory location maps to only one location in the cache. Thus, the cache controller needs to check only one location in the tag RAM to determine if requested data is available in the cache. DSP algorithms primarily consist of loops that execute the same program kernel many times on multiple data locations. Such algorithms remain in a loop for a long time before proceeding to the next kernel. The L1P is large enough to hold several typical DSP kernels simultaneously. Since these kernels execute sequentially, they will not thrash in the L1P. Thus, a simple direct mapped cache is all that is needed to achieve considerable program performance without requiring complex caching hardware.

When a cache miss occurs, the L1P requests an entire line of data from the L2. In other words, both the requested fetch packet and the next fetch packet in memory are loaded into the cache. Since most applications execute sequential instructions, there is a high likelihood that the next fetch packet will be immediately available when it is requested by the CPU. Thus, the startup latency to fetch the next fetch packet is eliminated by bursting an entire cache line. Fetching ahead also reduces the number of cache misses. Eliminating startup latency and reducing misses reduces the execution time of an application considerably compared to a cache with a smaller line size.



## 1.2 Level-one Data Cache (L1D)

The L1D is organized as a 2-way set associative cache with a 32-byte line size. A set associative cache provides additional flexibility to a direct mapped cache. This cache architecture is beneficial for DSP data, which tends to be more random and have larger strides than program data.

A 2-way set associative cache comprises two direct mapped caches, each of which is referred to as a cache way. Each way in the L1D caches 2 Kbytes of data. In a 2-way set associative cache, every cacheable memory location can reside in one location in each cache way. A 2-way set associative cache reduces the chance of a cache thrash since two thrashing addresses can be stored in the cache simultaneously. This is a beneficial architecture for DSP data, which often accesses multiple arrays simultaneously, such as arrays of coefficients and samples. A 2-way set associative cache is a advantageous design for the TMS320C6211 since the CPU has two data paths, which could simultaneously access two different data arrays. The L1D minimizes the chance of these two data paths thrashing.

The L1D replaces data with a Least Recently Used (LRU) replacement strategy. LRU replacement chooses which set to update with new data by determining which of the two cache ways was accessed least recently. The new data is then placed in the appropriate set of that least recently used way. LRU is the best replacement strategy for set associative caches because of the temporal locality of data – once data has been used it will probably be needed again within a short time. Thus, a cache should always keep data that was most recently used, and replace the least recently used data.

Like the L1P, the L1D line size provides a prefetch of subsequent data, minimizing the fetch latency for that data. When a cache miss occurs, the L1D requests an entire line of data from the L2. When the CPU is fetching a data array from contiguous non-cache memory, this greatly reduces the latency for subsequent data fetches. In the case of an array of words, only the first fetch will experience the delay in going to the L2 or off chip. The next seven array elements will be fetched from the L1D, each in a single cycle. For half-word and byte arrays, the benefit will be even greater since the next 15 or 31 array elements will be in the cache.

The L1D memories are dual ported, which allows the L1D to support two simultaneous CPU data accesses without stalling.

## 1.3 Level-two Cache/Unified Memory (L2)

The L2 is a 64-Kbyte SRAM divided into four 16-Kbyte blocks. The L2 is a unified memory, used for both program and data. The amount of program or data in the L2 is configurable. For example, if your application requires only 7 Kbytes of program space and 57 Kbytes of data space then both could be linked into the L2 at the same time. Likewise, if your application needed more program space than data, the majority of the L2 RAM could be linked as program space.

Each of the four blocks can be independently configured as either cache or memory mapped RAM. This allows you to dictate the amount of the L2 that is used as cache and how much is used as RAM. If your application uses some data which must be accessed quickly that data can be linked into an L2 block which is configured as RAM. The rest of the L2 can be configured as cache, which will provide high performance operation of the remaining program and data.



When an L2 block is configured as RAM, external data is not cached in that block; instead, that memory is accessed by direct addressing. Each block that is configured as a cache adds a cache way to the L2. For example, when only one block is configured as cache, the L2 operates as a 1-way set associative (direct mapped) cache and 48 Kbytes of RAM. When all four blocks are configured as cache, the L2 operates as a 4-way set associative cache. Figure 3 and Figure 4 illustrate the division of the L2 memory space according to the L2 Mode.

Figure 3. L2 Memory Configurations, Diagram 1

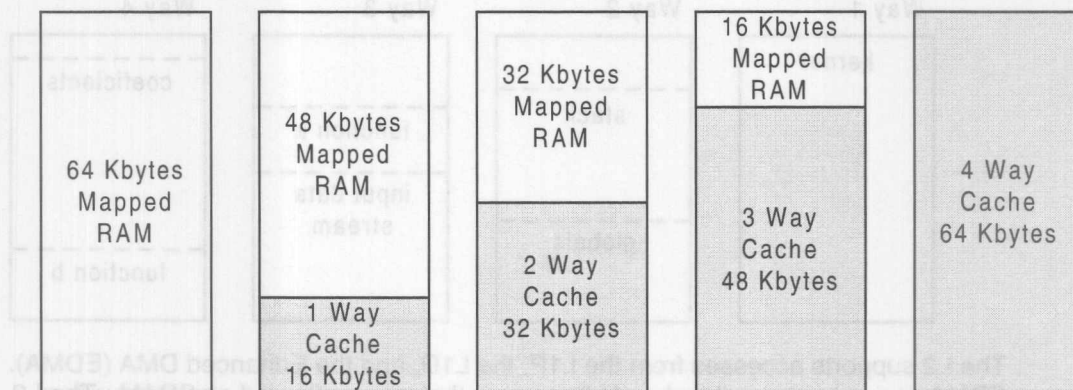
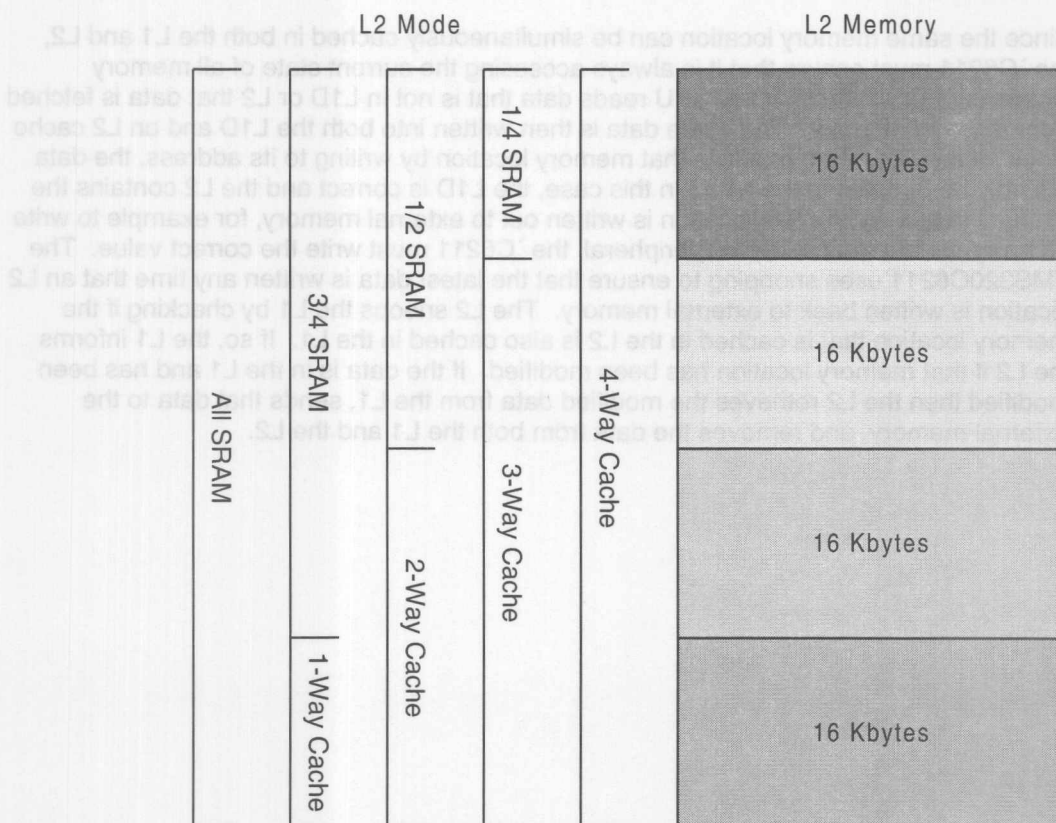


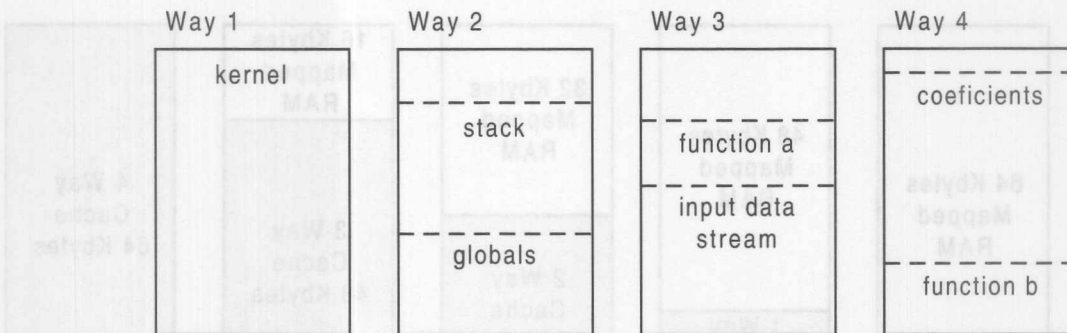
Figure 4. L2 Memory Configurations, Diagram 2





By providing a high level of associativity, the L2 minimizes thrashing between multiple data sources. For example, your application could execute program data on an array of coefficients, another data array, and a stack. The associativity of the L2 eliminates thrashing between the data since each data source can be cached by a different cache way. Figure 5 depicts an example of how multiple data streams can reside in the L2 without thrashing.

Figure 5. Data Allocation in Multiple Cache Ways



The L2 supports accesses from the L1P, the L1D, and the Enhanced DMA (EDMA). The EDMA can only access blocks of L2 memory that are configured as SRAM. The L2 memories are organized as four 64-bit wide banks. Two simultaneous accesses are serviced without stalling if the two accesses do not use the same bank. Thus, concurrent accesses by the L1D and EDMA busses to different banks are serviced without stalling.

Since the same memory location can be simultaneously cached in both the L1 and L2, the  $\text{\texttt{C6211}}$  must ensure that it is always accessing the current state of all memory locations. For example, if the CPU reads data that is not in L1D or L2 that data is fetched from external memory. The same data is then written into both the L1D and an L2 cache block. If the CPU then modifies that memory location by writing to its address, the data will only be updated in the L1D. In this case, the L1D is correct and the L2 contains the old data value. When this location is written out to external memory, for example to write an array of data to an external peripheral, the  $\text{\texttt{C6211}}$  must write the correct value. The TMS320C6211 uses snooping to ensure that the latest data is written any time that an L2 location is written back to external memory. The L2 snoops the L1 by checking if the memory location that is cached in the L2 is also cached in the L1. If so, the L1 informs the L2 if that memory location has been modified. If the data is in the L1 and has been modified then the L2 retrieves the modified data from the L1, sends that data to the external memory, and removes the data from both the L1 and the L2.



## 2 Cache Performance

The two-level cache of the TMS320C6211 achieves a high level of performance. Tests have shown that typical applications running on the TMS320C6211 operate at greater than 80% of the optimal cycle count performance of a C62x device. Optimal performance would be achieved only by having infinite internal program and data memory.

Table 1. TMS320C6211 Benchmark Performance

| Application            | Efficiency |
|------------------------|------------|
| v.34                   | 89%        |
| AC-3 Decoder           | 90%        |
| Zlib File Compression  | 96%        |
| Line Echo Cancellation | 99%        |
| GSM Frame Encoder      | 92%        |
| GSM Frame Decoder      | 88%        |
| ADSL                   | 85%        |

This level of performance is achievable due to the high hit rate of the L1 cache. Typically, 98% of program fetches execute without an L1P miss and 91% of data fetches hit in the L1D. When the L2 is configured as 4-way associative cache, normally 96% of the requests to the L2 are found in the L2 cache. Over 99.5% of all CPU cycles execute without requiring an access to external memory, virtually eliminating the access penalty associated with external memory devices.

### 2.1 Price / Performance

The primary focus of the TMS320C6211 is to achieve an easy to use, low cost, device with outstanding performance. The TMS320C6211 External Memory Interface (EMIF) has been optimized to operate a variety of devices. The C6211 offers 8-, 16-, and 32-bit interfaces to asynchronous memory, SDRAM, and SBRAM devices. This enables you to take advantage of a high performance processor with single chip external memory solutions, reducing total system cost and board area.

### 2.2 Two-Level Cache Benefits

The cache architecture of the TMS320C6211 allows the device to achieve high performance without large amounts of expensive on-chip memory. By having an efficient cache, low cost, high-density external memory, such as SDRAM, is as effective as on-chip memory. Having a two-level cache provides several benefits over a one-level cache system. It allows reduced latency for an L1 cache miss, and it unifies the program and data in the same on-chip memory.



### 2.2.1 L2 reduces latency due to cache miss

By providing the L2 space, L1 cache misses may be serviced much more quickly. There is a significant reduction in cycle time for retrieving data from on-chip L2 memory than from an external memory. All external memory devices have significant startup latencies associated with them. By having the intermediate L2 cache, this latency is hidden from the user. The external memories that interface to the 'C6211 may operate at a maximum of 100 MHz, while the device operates at a 150 MHz maximum frequency. Using the fast L2 memories to cache the slower external memories reduces the latency of external accesses by a factor of five. The wide, high-bandwidth L2 bus transfers data at up to 1920 Mbytes/s while the EMIF interface operates at up to 400 Mbytes/s.

### 2.2.2 Unifying program and data in L2

By unifying the program and data in the L2 space, the L2 cache is more likely to hold the memory requested by the CPU. It enables the on-chip memory to contain more data than program when highly computational, looping code is being run to process large data streams. For long, serial code with few data accesses, the L2 may be more densely populated with program instructions. The unification allows you to allocate the appropriate amount of memory for both program and data and keeps the on-chip memory full of instructions and data that are the most likely to be requested by the CPU.

## 2.3 Real-time operation

An important concern in cache systems is that the device be able to perform in real time. There are several requirements for a system to ensure that real-time operation is possible. The operation of the device must be predictable, interrupts to the CPU must be handled without affecting the continued real-time operation of the device, and efficient I/O must be maintained.

### 2.3.1 Predictability

The TMS320C6211 has a high degree of predictability. Device operation typically achieves over 80% of performance of a 'C62x device with infinite on-chip memory. Software tools to simulate the performance of the cache will be available in early 4Q98 to help you optimize system performance.

### 2.3.2 Interrupt Latency

Interrupt handling is an important part of DSP operation. It is crucial that the DSP be able to receive and handle interrupts while maintaining real-time operation. In typical applications, interrupt frequency has not increased in proportion to the increase in device operation frequency. As processing speeds have increased, latency requirements have not.

The TMS320C6211 is capable of servicing interrupts with a latency of a fraction of a microsecond when the service routine is located in external memory. By configuring the L2 memory blocks as memory-mapped SRAM, it is possible to lock critical program and data sections into internal memory. This is ideal for situations such as interrupts and OS task switching. By locking routines that need to be performed in minimal time, the microsecond delay for interrupts is reduced to tens of nanoseconds.



### 3 Efficient I/O Capability

Peripherals are a feature of most DSP systems that can take advantage of the memory-mapped L2 RAM. Typical processors require that peripheral data first be placed in external memory before it can be accessed by the CPU. The TMS320C6211 can maintain data buffers in on-chip memory, rather than in off-chip memory, providing a higher data throughput to peripherals. This increases performance when using on-chip McBSPs, the HPI, or external peripherals. The EDMA can be used to transfer data directly into mapped L2 space while the CPU processes the data. This increases performance since the CPU is not stalled while fetching data from slow external memory or directly from the peripheral. Using this method for transferring data also minimizes EMIF activity, which is crucial as data rates or the number of peripherals increase. Figure 6 illustrates the data flow from a peripheral to a typical processor. Figure 7 shows the same data flow from a peripheral to the TMS320C6211.

Figure 6. Typical processor peripheral data flow

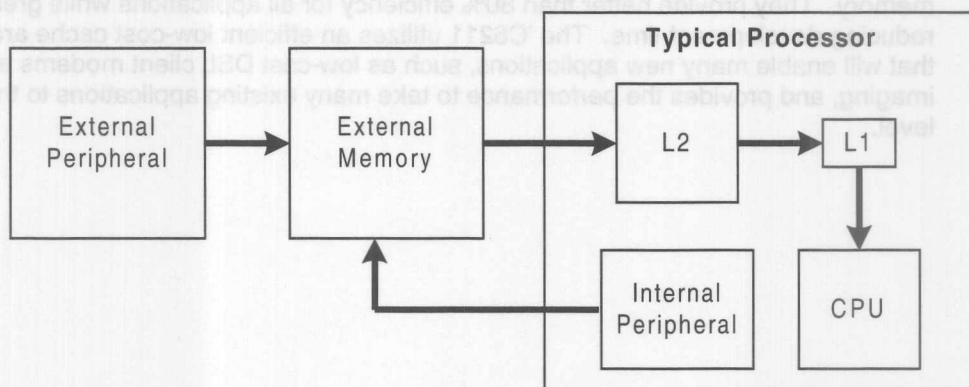
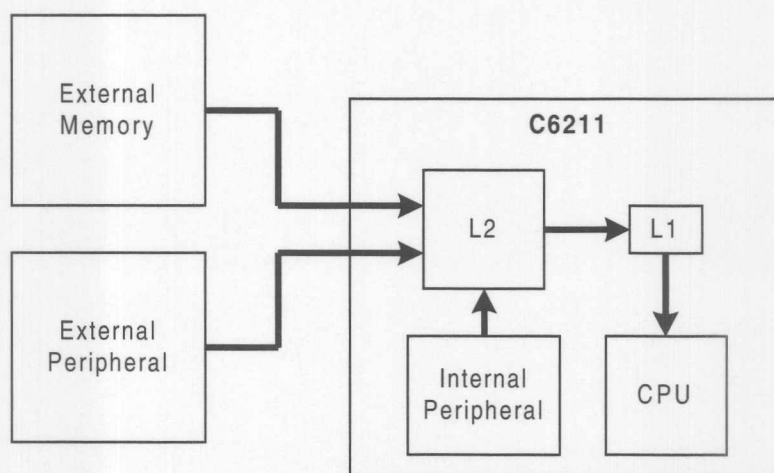


Figure 7. TMS320C6211 peripheral data flow



### 3.1 Ease of use

The efficiency of the 'C6211 cache architecture makes the device simple to use. The cache is inherently transparent to the user. Due to the level of associativity and the high cache hit rate, virtually no optimization must be done to achieve high performance. Reduced time for optimization leads to reduced development time, allowing functional systems to be up and running quickly. High performance can be immediately achieved with the 'C6211 cache architecture, while Harvard architecture with small internal memory requires much more time to achieve similar performance. This is because optimizing an application on a small Harvard architecture requires several iterations to tune the application to fit in the small, fixed internal memories.

## 4 Summary

The TMS320C6211 two-level cache architecture is optimized for DSP applications. The 'C6211's caches deliver high performance without the cost of large arrays of on-chip memory. They provide better than 80% efficiency for all applications while greatly reducing development time. The 'C6211 utilizes an efficient low-cost cache architecture that will enable many new applications, such as low-cost DSL client modems and imaging, and provides the performance to take many existing applications to the next level.

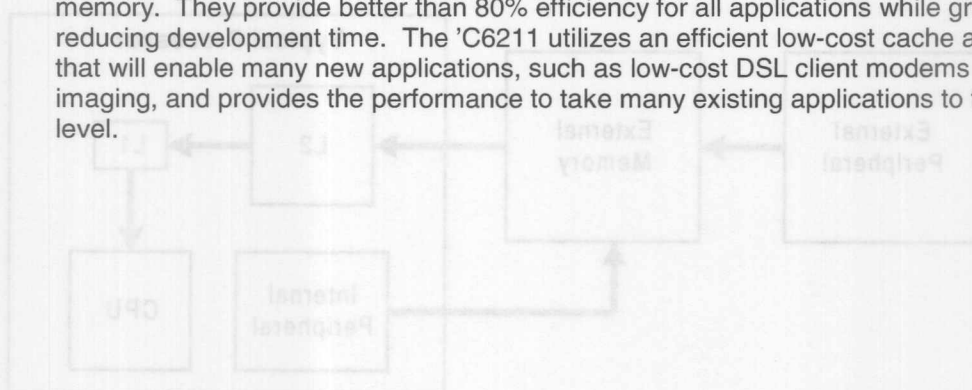
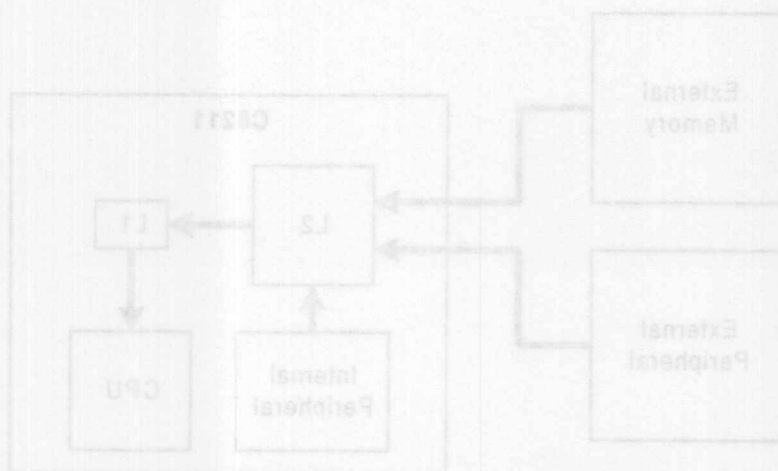


Figure 7. TMS320C6211 peripheral data flow





---

**IMPORTANT NOTICE**

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current and complete. TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements. Certain application using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications"). TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS. Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office. In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards. TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1998, Texas Instruments Incorporated

TI is a trademark of Texas Instruments Incorporated.

Other brands and names are the property of their respective owners



***White Paper:***  
**Guidelines for Software  
Development Efficiency on the  
TMS320C6000 VelociTI  
Architecture**



# ***Guidelines for Software Development Efficiency on the TMS320C6000 VelociTI Architecture***

---

---

***WHITE PAPER: SPRA434***

***Authors: Marie Silverthorn  
Leon Adams  
Richard Scales***

***Digital Signal Processing Solutions  
April 1998***



## IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain application using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1998, Texas Instruments Incorporated



## TRADEMARKS

TI and VelociTI are trademarks of Texas Instruments Incorporated.

Other brands and names are the property of their respective owners.

## CONTACT INFORMATION

|                   |                |
|-------------------|----------------|
| US TMS320 HOTLINE | (281) 274-2320 |
| US TMS320 FAX     | (281) 274-2324 |
| US TMS320 BBS     | (281) 274-2323 |
| US TMS320 email   | dsph@ti.com    |

## Contents

|                                                         |    |
|---------------------------------------------------------|----|
| Abstract .....                                          | 7  |
| Product Support on the World Wide Web .....             | 8  |
| Introduction .....                                      | 9  |
| DSP Product Line Compatibility .....                    | 10 |
| Recommended DSP Software Development Flow .....         | 13 |
| Benefits .....                                          | 16 |
| Appendix A. TI TMS320C6000 Optimization Checklist ..... | 18 |
| Appendix B. Reuse libraries.....                        | 20 |
| Appendix C. References .....                            | 21 |

## Figures

|                                                           |    |
|-----------------------------------------------------------|----|
| Figure 1. TMS320C6000 Code Reuse Efficiency Diagram ..... | 11 |
| Figure 2. Recommended DSP Software Development Flow ..... | 13 |
| Figure 3. Software Development Cycle Time Results.....    | 17 |



Product Support on the World Wide Web

Our World Wide Web site at [www.ti.com](http://www.ti.com) contains the most up to date product information, revisions, and additional. Users registering with TI&E can build custom information pages and receive new product updates automatically via email.

# Guidelines for Software Development Efficiency on the TMS320C6000 VelociTI Architecture

## Abstract

This white paper recommends programming and reuse techniques designed to develop efficient software applications for the Texas Instruments (TI™) TMS320C6000 digital signal processor (DSP). The TMS320C6000 DSP belongs to a powerful generation of DSPs designed with the TI VelociTI™ advanced VLIW architecture.

As DSP capability increases, product designers create more complex software applications. Responding to the desire of our clients to create and reuse code efficiently, Texas Instruments is committed to creating software development tools that support increasingly efficient, powerful, and easy to use programming environments.

A new feature of the Texas Instruments C6000 code is its compatibility with future C6000 platforms. This includes ANSI C code, ANSI C code with TI C6000 Language extensions, and TI C6000 Linear Assembly code.

The programming guidelines recommended in this paper include an efficient C6000 programming technique and offer references for additional detail. A code reuse efficiency diagram and development flow chart are included to aid understanding.

**We highly recommend using C with TI C6000 Language Extensions as the software development language for TI C6000 software development.**



## Product Support on the World Wide Web

Our World Wide Web site at **www.ti.com** contains the most up to date product information, revisions, and additions. Users registering with TI&ME can build custom information pages and receive new product updates automatically via email.

# Guidelines for Software Development Efficiency on the TMS320C6000 VelociTI Architecture

## Abstract

This white paper recommends programming and reuse techniques designed to develop efficient software applications for the Texas Instruments (TI) TMS320C6000 digital signal processor (DSP). The TMS320C6000 DSP belongs to a powerful generation of DSPs designed with the TI VelociTI™ advanced VLIW architecture.

As DSP capability increases, product designers create more complex software applications. Responding to the desire of our clients to create and reuse code efficiently, Texas Instruments is committed to creating software development tools that support increasingly efficient, powerful, and easy to use programming environments.

A new feature of the Texas Instruments C6000 code is its compatibility with future C6000 platforms. This includes ANSI C code, ANSI C code with TI C6000 Language extensions, and TI C6000 Linear Assembly code.

The programming guidelines recommended in this paper include an efficient C6000 programming technique and other references for additional detail. A code reuse efficiency diagram and development flow chart are included to aid understanding.

We highly recommend using C with TI C6000 Language Extensions as the software development language for TI C6000 software development.



## Introduction

Texas Instruments developed the TMS320C6000 DSP architecture with performance and high level programming capability as key criteria. VLIW (Very Long Instruction Word) techniques are used to maximize parallelism and minimize overhead, which in turn maximize the performance capabilities of the architecture. The architecture was tuned to the C compiler. The DSP hardware and software development tools were developed jointly. TI's programming tools enable development teams to program in C, which reduces development time and enables software to be reused on multiple DSP VelociTI platforms.

The efficient optimizers in the tool set schedule code to match the intricacies of the highly parallel pipeline without requiring the programmer to understand the hardware architecture. Programming can be completed in reusable C or Assembly Language. Tools optimize the performance and schedule directly to the parallel pipeline.

The guidelines presented in this paper aim to:

- ☐ Reduce software development cycle time
- ☐ Reduce software development cost
- ☐ Increase software quality
- ☐ Achieve the software performance required by the application

To achieve these goals, the guidelines

- ☐ Enable the reuse of software assets through the use of ANSI C, ANSI C with TI C6000 Language Extensions, and TIC6000 Linear Assembly language on multiple DSP VelociTI chipsets
- ☐ Use an abstract yet more powerful language for programming (ANSI C and ANSI C with TI C6000 Language Extensions)
- ☐ Automate the tedious task of optimizing the code to the C6000 pipeline with the C and Linear Assembly optimizers
- ☐ Reducing errors (and rework) in coding and optimizing assembly code through the more abstract language and automation of tasks



## DSP Product Line Compatibility

The C6000 is compatible with the following five types of code:

- ❑ ANSI C code
- ❑ ANSI C code with TI C6000 Language Extensions
- ❑ TI TMS320C6000 Linear Assembly code
- ❑ Scheduled assembly code
- ❑ Object binaries

Beginning with the C6000 Instruction Set Architecture (ISA), Texas Instruments supports ANSI C, ANSI C with TI C6000 Language Extensions (including intrinsics), and a C6000 Linear Assembly Language that can all be reused on future C6000 platforms. The investment in code you write today can be reused on future C6000 DSPs.

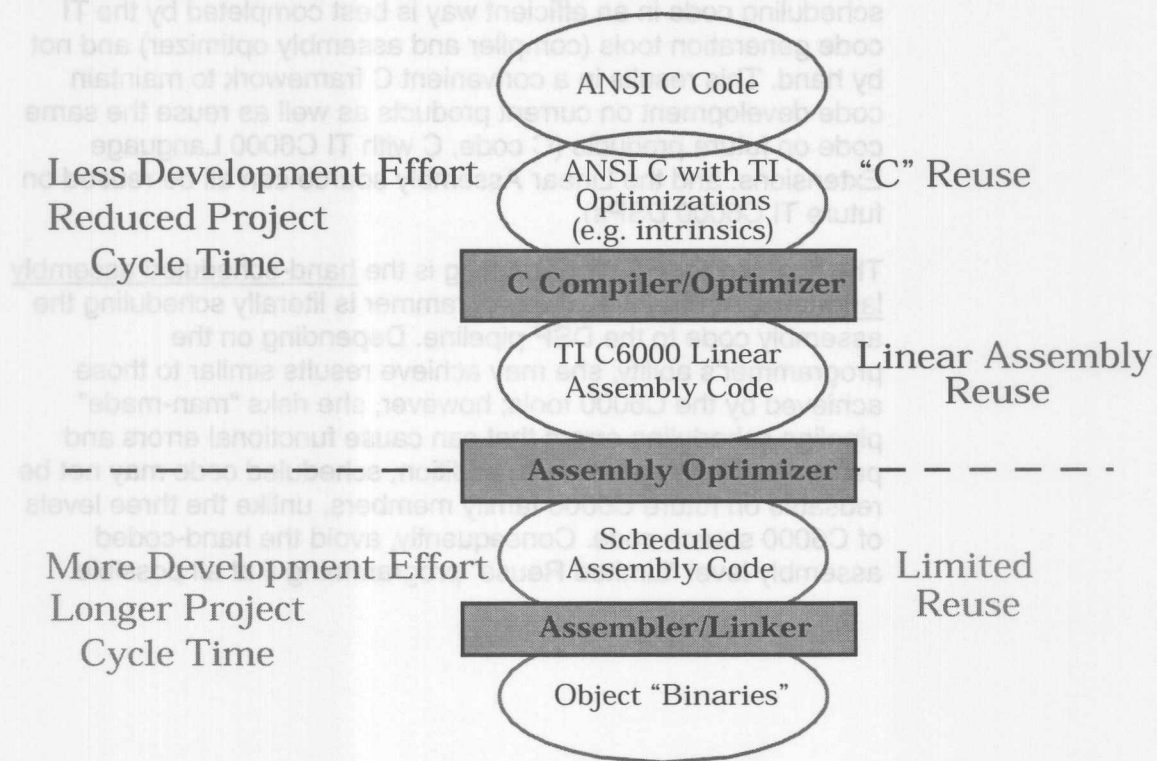
Figure 1 shows the three levels of source code for software development and reuse of software on the C6000:

- ❑ ANSI C
- ❑ ANSI C with TI C6000 Language Extensions (including intrinsics)
- ❑ TI C6000 Linear Assembly

ANSI C source code is an industry standard that can be input into the TI C compiler and compiled/optimized (see Figure 1). It is more abstract than assembly code and takes less programming resources. The TI compiler optimizes and schedules C code for the TI DSP. This offers many code development efficiencies but, in some specific cases (for example, tight loops) may not generate sufficient performance.



Figure 1. TMS320C6000 Code Reuse Efficiency Diagram



When additional performance or control needs addressing, the programmer can include TI Optimization Techniques (including C6000 Language Extensions) directly in the ANSI C code stream. TI Language Extensions are C functions that map directly to the C6000. This moves control of the code from the C compiler to the programmer. The combination of C and TI C6000 Language Extensions is a powerful combination for efficiently developing optimized and reusable software while maintaining direct control or literal performance tuning access.

**We highly recommend using C with TI C6000 Language Extensions as the software development language for TI C6000 software development.**

If more control is required to meet performance goals, another language, TIC6000 Linear Assembly, can be used. Linear Assembly is the C6000 machine instructions written in a serial, or linear, fashion with variable operands. The assembler optimizer takes the Linear Assembly as input and schedules the code for parallel pipeline of the DSP.



Because the C6000 is highly parallel and flexible, the task of scheduling code in an efficient way is best completed by the TI code generation tools (compiler and assembly optimizer) and not by hand. This results in a convenient C framework to maintain code development on current products as well as reuse the same code on future products (C code, C with TI C6000 Language Extensions, and the Linear Assembly source can all be reused on future TI C6000 DSPs).

The final territory of programming is the hand-scheduled assembly language. At this level, the programmer is literally scheduling the assembly code to the DSP pipeline. Depending on the programmer's ability, she may achieve results similar to those achieved by the C6000 tools; however, she risks "man-made" pipeline scheduling errors that can cause functional errors and performance degradation. In addition, scheduled code may not be reusable on future C6000 family members, unlike the three levels of C6000 source code. Consequently, avoid the hand-coded assembly level "Limited Reuse" programming if at all possible.

When additional performance or control needs addressing, the programmer can include TI Optimization Techniques (including C6000 Language Extensions) directly in the ANSI C code stream. TI Language Extensions are C functions that map directly to the C6000. This moves control of the code from the C compiler to the programmer. The combination of C and TI C6000 Language Extensions is a powerful combination for efficiently developing optimized and reusable software while maintaining direct control or literal performance tuning access.

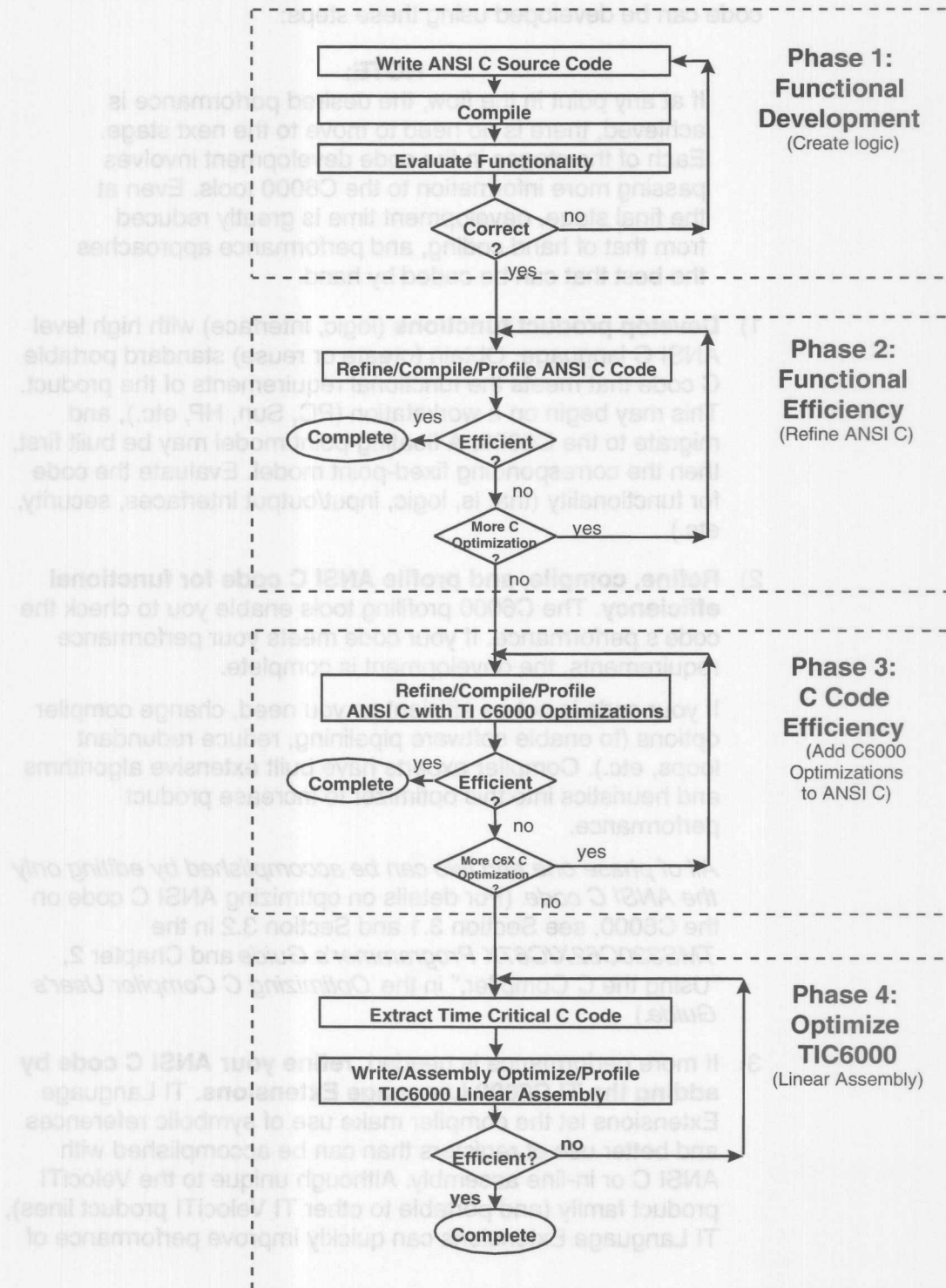
We highly recommend using C with TI C6000 Language Extensions as the software development language for TI C6000 software development.

If more control is required to meet performance goals, another language, TI C6000 Linear Assembly, can be used. Linear Assembly is the C6000 machine instructions written in a scalar, or linear, fashion with variable operands. The assembler optimizer takes the Linear Assembly as input and schedules the code for parallel pipeline of the DSP.



## Recommended DSP Software Development Flow

Figure 2. Recommended DSP Software Development Flow





Developing software code is one phase of the product development process. Understanding the product requirements and creating a high level design before coding ensures the product goals are understood and reduces rework during code development. When these phases are complete, the software code can be developed using these steps:

**NOTE:**

If at any point in the flow, the desired performance is achieved, there is no need to move to the next stage. Each of the stages in the code development involves passing more information to the C6000 tools. Even at the final stage, development time is greatly reduced from that of hand coding, and performance approaches the best that can be coded by hand.

- 1) **Develop product functions** (logic, interface) with high level ANSI C language. Obtain (create or reuse) standard portable C code that meets the functional requirements of the product. This may begin on a workstation (PC, Sun, HP, etc.), and migrate to the C6000. A floating-point model may be built first, then the corresponding fixed-point model. Evaluate the code for functionality (that is, logic, input/output interfaces, security, etc.).
- 2) **Refine, compile, and profile ANSI C code for functional efficiency.** The C6000 profiling tools enable you to check the code's performance. If your code meets your performance requirements, the development is complete.  
  
If your code is not as efficient as you need, change compiler options (to enable software pipelining, reduce redundant loops, etc.). Compiler experts have built extensive algorithms and heuristics into this optimizer to increase product performance.  
  
*All of phase one and two can be accomplished by editing only the ANSI C code.* (For details on optimizing ANSI C code on the C6000, see Section 3.1 and Section 3.2 in the *TMS320C62X/C67X Programmer's Guide* and Chapter 2, "Using the C Compiler," in the *Optimizing C Compiler User's Guide*.)
- 3) If more performance is needed, **refine your ANSI C code by adding the TI C6000 Language Extensions.** TI Language Extensions let the compiler make use of symbolic references and better use of registers than can be accomplished with ANSI C or in-line assembly. Although unique to the VelociTI product family (and portable to other TI VelociTI product lines), TI Language Extensions can quickly improve performance of



your C code. TI Language Extensions include the following examples:

- Saturated instructions Language Extensions (see Section 3.3.1 in the *TMS320C62X/C67X Programmer's Guide* for details).
- Unrolling the loop (expanding small loops so that each iteration of the loop appears in your code. This increases the number of instructions available to execute in parallel (see Section 3.3.3.4 in the *TMS320C62X/C67X Programmer's Guide* for more detail).
- Using word (int) access to read two short values at a time with Language Extensions to operate on the data. This can double the performance of some loops (for more information, see Section 3.3.2.1 in the *TMS320C62X/C67X Programmer's Guide* and Chapter 3, "Optimizing Your Code," in the *Optimizing C Compiler User's Guide*)

After applying these techniques, analyze your performance with optimizer options. If you meet your product's functional and performance requirements, your development is complete.

- 4) **Optimize the TIC6000 Linear Assembly code.** (Those who prefer to code in Linear Assembly begin here.)

If the required performance is not achieved after following these steps, write Linear Assembly by extracting the time-critical areas from your C code and rewriting the code in Linear Assembly.

Expert DSP assembly programmers may be able to achieve greater optimization than the tool; however, optimal implementations require exhaustive searches that machines can perform many times faster and generally are not portable to other DSP platforms. (For additional details, see Section 4, "Using the Assembler Optimizer," in the *Optimizing C Compiler User's Guide*.)



## Benefits

DSP software developers often jump into coding at the assembly language level at the project start without understanding either the product requirements or the alternative design solutions. Issues with product functions, performance, and interfaces with hardware are not resolved and cannot be reworked until found during testing.

At Texas Instruments we have developed a Product Development Process: requirements, high level design, and low level design phases are complete *before* linear assembly coding. Although these activities add time at the beginning of software development, they typically reduce overall cycle time by one-third to one-half. The final product arrives to market sooner.

In the design phase, the developer can use ANSI C to design the code. This enables the developer to work **in a more abstract and powerful language** than assembly language. The developer can focus on developing the product functions and algorithm instead of tuning the algorithm to the hardware platform. TI's compilers and optimizers translate C source code into the assembly code instructions. The programmer no longer needs to learn the intricate details of the C6000 architecture.

The code development may be complete at this point. If additional performance is required, the developer can add TI C6000 Language Extensions to the ANSI C before working at the assembly level. Because the developer has created fewer lines of C code than assembly for the same capability, less work was done, reducing product development cycle time and effort.

**Reuse:** Not just code but requirements and designs can be reused on other DSP products. This eliminates work and reduces product development time.

Code developed with TI tools in ANSI C, C with C6000 Language Extensions, or in TIC6000 Linear Assembly can be reused with future generations of the C6000 architecture family.



Figure 3. Software Development Cycle Time Results

| Software Development Process                         | Typical Software Development Cycle Time |                         |        |   |          |
|------------------------------------------------------|-----------------------------------------|-------------------------|--------|---|----------|
| Typical DSP Software Development                     | R                                       | Implement Assembly Code |        |   | Evaluate |
| Development With C and Linear Assembly Optimizations | R                                       | HLD                     | DD (C) | I | E        |
| Development With C                                   | R                                       | HLD                     | DD (C) | I | E        |
| Reuse (Requirements, Design, Code, Test Suites)      | R                                       | HLD                     | DD (C) | E |          |

**Legend:**

R Requirements

HLD High Level Design

DD Detail Design

I Implement

E Evaluate



## Appendix A. TI TMS320C6000 Optimiztion Checklist

| Feedback                                                                          | Solution                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Loop Carried Dependency Bound is much larger than Unpartitioned Resource Bound    | <p>C Code</p> <p>Use -pm program level optimization to reduce memory pointer aliasing (<i>Ref 3.2.2.2 in TMS320C62X/C67X Programmer's Guide</i>)</p> <p>Add const declarations to all pointers passed to a function that are read only (<i>Ref 3.2.2.1 in TMS320C62X/C67X Programmer's Guide</i>)</p> <p>Use -mt option to assume no memory pointer aliasing (<i>Ref 3.2.2 in TMS320C62X/C67X Programmer's Guide</i>)</p> <p>Linear Assembly</p> <p>Make sure instructions accessing memory at the beginning of the loop do not use the same pointer variables as instructions accessing memory at the end of the loop (<i>Ref 5.6.3 in TMS320C62X/C67X Programmer's Guide</i>)</p> |
| Partitioned Resource Bound is higher than Unpartitioned Resource Bound            | <p>Write code in Linear Assembly with partitioning/functional unit information (<i>Ref 5.3.4 in TMS320C62X/C67X Programmer's Guide</i>)</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| Too many instructions, or inefficient instructions were generated by the compiler | <p>Use intrinsics in C code to pick force more efficient C6000 instructions (<i>Ref 3.3.1 in TMS320C62X/C67X Programmer's Guide</i>)</p> <p>Write code in Linear Assembly to pick exact C6000 instruction to be executed (<i>Ref 4.3 in Optimizing C Compiler User's Guide</i>)</p>                                                                                                                                                                                                                                                                                                                                                                                                 |
| Failed to software pipeline due to Register live too long                         | <p>Write Linear Assembly and insert MV instructions to split register lifetimes that are live too long (<i>Ref 5.9.4.4 in TMS320C62X/C67X Programmer's Guide</i>)</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| Failed to software pipeline due to register allocation                            | <p>Try splitting the loop into two separate loops</p> <p>If multiple conditionals are used in the loop register allocation of the condition registers could be the reason for the failure. Try writing Linear Assembly and partition all instructions writing to a condition register evenly between the A and B sides of the machine. If there is an uneven number, put more on the B side as there are 3 condition registers on the B side and 2 on the A side.</p>                                                                                                                                                                                                               |



| Feedback                                                                               | Solution                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
|----------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| T address paths are Resource Bound                                                     | <p>C Code</p> <p>Use word access for short arrays – declare int * and use mpy Language Extensions to multiply upper and lower halves of registers (Ref 3.3.2 in TMS320C62X/C67X Programmer's Guide)</p> <p>Try to employ redundant load elimination technique if possible (Ref 5.10 in TMS320C62X/C67X Programmer's Guide)</p> <p>Linear Assembly</p> <p>Use LDW/STW instructions for accesses to memory (Ref 5.3 in TMS320C62X/C67X Programmer's Guide)</p> |
| There are memory bank conflicts (specified in the memory analysis window of simulator) | Write Linear Assembly and use the .mptr directive (Ref 5.11 in TMS320C62X/C67X Programmer's Guide)                                                                                                                                                                                                                                                                                                                                                           |
| Large outer loop overhead in nested loop                                               | <p>Unroll inner loop (Ref 3.3.3.4 and 5.8 in TMS320C62X/C67X Programmer's Guide)</p> <p>Make one loop with outer loop instructions conditional on an inner loop counter (Ref 5.13 in TMS320C62X/C67X Programmer's Guide)</p>                                                                                                                                                                                                                                 |
| Uneven resources (i.e., 3 multiplies per loop iteration)                               | Unroll loop to make even number of resources (Ref 5.8 in TMS320C62X/C67X Programmer's Guide)                                                                                                                                                                                                                                                                                                                                                                 |
| Two loops are generated, one not software pipelined.                                   | Use _nassert statement to specify loop count info (Ref 3.3.3.3 in TMS320C62X/C67X Programmer's Guide)                                                                                                                                                                                                                                                                                                                                                        |
| Loop will not software pipeline for other reasons                                      | <p>Make sure there are no function calls, branches to other code, or conditional break statements in loop (Ref 3.3.3.5 in TMS320C62X/C67X Programmer's Guide)</p> <p>Try making the loop counter downcounting (Ref 3.3.3.1 in TMS320C62X/C67X Programmer's Guide)</p> <p>Remove any modifications to the loop counter inside the loop (Ref 3.3.3.5 in TMS320C62X/C67X Programmer's Guide)</p>                                                                |



## Appendix B. Reuse libraries

One way to reduce development time is to avoid developing new code by reusing existing proven code. Texas Instruments continues to promote libraries.

The Texas Instruments TMS320 **Third Party Program** is the most extensive collection of Digital Signal Processing development support in the industry. Over 250 independent companies and consultants provide development boards, operating systems, software algorithms, function libraries, and system consulting services around the world. Types of applications include vocoders, speech recognition/ synthesis, audio, telecommunications, image/video, and run-time support libraries. For a current listing of available software, visit the world wide web at:

<http://www.ti.com/sc/docs/dsp/develop/freeman.htm>

The DSP North American Business Development organization is developing the following libraries:

- ❑ **General 6Cx kernels:** FFTs (block floating point, complex, Radix-2, Radix-4, real), FIRs (real block, single-sample, complex block, LMS adaptive), IIRs, vector manipulation (dot product, add, maximum), convolution encoder, and finite state machine
- ❑ **Math functions:** arithmetic (single-precision, double precision, 32-bit, pseudo-double precision), arctangent, auto-covariance, autocorrelation, convolution and correlation, convolution encoder, cross-correlation, cross covariance, log, matrix manipulation, trig functions
- ❑ **References to www freeware/shareware.** Software with unknown levels of quality control, including university software. Examples include: Vocoders (G.711, G.721 ADPCM, etc.), Parametric coders (CELP, G.728, etc.), Waveform coders (G.711, ITU G.726 ADPCM, etc.), Speech Recognition/Synthesis (Text-to-Speech, Speaker Independent, etc.), Audio (Karaoke, Graphic Equalizers, etc.), Control, Telecom (Acoustic Echo Canceller, Line Echo Canceller, etc.), Image (JPEG Still Image, H.324, etc.)

For additional information, contact your Texas Instruments field sales technical staff.



## Appendix C. References

- Texas Instruments, *TMS320C62x/C67x Programmer's Guide*  
<http://www-s.ti.com/sc/psheets/spru198b/spru198b.pdf>
- "C6x Code Optimization Checklist" by Richard Scales, pp 3-4 and 3-5,  
*TMS320C62x/C67x Programmer's Guide*  
<http://www-s.ti.com/sc/psheets/spru198b/spru198b.pdf>
- Texas Instruments, *TMS320Cx Optimizing C Compiler User's Guide*  
<http://www-s.ti.com/sc/psheets/spru187c/spru187c.pdf>



*Technical Brief:*  
**Designing Low-Power  
Applications with the  
TMS320LC54x**



# ***Designing Low-Power Applications with the TMS320LC54x***

---

---

***TECHNICAL BRIEF: (SPRA281)***

***Art Fischman/Patrick Rowland  
Digital Signal Processing Products  
Semiconductor Group***

***Texas Instruments  
August 7, 1997***



## IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain application using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

## Contents

### TRADEMARKS

|    |                                                               |
|----|---------------------------------------------------------------|
| 7  | Abstract                                                      |
| 8  | Introduction                                                  |
| 9  | Architectural Features of a Low-Power Design                  |
| 11 | System Design Considerations for Minimizing Power Dissipation |
| 14 | Total Power Dissipation                                       |
| 15 | LC54x Road Map                                                |
| 18 | Contents Of Power Dissipation Application Report              |
| 17 | Summary                                                       |

|    |                                                 |
|----|-------------------------------------------------|
| 12 | Figure 1. Algorithm current use vs. clock speed |
|----|-------------------------------------------------|

|    |                                                     |
|----|-----------------------------------------------------|
| 10 | Table 1. TM320LC54x Activity During Low Power Modes |
| 15 | Table 2. LC54x Low-Power High Performance Road Map  |

## Contents

|                                                                    |    |
|--------------------------------------------------------------------|----|
| Abstract.....                                                      | 7  |
| Introduction .....                                                 | 8  |
| Architectural Features of a Low-Power Design .....                 | 9  |
| System Design Considerations for Minimizing Power Dissipation..... | 11 |
| Total Power Dissipation .....                                      | 14 |
| LC54x Road Map .....                                               | 15 |
| Contents Of Power Dissipation Application Report .....             | 16 |
| Summary.....                                                       | 17 |

## Figures

|                                                       |    |
|-------------------------------------------------------|----|
| Figure 1. Algorithm current use vs. clock speed ..... | 12 |
|-------------------------------------------------------|----|

## Tables

|                                                            |    |
|------------------------------------------------------------|----|
| Table 1. TMS320LC54x Activity During Low Power Modes ..... | 10 |
| Table 2. LC54x Low-Power, High Performance Road Map.....   | 15 |

# Designing Low-Power Applications with the TMS320LC54x

## Abstract

This technical brief is an overview of the low power architectural features and design considerations of the TMS320LC54x DSP (Digital Signal Processor) family. For those with a deeper interest in low-power DSP design, this technical brief also provides an overview of a more detailed application brief titled, *Calculation of TMS320C54x Power Dissipation*, TI literature number SPRA164. The audience for this and the above referenced paper are designers of portable, power-sensitive, and battery-operated applications such as digital cellular telephones, laptop modems, and voice-mail pagers.



## Introduction

TI is the DSP of choice in low-power applications. One out of every two digital cellular phones shipped in the world has a TI DSP. This includes industry leaders like Nokia and Ericsson who rely on TI for their DSP solutions.

TI research and development in Dallas recently demonstrated the operation of a 1V DSP based off the C54x core. That is another reason why designers of low-power end-equipments look to TI, for their design solutions. With the C54x core, TI currently offers world-class, low-power, high-performance DSP solutions, and continued aggressive improvements in both power consumption and processing power are planned for the future. This is just one reason why TI is the leader in DSP Solutions.

This technical brief provides insight in the following areas:

- ❑ **Architectural Features of a Low-Power Design** - Describes key TMS320LC54x features designed to minimize power usage yet provide high performance.
- ❑ **System Design Considerations** - Summary of key areas critical to designing low-power applications.
- ❑ **Total Power Dissipation** - Overview of what the designer must consider when predicting power usage.
- ❑ **TMS320LC54x Road Map** - The future of TI low-power DSPs.
- ❑ **Summary of *Calculation of TMS320C54x Power Dissipation* Application Report** - For designers needing specific information on techniques for analyzing system and device conditions to determine operating current levels and device thermal management requirements.



## Architectural Features of a Low-Power Design

The TMS320C54x devices are a family of 16-bit fixed-point processors with enhanced processing capabilities over the previous fixed-point family of DSPs. Architecture, design, and process enhancements have produced a generation of processors which provide high performance while maintaining low power dissipation.

The TMS320C54x family of DSPs is capable of processing speeds as high as 100 million instructions per second (MIPS), sufficient to handle a wide variety of high-performance applications. In addition, the device is designed to exhibit very low power dissipation, and features flexible power management features which allow further reduction in power requirements.

These characteristics make the TMS320C54x devices uniquely well-suited to portable power-sensitive and battery-operated applications such as digital cellular telephones, laptop modems, voicemail pagers, etc.

Here are the key power-management features of the TMS320C54x:

- ❑ **CMOS technology** yields typical active current requirements of 0.45 mA per MIPS for 2.5-volt operation. The static CMOS technology used in fabrication of the TMS320C54x family of devices combines high density with low power dissipation. Because CMOS devices ideally draw current only when switching, this technology offers the potential for fully static devices with standby modes exhibiting very low current drain.
- ❑ **Flexible low-power modes** (IDLE instructions) conserve power by halting sections of the device when their use is not required. Operation of the CPU, the on-chip peripherals, and the clock generation circuitry can be halted independently. See Table 1 below for an overview of the low-power modes.
- ❑ **CLKOUT switching** allows the external CLKOUT signal to be stopped providing power savings when external clock synchronization is not necessary.
- ❑ **Bus holder circuitry** integrated into the device prevents floating buses, eliminating the need for power-wasting external pull-up resistors.



Table 1. TMS320LC54x Activity During Low-Power Modes

| Mode   | CPU | PLL | Timer | Standard Serial Ports | Buffered Serial port | Host Port Interface | CLKOUT |
|--------|-----|-----|-------|-----------------------|----------------------|---------------------|--------|
| Normal | •   | •   | •     | •                     | •                    | •                   | •      |
| IDLE1  |     | •   | •     | •                     | •                    | •                   | •      |
| Hold   |     | •   | •     | •                     | •                    | •                   | •      |
| IDLE2  |     | •   |       |                       | •                    | •                   |        |
| IDLE3  |     |     |       |                       | †                    | †                   |        |
| Stop   |     |     |       |                       | †                    | †                   |        |

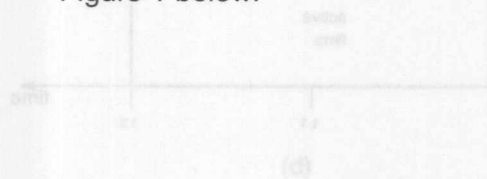
† - under special conditions



## System Design Considerations for Minimizing Power Dissipation

There are several issues that can be considered in the design process to reduce power consumption of a particular TMS320LC54x application:

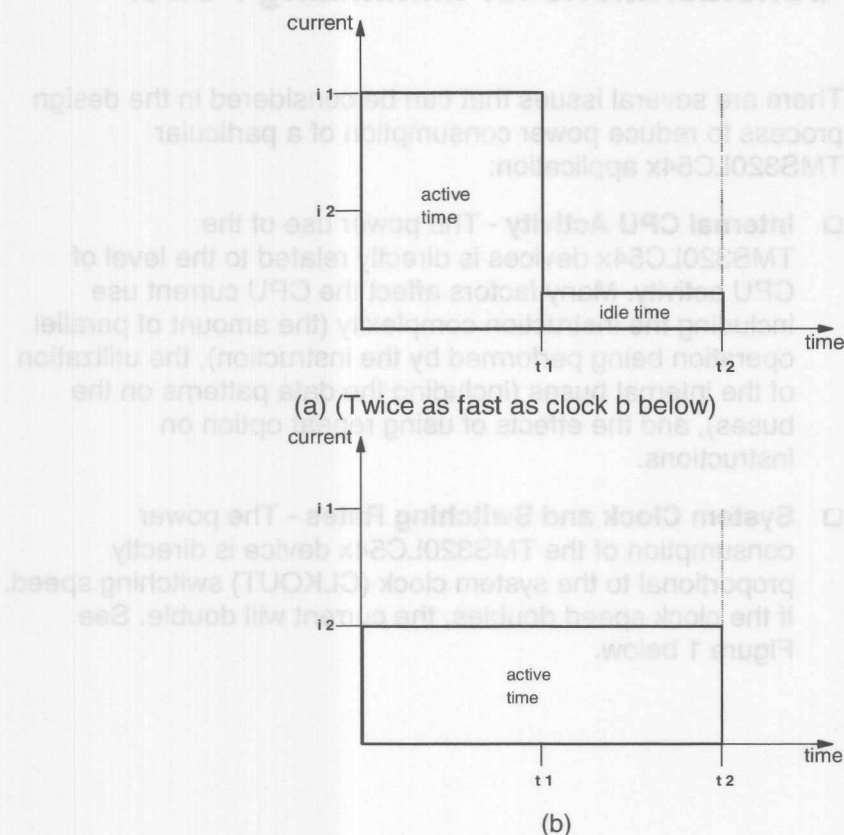
- ❑ **Internal CPU Activity** - The power use of the TMS320LC54x devices is directly related to the level of CPU activity. Many factors affect the CPU current use including the instruction complexity (the amount of parallel operation being performed by the instruction), the utilization of the internal buses (including the data patterns on the buses), and the effects of using repeat option on instructions.
- ❑ **System Clock and Switching Rates** - The power consumption of the TMS320LC54x device is directly proportional to the system clock (CLKOUT) switching speed. If the clock speed doubles, the current will double. See Figure 1 below.



- ❑ **On-chip vs. Off-chip Memory** - On-chip memory requires less power because the external memory interface is not driven during internal accesses.
- ❑ **On-chip ROM vs. on-chip RAM** - Use of internal ROM requires less power than use of internal RAM. Code execution from internal ROM requires about 10% less CPU current than the same code executing from internal SRAM.
- ❑ **Capacitive Loading of Outputs** - Increased capacitive loading on device outputs increases the current required to drive the output pins. Minimizing this loading will minimize the current required to operate these pins.
- ❑ **Address Visibility** - When address visibility is enabled, addresses are passed to the external address bus even during internal memory accesses. This feature is very useful primarily as a development and debugging tool, but it should be disabled when debugging is complete.



Figure 1. Algorithm current use vs. clock speed



- ❑ **On-chip vs. Off-chip Memory** - On-chip memory requires less power because the external memory interface is not driven during internal accesses.
- ❑ **On-chip ROM vs. on-chip RAM** - Use of internal ROM requires less power than use of internal RAM. Code execution from internal ROM requires about 10% less CPU current than the same code executing from internal SARAM.
- ❑ **Capacitive Loading of Outputs** - Increased capacitive loading on device outputs increases the current required to drive the output pins. Minimizing this loading will minimize the current required to operate these pins.
- ❑ **Address Visibility** - When address visibility is enabled, addresses are passed to the external address bus even during internal memory accesses. This feature is very useful primarily as a development and debugging tool, but it should be disabled when debugging is complete.



- ❑ **DC Loading of Outputs** - DC loading of outputs due to TTL or other sources should be minimized to conserve power.
- ❑ **Power-down Mode** - When device CPU activity is not necessary, the device should be placed in one of the IDLE modes to conserve power. See the TMS320LC54x Reference Set Volume 1 for more information.



## Total Power Dissipation

The total power consumption of the device is the sum of the individual components. This total current value is determined as the total current supplied to the device through all of the  $V_{DD}$  inputs.

Below is a summary of the steps used to calculate overall device power consumption. For a more detailed explanation, refer to the detailed TI application report *Calculation of TMS320C54x Power Dissipation*:

- 1) **Algorithm Partitioning** - The algorithm under consideration should be broken into sections of unique device activity and the power requirements for these sections calculated separately. The sections can then be time-averaged to determine the overall device current requirement. This includes IDLE time as Figure 1 demonstrates.
- 2) **CPU Activity** - The current contribution due to CPU activity can be determined by examining the code and determining the time-averaged current for each algorithm partition.
- 3) **Memory Usage** - Scale the current calculated in step 2 based on memory usage. Use of on-chip memory requires less current than off-chip memory (because of the additional current due to the external memory interface). Running code from internal ROM requires less current than running from internal RAM.
- 4) **Peripherals** - Consider the additional current required by use of the timer, standard serial port, buffered serial port, and host port interface.
- 5) **Current Due to Outputs** - Consider the current required by the algorithm to operate the external address and data buses.
- 6) **Calculation of Average Current** - If power supply current is observed over the full duration of device activity, different segments of activity will exhibit different current levels for different lengths of time.
- 7) **Effects of Temperature and Supply Voltage on Device Operating Current** - Include the effects of these factors after the total device current has been calculated.



## LC54x Road Map

One of the primary vectors for future DSP applications is that of low power. We see a wealth of portable devices such as cellular phones filtering into our everyday lives. Each, while demanding performance, also requires miserly power consumption for longer usage time between recharging. TI's low power vector in DSP enables many of today's applications as well as opening the door for tomorrow.

This can best be seen by looking at the C54x product roadmap presented below in Table 2.

*Table 2. LC54x Low-Power, High-Performance Road Map*

| MIPS | Node (process) | When placed in production | mA/MIPS | Core Voltage | mW/MIPS |
|------|----------------|---------------------------|---------|--------------|---------|
| 40   | 0.60um         | 1996                      | 1.00    | 3.0          | 3.00    |
| 50   | 0.45um         | 1996                      | 0.80    | 3.0          | 2.40    |
| 66   | 0.35um         | 1997                      | 0.65    | 3.0          | 1.95    |
| 80   | 0.35um         | 1997                      | 0.65    | 3.0          | 1.95    |
| 100  | 0.25um         | 1H98                      | 0.45    | 2.5          | 1.13    |

The proven success in the C54x family of DSPs in low power devices is also being fanned out to other families. In the microcontroller realm where increased performance coupled with low power are driving the high end of that market, the LC203 is introducing low power DSPs to cost-sensitive applications, and as the C2xx product family continues to mature, more low-power members will be introduced.



## Contents of Power Dissipation Application Report

For those with a deeper interest in low-power DSP design with the TMS320C54x, designers can download the detailed application brief titled, *Calculation of TMS320C54x Power Dissipation*, TI literature number SPRA164 from our web site ([www.ti.com](http://www.ti.com)). This application report describes in detail, techniques for analyzing system and device conditions to determine operating current levels.

From this analysis, power dissipation can in turn be used to determine device thermal management requirements. This application report contains:

- ☐ Detailed power testing set-ups
- ☐ Instruction set power characteristics
- ☐ Bus switching power considerations
- ☐ Detailed device internal power considerations
- ☐ Device interface power considerations
- ☐ The relationship between clock speed and current use
- ☐ Specific suggestions for minimizing power usage
- ☐ Thermal management



## Summary

By now it should be understood that the real-time processing of digital information is best handled by the engine designed specifically for the task, the DSP, a technology developed by Texas Instruments, Inc. Real-time, high-performance processing may seem like the antithesis of low power design, but it is not. The TMS320LC54x family of DSPs provides exceptionally high performance with much lower than expected power requirements. The future promises even faster, more efficient versions specifically optimized for portable, high-performance end equipment.



***Application Brief:***  
**TMS320C54x DSP**  
**Programming Environment**



# ***TMS320C54x DSP Programming Environment***

---

---

---

## ***APPLICATION BRIEF: SPRA182***

***M. Tim Grady  
Senior Member, Technical Staff  
Texas Instruments  
April 1997***



## IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain application using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated



## TRADEMARKS

TI is a trademark of Texas Instruments Incorporated.

Other brands and names are the property of their respective owners.

|                                            |    |
|--------------------------------------------|----|
| Abstract.....                              | 1  |
| 1. Introduction.....                       | 2  |
| 2. Basic Architecture.....                 | 3  |
| 3. Advantages of Multiple Buses.....       | 4  |
| 4. Special Instructions.....               | 5  |
| 5. Addressing Modes.....                   | 6  |
| 5.1 Immediate Addressing.....              | 6  |
| 5.2 Direct Addressing.....                 | 6  |
| 5.3 Indirect Addressing.....               | 7  |
| 5.4 Accessing Memory-Mapped Registers..... | 7  |
| 6. Pipeline.....                           | 8  |
| 6.1 Pipeline Conflicts.....                | 8  |
| 6.1.1 Resolved Conflict.....               | 9  |
| 7. Loops and Control Structures.....       | 11 |
| 8. Interrupts - Special Features.....      | 13 |
| 9. More on Special Instructions.....       | 14 |
| 10. Summary.....                           | 15 |

## Figures

|                                                        |   |
|--------------------------------------------------------|---|
| Figure 1. TMS320C54x block diagram.....                | 3 |
| Figure 2. Symmetric filter.....                        | 5 |
| Figure 3. The TMS320C54x pipeline.....                 | 8 |
| Figure 4. Auxiliary register updates.....              | 8 |
| Figure 5. Multiple buses avoid pipeline conflicts..... | 9 |
| Figure 6. Potential pipeline conflict.....             | 9 |

## Examples

|                                                             |   |
|-------------------------------------------------------------|---|
| Example 1. Direct addressing example.....                   | 6 |
| Example 2. Indirect addressing example (with indexing)..... | 7 |

## Contents

|                                              |           |
|----------------------------------------------|-----------|
| <b>Abstract.....</b>                         | <b>1</b>  |
| <b>1. Introduction.....</b>                  | <b>2</b>  |
| <b>2. Basic Architecture .....</b>           | <b>3</b>  |
| <b>3. Advantages of Multiple Buses .....</b> | <b>4</b>  |
| <b>4. Special Instructions.....</b>          | <b>5</b>  |
| <b>5. Addressing Modes.....</b>              | <b>6</b>  |
| 5.1 Immediate Addressing .....               | 6         |
| 5.2 Direct Addressing .....                  | 6         |
| 5.3 Indirect Addressing .....                | 7         |
| 5.4 Accessing Memory-Mapped Registers .....  | 7         |
| <b>6. Pipeline.....</b>                      | <b>8</b>  |
| 6.1 Pipeline Conflicts .....                 | 8         |
| 6.1.1 Resolved Conflict .....                | 9         |
| <b>7. Loops and Control Structures .....</b> | <b>11</b> |
| <b>8. Interrupts – Special Features.....</b> | <b>13</b> |
| <b>9. More on Special Instructions .....</b> | <b>14</b> |
| <b>10. Summary .....</b>                     | <b>15</b> |

## Figures

|                                                        |   |
|--------------------------------------------------------|---|
| Figure 1. TMS320C54x block diagram .....               | 3 |
| Figure 2. Symmetric filter .....                       | 5 |
| Figure 3. The TMS320C54x pipeline .....                | 8 |
| Figure 4. Auxiliary register updates .....             | 8 |
| Figure 5. Multiple buses avoid pipeline conflicts..... | 9 |
| Figure 6. Potential pipeline conflict.....             | 9 |

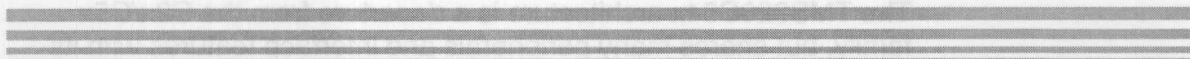
## Examples

|                                                               |   |
|---------------------------------------------------------------|---|
| Example 1. Direct addressing example: .....                   | 6 |
| Example 2. Indirect addressing example (with indexing): ..... | 7 |



The TMS320C54x DSP family began as the Low-Power Enhanced Architecture DSP (LEAD) project. The original goal was a fixed-point DSP for the cellular communications market. The need for a multi-mode design with special CPU elements such as two accumulators and dual addressing modes that support the design goals.

# TMS320C54x DSP Programming Environment



## Abstract

This document describes some of the programming techniques that may be used in different applications to take advantage of the full feature set of the TMS320C54x high-performance fixed-point DSP family.



## 1. Introduction

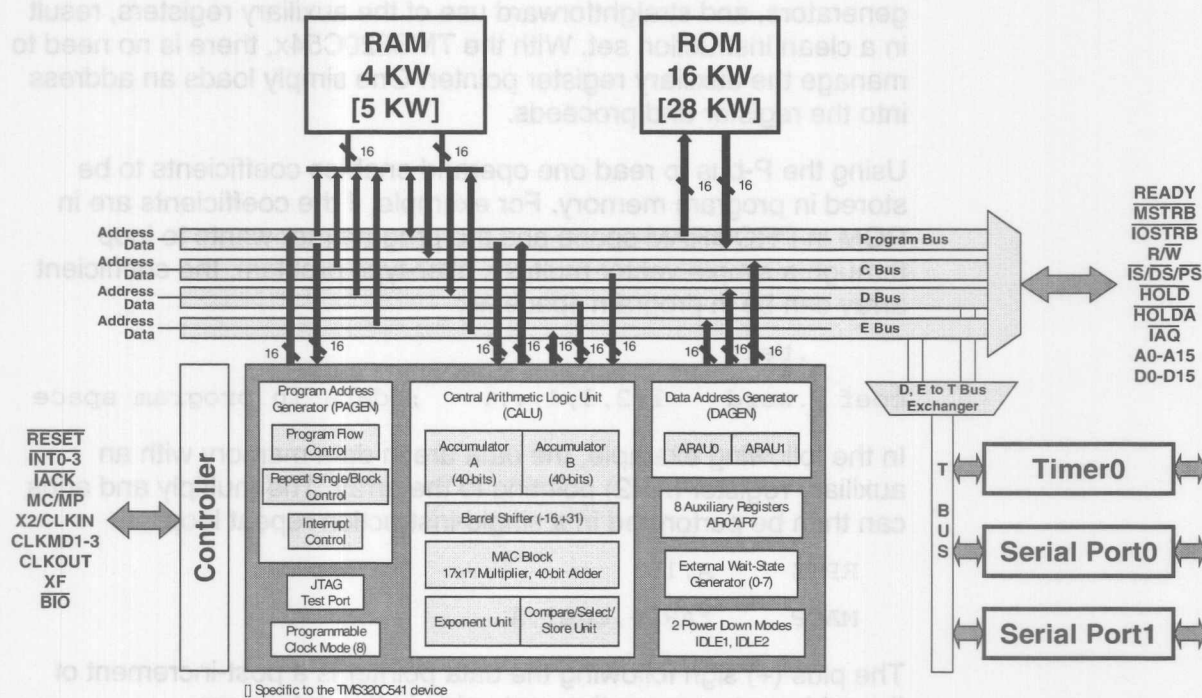
The TMS320C54x DSP family began as the Low-Power Enhanced Architecture DSP (LEAD) project. The project goal was a fixed-point DSP with power-saving characteristics well suited for the cellular telephone market. The result is a multi-bus design with special CPU features such as two accumulators and dual addressing modes that support the design goals.

The TMS320C54x architecture is a departure from the C2x/C5x family, but shares many peripherals and interface features with its cousins. The TMS320C54x User's Guide gives a detailed description of the architecture. This application brief discusses elements of the programming style used with this processor.

## 2. Basic Architecture

Many DSPs are based around a Harvard architecture with separate data and program memories and associated buses. The TMS320C54x devices share this feature, but additional data buses embellish the architecture and improve throughput. See Figure 1.

Figure 1. TMS320C54x block diagram



Internally, there are several buses:

- ❑ The P-Bus, used to fetch instructions from program memory, is also connected to the multiplier to provide an input from program memory.
- ❑ A dual data-bus scheme, the C-Bus and D-Bus, permits fetching two operands in the same cycle or a double word in one cycle.
- ❑ A separate output data bus, the E-Bus, allows simultaneous reads and writes in one parallel instruction.



### 3. Advantages of Multiple Buses

The dual data buses provide two address generators for fetching operands. These accesses are via the eight auxiliary registers (AR0 to AR7) by indirect addressing. For example, if AR2 points to a table of coefficients and AR3 points to a data array, the multiply can look like:

```
MPY *AR2, *AR3, A
```

This is a single-cycle instruction. Two buses, two address generators, and straightforward use of the auxiliary registers, result in a clean instruction set. With the TMS320C54x, there is no need to manage the auxiliary register pointer. One simply loads an address into the register and proceeds.

Using the P-bus to read one operand enables coefficients to be stored in program memory. For example, if the coefficients are in ROM in PROGRAM space and the programmer wants to loop through a simple vector multiply, filter-type problem, the coefficient array can be in program space as:

```
.text
coef .word 1,2,3,4,... ; data in program space
```

In the following example, the data are in data memory with an auxiliary register (AR2) pointing to the array. The multiply and adds can then be performed in a single-instruction repeat loop:

```
RPTZ A, 15
MACP *AR2+, coef, A
```

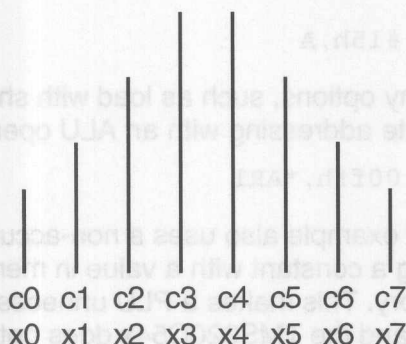
The plus (+) sign following the data pointer is a post-increment of the address to access the next value in the data array.

The plus sign for the coefficient is implied. The pointer to the address in the coefficient array is stored in a register in the program counter (PC) controller. Accessing the coefficient array automatically increments the pointer, so no symbol is used. The RPTZ instruction zeroes accumulator A and repeats the next instruction  $15 + 1 = 16$  times.

## 4. Special Instructions

Several instructions specific to the TMS320C54x improve device performance. For example, the FIRS, or symmetric FIR filter instruction uses the P-bus, both data buses and both accumulators. Figure 2 illustrates the filter with a set of symmetric coefficients.

Figure 2. Symmetric filter



In a typical FIR filter, the y values are the sum of the products:

$$y = (c0 * x0) + (c1 * x1) + (c2 * x2) + (c3 * x3) + (c4 * x4) + \dots + (c7 * x7)$$

Since this is a symmetric filter ( $c0=c7$ ,  $c1=c6$ , etc.) the equation can be simplified to:

$$y = c0*(x0 + x7) + c1*(x1 + x6) + c2*(x2 + x5) + c3*(x3 + x4)$$

The simplification results in half the number of multiplies.

The FIRS instruction uses the P-bus to point to the coefficients and the two data buses to point to the data pairs:

FIRS      \*AR2+, \*AR3+, coef

The FIRS instruction multiplies accumulator A by the value in the coefficient matrix and adds the result to accumulator B. At the same time, it adds the memory operands pointed to by auxiliary registers AR2 and AR3 and places the sum in accumulator A. Accumulator A must be pre-loaded with the first sum.

The TMS320C54x performs an N-tap symmetric FIR filter in  $N/2 + x$  cycles, where x is the overhead for setting up the loop. This is a big improvement over most DSPs, which require  $N + x$  cycles for the same operation. The TMS320C54x multiple buses, two accumulators, and special instruction hardware make this possible.

Later examples illustrate some of the other special instructions.



## 5. Addressing Modes

The TMS320C54x has immediate, direct (page + offset), and indirect addressing.

### 5.1 Immediate Addressing

Immediate is very simple; for example, to place 15h in accumulator A:

```
LD #15h,A
```

There are many options, such as load with shifts. Other instructions allow immediate addressing with an ALU operation, for example:

```
ANDM 00ffh,*AR1
```

This particular example also uses a non-accumulator destination; that is, ANDing a constant with a value in memory and placing the result in memory. This makes a PLU unnecessary for bit manipulation, and the TMS320C54x does not have one.

### 5.2 Direct Addressing

Direct addressing requires the use of a data page pointer (DP) and an offset into the 128-word page. While direct addressing has its uses, most algorithms use indirect addressing and the auxiliary registers.

*Example 1. Direct addressing example:*

```
.mmregs
.global x,y,Entry
.bss x,128,1 ; put "x" on single page

.sect "program"
LD #0,A ; zero accumulator A
LD #x,DP ; set DP to page with "x"
ADD #1,A,A ; add 1 to accumulator
STL A,@x ; store accumulator A at "x"
ADD #1,A,A
STL A,@x+128 ; Wrap back to start of same
 ; page
 ; (modulo 128)
```



## 5.3 Indirect Addressing

The indirect addressing modes of the TMS320C54x allow many options. For example, \*ARn simply accesses the value ARn points to. On the other hand, \*ARn+, \*ARn+0, and \*ARn+0% respectively, provide post-increment, post-increment with variable step size, and circular buffering. The TMS320C54x offers post-increment for reads and either pre- or post-increment for writes.

*Example 2. Indirect addressing example (with indexing):*

```
.mmregs
.global x,y,Entry
.bss x,128,1 ;put "x" on single page

.sect "program"
STM #2,AR0 ;set index value to 2.
; AR0 == index register
STM #x+126,AR1 ;start near end of page
; "x"
ADD #1,A,B
STL B,*AR1+ ;store at x+126
ADD #1,B,A
STL A,*AR1+0 ;store at AR1+2*(AR1+2)=A
ADD #1,A,B
STL B,*(#x+140) ;store at x+140
; (absolute address plus index)
```

## 5.4 Accessing Memory-Mapped Registers

The TMS320C54x has a Memory-Mapped Register file (MMR). All the peripheral control registers are memory mapped. Since the MMRs are all on Data Page Zero, special rules allow register access without first modifying the DP pointer. Typically, there is a one-cycle penalty for using an MMR as an operand; however, the one-cycle penalty is less than the overhead of managing the DP and the associated lines of code:

```
ADD DRR,0,A ;two-cycle instruction (DRR ==
; Serial Port data register)
ADD A,-8,B ;one-cycle instruction
ORM 0f0fh,SPC ;three-cycle instruction (SPC ==
; Serial Port Control register)
ORM 0f0fh,*AR4+ ;two-cycle instruction
```



## 6. Pipeline

The TMS320C54x has a six-level pipeline as shown in Figure 3. The pipeline provides very fast throughput, but requires some attention to detail in programming.

Figure 3. The TMS320C54x pipeline

| PF        | F     | D      | A      | R    | X       |
|-----------|-------|--------|--------|------|---------|
| Pre-Fetch | Fetch | Decode | Access | Read | Execute |

Most values change at the execution phase. Some changes occur at other times, such as auxiliary register (AR) updates during the access phase. This allows a sequence of instructions such as:

```
ADD *AR1+, A
MPY *AR1, #07h, B
```

The second instruction requires AR1 to have the updated value before its access phase. If AR1 were only updated at the execution phase of the first instruction, the second instruction would have to wait two cycles before its access phase could start. Two NOPs or other valid instructions would be required between the two instructions. However, since AR1 is updated during the access phase of the first instruction, the second instruction executes without difficulty or additional code (see below).

Figure 4. Auxiliary register updates

| ADD | D | A                 | R | X |
|-----|---|-------------------|---|---|
|     |   | AR1 modified here |   |   |
| MPY | D | A                 | R | X |
|     |   | New AR1 used here |   |   |

### 6.1 Pipeline Conflicts

The pipeline can be an issue in some operations. If both the C- and D-buses are in use on a dual operand instruction, which overlaps a previous instruction that accesses the E-bus at the same time, conflict may occur.

For the most part, however, conflicts are unlikely. The access phase for read occurs in the access phase of the pipeline, while the access phase for write occurs during the read phase of the pipeline. Further, the access for the D-bus occurs during only the first half of the cycle, while the access for the E-bus occurs during the second half of the cycle. So, even if two instructions overlap for the same cycle, conflict is minimized by the two address generators occurring in the same cycle.

The following example shows two instructions that avoid a pipeline conflict:

```
STL A, *AR3+ ; instruction 1
ADD *AR4, *AR5, A ; instruction 2
```

*Figure 5. Multiple buses avoid pipeline conflicts*

| Instruction 1 | A | R | X          |            |   |
|---------------|---|---|------------|------------|---|
|               |   |   |            | E-bus used |   |
| Instruction 2 |   | A | R          |            | X |
|               |   |   | C-bus used | D-bus used |   |

In the pipeline, the write to the E-bus occurs during the second half of the execute phase. The C-bus and the D-bus load during the second half of the access phase and the first half of the read phase, respectively.

### 6.1.1 Resolved Conflict

A conflict may occur if a write is followed by two dual-access reads, the second of which is from the same memory block as the write.

```
STL A, *AR3+
ADD AR4+, *AR5+, A
MPY AR2+, AR3, B
```

*Figure 6. Potential pipeline conflict*

| STL | A |        | R      |        | X      |        |        |  |   |  |
|-----|---|--------|--------|--------|--------|--------|--------|--|---|--|
|     |   |        |        | E Addr |        | E Data |        |  |   |  |
| ADD | D |        | A      |        | R      |        | X      |  |   |  |
|     |   | C Addr | D Addr | C Data | D Data |        |        |  |   |  |
| MPY |   |        | D      |        | A      |        | R      |  | X |  |
|     |   |        |        | C Addr | D Addr | C Data | D Data |  |   |  |



The conflict only occurs between the store instruction (STL) and the multiply instruction (MPY) if the accesses via the E-bus and C-bus are to the same block of memory. Otherwise, no conflict occurs.

If a conflict does occur, it is automatically resolved by the CPU delaying the write operation of the STL instruction to the execute phase of the ADD instruction. No extra cycles are inserted. If the data from the write operation is required before it is written to memory, it is read directly from an internal bus.

Figure 5. Multiple buses avoid pipeline conflicts

| Instruction 1 | Instruction 2 |     |     |     |
|---------------|---------------|-----|-----|-----|
|               | STL           | ADD | MPY | STL |
| Instruction 1 | STL           | ADD | MPY | STL |
| Instruction 2 | ADD           | MPY | STL | ADD |

In the pipeline, the write to the E-bus occurs during the second half of the execute phase. The C-bus and the D-bus load during the second half of the access phase and the first half of the read phase, respectively.

### 6.1.1 Resolved Conflict

A conflict may occur if a write is followed by two dual-access reads, the second of which is from the same memory block as the write.

STL     A, \*AR3+  
ADD     AR4+, \*AR2+, A  
MPY     AR2+, AR3, B

Figure 6. Potential pipeline conflict

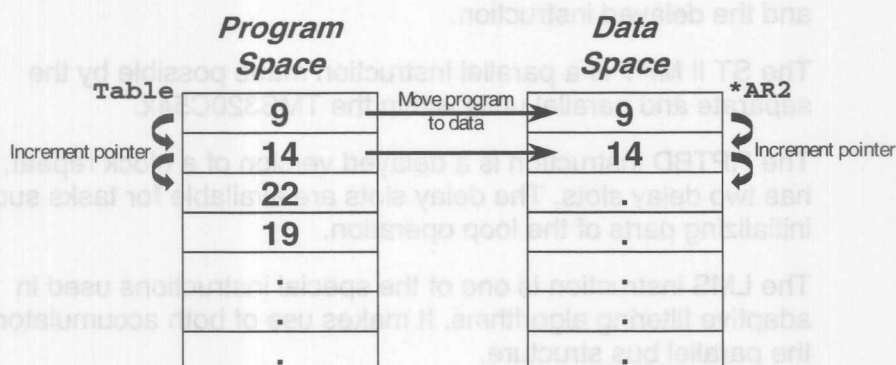
| Instruction 1 | Instruction 2 |     |     |     |
|---------------|---------------|-----|-----|-----|
|               | STL           | ADD | MPY | STL |
| Instruction 1 | STL           | ADD | MPY | STL |
| Instruction 2 | ADD           | MPY | STL | ADD |

## 7. Loops and Control Structures

The TMS320C54x has several loop-control mechanisms, including a repeat single and a repeat block. Both may be asserted at the same time, allowing nested loops. A single instruction may be repeated N times, as:

```
RPT #16-1 ;load repeat counter with 15
 ; for 16 iterations
MVPD #table,*AR2+ ; copy value from data list
 ;pointed to by table
```

Figure 7 – Moving values from program space to data space



This example also illustrates the move from program space to data space command. The pointer to Table is managed and automatically incremented by the program address generation (PAGEN) unit, so must be inside a repeat single. No instructions are fetched during a repeat single, which makes it a great candidate for use when fetching data from program space. In addition, the repeat single may not be interrupted.

A second version of the repeat single is the RPTZ, which first writes a zero to one of the accumulators. For example, to accumulate a sum of products into accumulator A, with N iterations:

```
RPTZ A, #N-1
MACP *AR2-%, Table, A
```

The repeat block command allows including a series of instructions in an automatic loop structure. The block repeat counter (BRC) must be loaded before beginning the loop. This may also be a delayed instruction with two delay slots:

```
STM #N-2, BRC ;initialize the Block
 ; repeat counter with Store MMR
LD ERROR,T ;initialize a variable
 ; called ERROR to 0
```



```
RPTBD END_LOOP-1 ;establish last line of
 ; loop
MPY *AR4,A ;delay slot instruction
 ; that initializes accumulator A
LMS *AR3,*AR4+0% ;2nd delay slot instruction
 ;loop starts here
ST A,*AR3+ ;save filter coefficient
|| MPY *AR4,A ;new term calculated
LMS *AR3,*AR4+0% ;LMS instruction for
 ; adaptive filter
 ; A = A + *AR3<<16 + 2^15
 ; B = B + *AR3 x *AR4
END_LOOP:
```

This example also illustrates two other ideas: the parallel instruction and the delayed instruction.

The ST || MPY is a parallel instruction made possible by the separate and parallel units within the TMS320C54x.

The RPTBD instruction is a delayed version of a block repeat, which has two delay slots. The delay slots are available for tasks such as initializing parts of the loop operation.

The LMS instruction is one of the special instructions used in adaptive filtering algorithms. It makes use of both accumulators and the parallel bus structure.

## 8. Interrupts – Special Features

The TMS320C54x device uses interrupts much like other DSPs and processors, but there are additional features. The TMS320C54x has four external interrupts and the usual assortment of internal interrupts including serial port, timer and traps. There are two interesting features of TMS320C54x interrupts: the way the vector table is built and a special fast interrupt feature.

The vector table occupies four words. Thus, when an interrupt is taken and the PC switches to the vector table, it is possible to have a traditional branch instruction such as:

```
BR ;1st entry
isr-1 ;2nd entry
not used ;3rd entry
not used ;4th entry
```

This results in two unused instructions. If, however, the first entry is a delayed return statement, the two delay slots could be used:

```
RETED ;1st entry
LDM DRR,A ;2nd entry, first delay slot
 ;3rd entry, 2nd delay slot.
 ;Note: MMRs take 2 cycles
not used ;4th entry not used because
 ; transfer has occurred
```

The RETE instruction requires five cycles, while the RETED takes three cycles and automatically re-enables the global interrupts. Using the four vector table slots is faster than the typical overhead of branching to an ISR and returning. An even faster method is to use the RETF instruction:

```
RETFD ; 1st entry
ADD 1, *AR4 ; 2nd delay slot
LD #5, ASM ; 3rd delay slot
not used ; 4th entry
```

The RETFD instruction takes only one cycle and speeds short interrupt routine handling. The interrupt latency for a fast interrupt is very low. Its speed is made possible by a special register in the PAGEN unit in which the return address is stored.



## 9. More on Special Instructions

Examples of the FIRS instruction and the LMS instruction are shown earlier in this article. Several other special instructions are supported by hardware, including a series of double add and double subtract instructions which, combined with the Compare, Select and Store instruction (CMPS), provide excellent throughput on algorithms such as the Viterbi decoder.

A concept in Viterbi decoding is to compare two metrics to determine and store the larger distance. In addition, a record of which metric was stored is required. The TMS320C54x CMPS unit performs this function.

With either accumulator as an input, the CMPS compares the two halves and writes one to memory. It also updates the transition (TRN) register by shifting the contents to the left one place and ORing in a new value (either 1 or 0, depending on which half is updated).

The accumulator used as input to the CMPS has two 16-bit values calculated by two parallel adds or subtracts. A value is placed in the T register, and the AR register points to a double word. Half the double word is either ADDED or SUBtracted from the T register and the two results are stored in the 32-bit accumulator.

For example:

```
STM #2-1, BRC ;initialize repeat counter
RPTBD end-1 ;begin repeat block
LD *AR7,T ;initialize T in delay slot
NOP ;second delay slot
DADST *AR5, A ;A(h) = OLDValue[i] + T
 ;A(l) = OLDValue[j] - T
 ;DADST means double add and subtract
DSADT *AR5+,B ;B(h) = OLDValue[i] - T
 ;B(l) = OLDValue[j] + T
 ;DSADT means double subtract and add
CMPS A,*AR4+% ;Write one-half of A to
 ;memory and update TRN
CMPS B,*AR3+% ;Write one-half of B to
 ;memory and update TRN
```

While not a complete algorithm, this segment illustrates the use of some of the special instructions. All the instructions shown are single-cycle instructions.

---

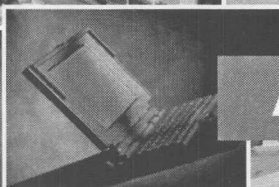
## 10. Summary

The TMS320C54x device is a fast, low-power fixed-point machine with performance enhancements. It features dual data buses and dual address generators to fetch dual operands or double words in one cycle. Two accumulators and hardware support double adds and/or subtracts. The P-bus is used to fetch instruction words, but may also be an input to the multiplier. This simplifies several instructions that use data buses for operands and the program bus for a third operand.

The TMS320C54x includes a compare, select and store unit, which improves the performance of GSM and Viterbi algorithms. Hardware support for special instructions such as the LMS instruction used in adaptive filter algorithms, further enhance the device.

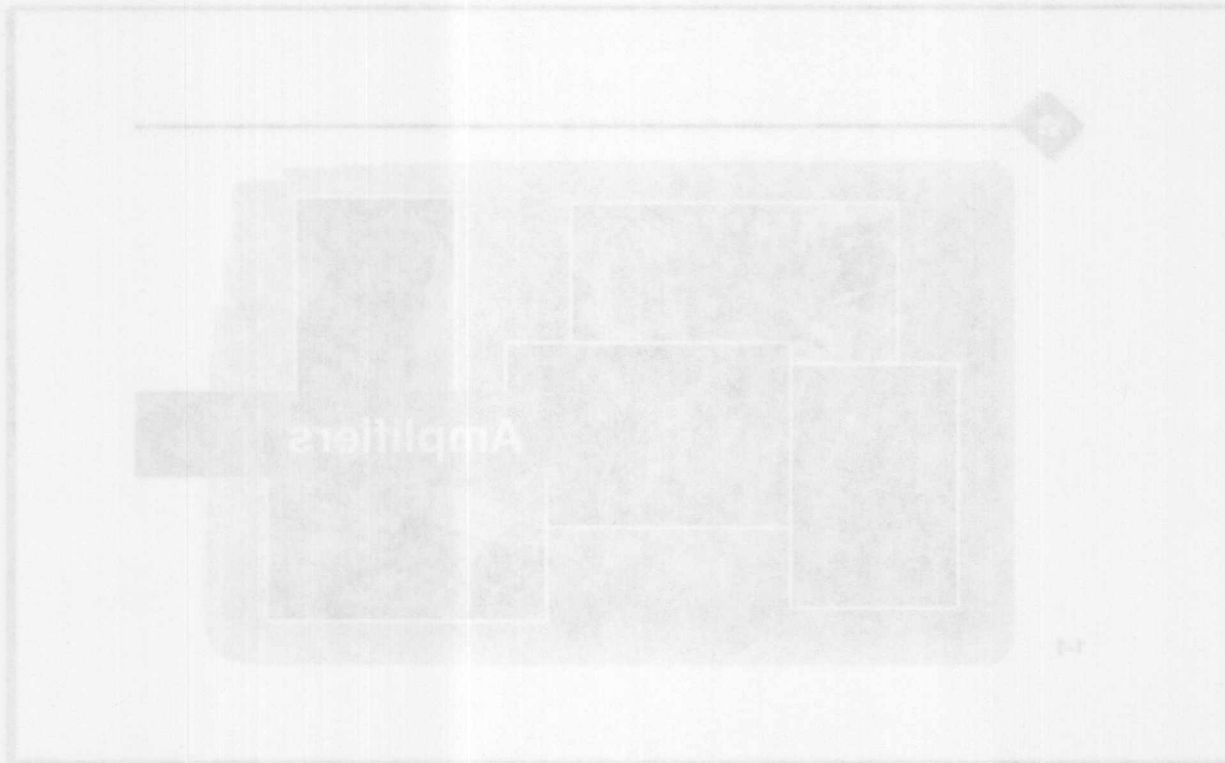
The TMS320C54x may also be used as a DSP in non-telecom applications. The loop control structures, addressing modes, and fast interrupt features enable fast, compact code.





## **Amplifiers**

1-1



## Table of Contents

|                                                                    |           |
|--------------------------------------------------------------------|-----------|
| <b>Signal Conditioning – Amplifiers .....</b>                      | <b>5</b>  |
| <b>Operational Amplifiers .....</b>                                | <b>6</b>  |
| How Do I Select Op Amps? Practical Considerations .....            | 6         |
| Low Noise Operational Amplifier Selection Guide.....               | 17        |
| Precision Op Amp Selection Guide .....                             | 19        |
| Design Considerations Migrating from Dual to Single Supplies ..... | 20        |
| <b>Evaluating Operational Amplifiers.....</b>                      | <b>34</b> |
| Universal Op Amp EVM Description.....                              | 34        |
| Universal Op Amp EVM - Accelerometer Application .....             | 36        |
| Accelerometer System Diagram.....                                  | 37        |
| Sensor Signal Conditioning .....                                   | 38        |
| <b>High Speed Amplifiers .....</b>                                 | <b>40</b> |
| What is a high speed amplifier?.....                               | 40        |
| What parameters are important? .....                               | 41        |
| Where do you use high speed amplifiers? .....                      | 43        |
| Amplifier Architectures.....                                       | 44        |
| Voltage feedback .....                                             | 46        |
| Current feedback .....                                             | 48        |
| <b>Audio Power Amplifiers .....</b>                                | <b>51</b> |
| Integrated Class-D Power Amplifier .....                           | 56        |
| Class-D Amplifier Efficiency.....                                  | 58        |
| Audio Power Amplifier Selection Chart.....                         | 69        |
| <b>Conclusion .....</b>                                            | <b>70</b> |
| <b>Reference Material.....</b>                                     | <b>71</b> |
| Input Stage Considerations .....                                   | 71        |
| Output Stage Considerations.....                                   | 78        |
| DC-Considerations of Operational Amplifiers .....                  | 86        |
| AC-Considerations of Operational Amplifiers .....                  | 103       |
| Device Ratings.....                                                | 116       |

## Table of Contents

|                                                                  |     |
|------------------------------------------------------------------|-----|
| Signal Conditioning - Amplifiers .....                           | 5   |
| Operational Amplifiers .....                                     | 5   |
| How Do I Select Op Amps? Practical Considerations .....          | 6   |
| Low Noise Operational Amplifier Selection Guide .....            | 13  |
| Precision Op Amp Selection Guide .....                           | 19  |
| Design Considerations Migrating from Dual to Single Supply ..... | 20  |
| Evaluating Operational Amplifiers .....                          | 24  |
| Universal Op Amp EVM Description .....                           | 34  |
| Universal Op Amp EVM - Accelerometer Application .....           | 38  |
| Accelerometer System Diagram .....                               | 37  |
| Sensor Signal Conditioning .....                                 | 38  |
| High Speed Amplifiers .....                                      | 40  |
| What is a high speed amplifier? .....                            | 40  |
| What parameters are important? .....                             | 41  |
| When do you use high speed amplifiers? .....                     | 43  |
| Amplifier Architectures .....                                    | 44  |
| Voltage feedback .....                                           | 45  |
| Current feedback .....                                           | 45  |
| Audio Power Amplifiers .....                                     | 51  |
| Integrated Class-D Power Amplifier .....                         | 55  |
| Class-D Amplifier Efficiency .....                               | 58  |
| Audio Power Amplifier Selection Chart .....                      | 59  |
| Conclusion .....                                                 | 70  |
| Reference Material .....                                         | 71  |
| Input Stage Considerations .....                                 | 71  |
| Output Stage Considerations .....                                | 75  |
| DC-Considerations of Operational Amplifiers .....                | 85  |
| AC-Considerations of Operational Amplifiers .....                | 103 |
| Device Ratings .....                                             | 115 |

## Signal Conditioning – Amplifiers

In the era of digital signal processing, capturing analog “real world” information and conditioning it for digital manipulation presents challenges to engineers less familiar with analog system design. Furthermore, preparing analog signals for conversion to digital data and recreating them from such data involves taking special care of details of little concern in traditional all-analog systems.

This section will address the concerns of signal conditioning for input and output signals. Specifically we will discuss the choice and use of amplifiers. The amplifiers discussed will include operational amplifiers, high speed operational amplifiers and audio power amplifiers.

- Choosing the best op amp for a specific application.
- Choosing between single and dual supply operation.
- Evaluating op amp circuits quickly even with surface mount components.

Additional reference material is provided on AC and DC characteristics, input - output considerations and data sheet specifications.

### How Do I Select Op Amps? Practical Considerations

An op amp is an integral part of just about any signal chain. Ironically, the op amp has near standard pin-configuration, although there is no consistency of specifications from one manufacturer to the next, or even from one amplifier to the next by a given manufacturer. So which op amp are you going to use in your application? How do you take the hundreds of available op amps and select the one that will fit the criteria of your application the best. It may seem to be a daunting task, but it doesn't have to be. Armed with a basic understanding of the fundamental characteristics of the op amp and the inherent tradeoffs within the manufacturing processes of the device, a stepwise approach can quickly narrow the choices for a given application down to a manageable few.

## **Operational Amplifiers**

Operational amplifiers (Op Amps) are the general purpose work horse of the signal conditioning world. Op Amps are used to build amplifiers, filters, to match impedances, to increase drive capabilities and numerous other functions associated with conditioning input and output signals.

The basic functionality of all op amps are very similar with variations in performance, special features, and packaging. The questions then become why are hundreds of different op amps available? What are the differences? How do I choose?

The following sections will address practical considerations such as:

- Choosing the best op amp for a specific application.
- Choosing between single and dual supply operation.
- Evaluating op amp circuits quickly even with surface mount components.

Additional reference material is provided on AC and DC characteristics, input - output considerations and data sheet specifications.

### **How Do I Select Op Amps? Practical Considerations**

An op amp is an integral part of just about any signal chain. Ironically, the op amp has near standard pin-configuration, although there is no consistency of specifications from one manufacturer to the next, or even from one amplifier to the next by a given manufacturer. So which op amp are you going to use in your application? How do you take the hundreds of available op amps and select the one that will fit the criteria of your application the best. It may seem to be a daunting task, but it doesn't have to be. Armed with a basic understanding of the fundamental characteristics of the op amp and the inherent tradeoffs within the manufacturing processes of the device, a stepwise approach can quickly narrow the choices for a given application down to a manageable few.



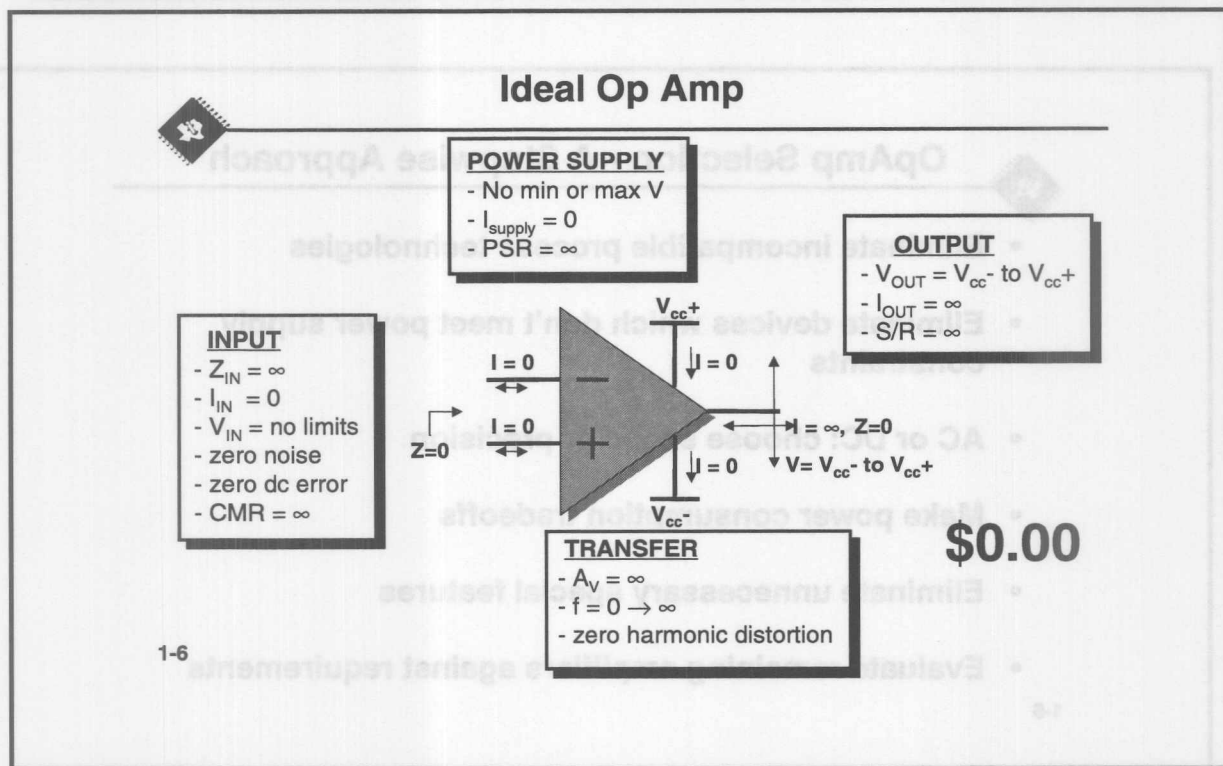
## **OpAmp Selection - A Stepwise Approach**

- **Eliminate incompatible process technologies**
- **Eliminate devices which don't meet power supply constraints**
- **AC or DC: choose speed or precision**
- **Make power consumption tradeoffs**
- **Eliminate unnecessary special features**
- **Evaluate remaining amplifiers against requirements**

1-5

### **Op Amp Selection a Stepwise Approach**

First, eliminate incompatible process technologies. Then, eliminate devices which don't meet the power supply constraints of the application. Next, determine whether the application is ac or dc and understand the inherent power consumption tradeoffs that will come with the increased ac performance. Then eliminate any devices with unnecessary special features. Lastly, evaluate the remaining amplifiers against the requirements of the application. This section will address each of these steps in more detail.



## The Ideal Op Amp Characteristics

Before examining the advantages and disadvantages inherent to amplifiers manufactured in the various fabrication technologies commonly used today, it may be helpful first to review the basic characteristics of an "ideal" op amp. And, it is convenient to group the characteristics into four categories: input characteristics, output characteristics, power supply characteristics, and transfer characteristics. These are the four basic facilities for evaluation in selecting a device for a given application as well.

Let's start with the input characteristics. The ideal op amp would have infinite input impedance and no input bias currents causing no loading on the signal source. It would have infinite input differential as well as common mode voltage making no constraints on the properties of the input signal. There would be perfect matching of the input transistors leading to no dc input offset voltage, and there would be no noise sources with no noise voltage or current generated by the op amp.

Moving to the output characteristics, the ideal op amp would be able to source or sink in infinite amount of current with a rail to rail output swing with an infinite step response (no slew rate limitations) into any resistive, capacitive, or inductive load.

As to the characteristics of the power supply, there would be no minimum voltage requirement, nor a maximum voltage limit. The device would consume no power, dissipate no power and it would work in split- and single-supply systems. For the transfer characteristics, the ideal op amp would have infinite open-loop gain and run at any frequency with no distortion. And the most important aspect to any designer, or at least purchaser, it would be absolutely free.

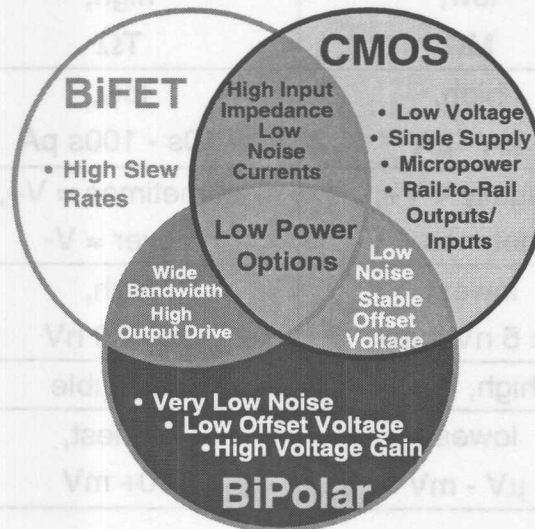
Of course, no op amp exhibits any of these characteristics, but an understanding of them will enable the designer to narrow his choices for further evaluation.

|                     | <b>bipolar</b>                                 | <b>biFET</b>                                             | <b>CMOS</b>                                                         |
|---------------------|------------------------------------------------|----------------------------------------------------------|---------------------------------------------------------------------|
| <b>inputs</b>       |                                                |                                                          |                                                                     |
| $Z_{IN}$            | low,<br>$M\Omega$                              | high,<br>$T\Omega$                                       | high,<br>$T\Omega$                                                  |
| $I_{IN}$            | high,<br>$nA - \mu A$                          | low,<br>$10s - 100s\ pA$                                 | low,<br>$pA$                                                        |
| $V_{IN}$            | usually $< V_{+}$ ,<br>sometimes $= V_{-}$     | sometimes $= V_{+}$ ,<br>never $= V_{-}$                 | sometimes $= V_{+}$ ,<br>always $= V_{-}$                           |
| $V_N$               | lowest,<br>$< 5\ nV$ avail                     | high,<br>$20 - 80\ nV$                                   | some low,<br>$10 - 100\ nV$                                         |
| $I_N$               | high, $f(I_N)$                                 | negligible                                               | negligible                                                          |
| $V_{IO}$            | lowest,<br>$\mu V - mV$                        | highest,<br>$10+ mV$                                     | varies,<br>$100s\ \mu V - mV$                                       |
| <b>outputs</b>      |                                                |                                                          |                                                                     |
| $V_O$               | usually $< V_{+}$ ,<br>sometimes $= V_{-}$     | never $= V_{+}$ ,<br>never $= V_{-}$                     | sometimes $= V_{+}$ ,<br>always $= V_{-}$                           |
| $I_O$               | good,<br>$10 - 100\ mA$                        | good,<br>$10 - 100\ mA$                                  | low,<br>$100s\ \mu A - 10s\ mA$                                     |
| SR                  | poor to fair,<br>$V/ms - 10\ V/\mu s$          | good,<br>$10s\ V/\mu s$                                  | poor to fair,<br>$V/ms - < 5\ V/\mu s$                              |
| <b>power supply</b> |                                                |                                                          |                                                                     |
| $V_{CC}$            | some 3V<br>some single supply<br>$40+ V_{max}$ | min $\pm 3.5V$<br>no single supply<br>$36 - 40+ V_{max}$ | low voltage $< 3V$<br>all single supply<br>$V_{max}$ limited 5-18 V |
| $I_{CC}$            | med to high,<br>$100s\ \mu A - 10\ mA$         | med to high,<br>$100s\ \mu A - 3\ mA$                    | $\mu$ power to avg,<br>$\mu A, 10s\ \mu A, 100s\ \mu A$             |
| <b>transfer</b>     |                                                |                                                          |                                                                     |
| BW                  | dc - $\sim 5\ MHz$                             | dc - $10+ MHz$                                           | dc - $2\ MHz$                                                       |

### Relative Process Performance

This chart provides a relative indication of various amplifier performance by various technologies. These values are given as guidelines with the knowledge that in specific instances these values are exceeded.

## Process Tradeoffs



1-7

## Process Technology Tradeoffs

As stated earlier, there are three processes in which most of today's op amps can be categorized: bipolar, biFET, and CMOS. There are inherent tradeoffs within each process which facilitates a natural method for eliminating broad classes of devices, significantly narrowing the designer's choices.

In the bipolar process, an op amp will generally have low voltage noise and the lowest input offset voltage of the three families. The device will have pretty good bandwidth with a fair amount of output drive. However, to achieve this precision, some tradeoffs are made. A bipolar device has low input impedance, high current noise and generally consume a large amount of current from the power supply.

In the biFET process, an op amp will generally have high input impedance and low input bias currents. It will provide pretty good output drive with exceptional slew rate and bandwidth. However, again, other characteristics are sacrificed for these advantages. A biFET device will have high voltage noise and demonstrate the highest input offset voltage. There are constraints on the power supply and they consume a fairly large amount of current.

As for op amps fabricated in the CMOS process, they exhibit the highest input impedance and lowest input bias current of the three classifications. They have the widest input and output voltage ranges with respect to the supply rails and they are micropower devices. Conversely they have poor output drive, poor to fair slew rates and low bandwidths.

It should be noted these are not to be taken as absolutes. Process limits can be exploited and design techniques used to extend process capabilities. But beware of the tradeoffs necessary for the additional advantages .

## Power Supply Constraints

### ■ CMOS

- - Lower voltage systems
- $V_{CC} < \sim 18V$  often lower

### ■ BiFET -

- Dual- supply operation
- Not for  $V_{CC} < \pm 3.5V$ .

### ■ Bipolar -

- Normally higher voltages  $\sim 40V$
- Some for single-supply operation

1-11

## Power Supply Constraints

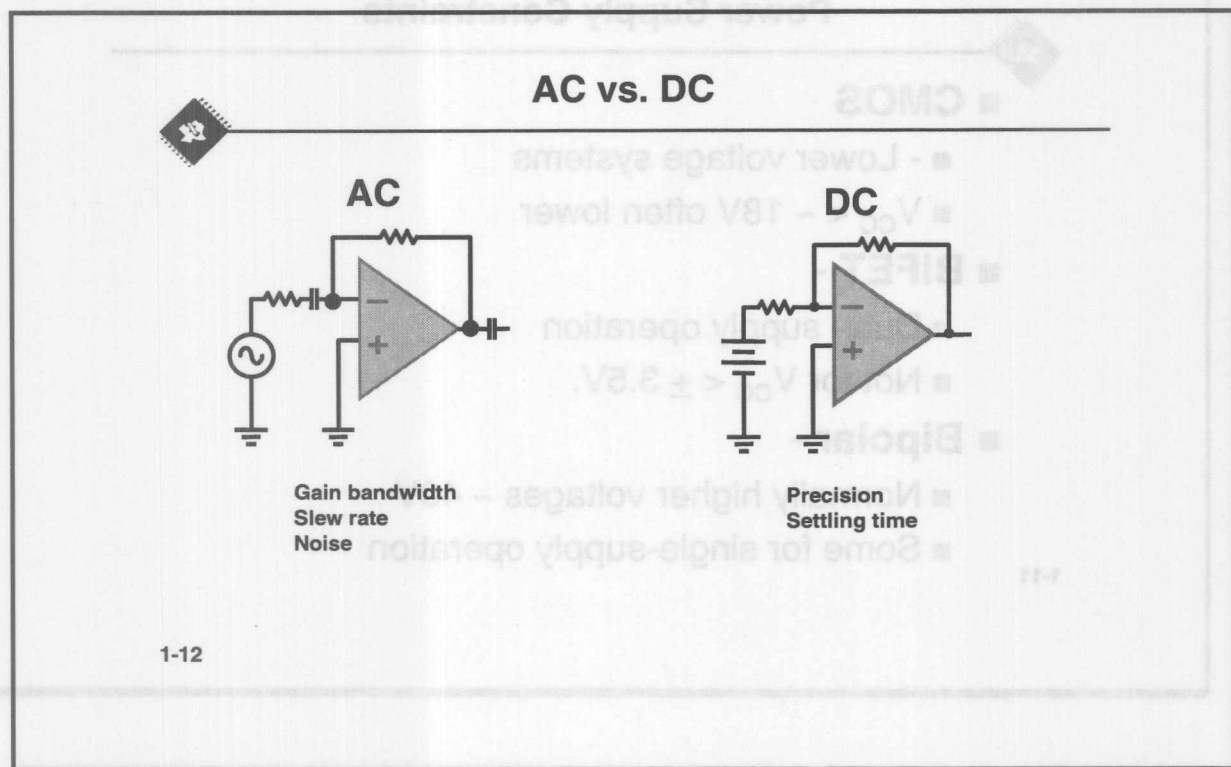
Armed with this basic understanding of process-related strengths and weaknesses, the easiest first cut against available amplifiers is made based on power supply voltage, minimum or maximum. Some conclusions can be made by considering the supply voltage characteristics as previously stated:

CMOS amplifiers are not suited for higher-voltage systems. The maximum supply voltage is generally around 18V and in many cases even as low as 7V. CMOS op amps are well-suited for single-supply, low-voltage systems.

BiFET op amps will not work in low voltage systems. If your system is less than  $\pm 3.5V$ , a BiFET op amp is a choice. The input common mode voltage is 3.5V from the top supply rail to 3.5V from the bottom supply rail. Even with the smallest signal, the op amp is useless with a supply range of less than 7V. Of course, some BiFETs are better than others but this is generally true. They are not designed for single-supply systems. However, they can be used if the supply voltage is adequate and careful attention is paid to signal and load referencing.

Bipolar op amps are the most forgiving when it comes to power supply requirements. The bipolar process is generally capable of higher voltages, usually around 40V, and some can even be used in single supply systems. However, they generally have lower common mode input voltage ranges than a CMOS device which would generally be the more logical place to start looking unless other characteristics were more critical. By eliminating or focusing on one or more technologies, you not only remove hundreds of amplifiers from contention, but frequently also limit the number of manufacturers you

consider. Many manufacturers offer only bipolar amplifiers; a select few are prolific in CMOS; and biFETs are similarly distributed.



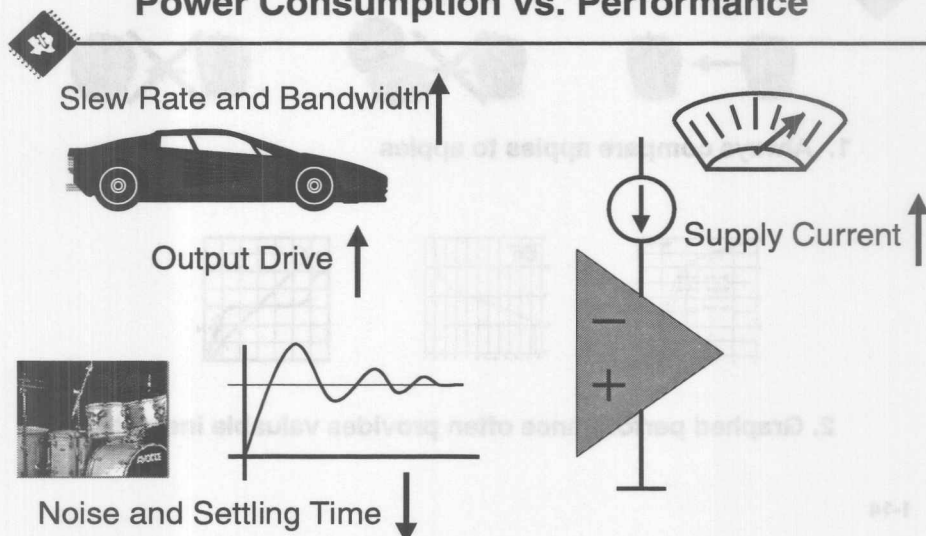
## Signal Characteristics AC vs DC.

Another guide for choosing an amplifier for a given sub-circuit is to classify that circuit as primarily ac or dc. In a dc system, the signals are generally slow moving and typically require little bandwidth. Unless there is a step function, slew rate and settling time are also of lesser importance. In an ac circuit the signal places significant requirements on gain-bandwidth and slew rate, whereas dc precision is generally unimportant. A signal which is ac-coupled does not require a precision grade op-amp; however a dc-coupled ac signal may.

Obviously, small signals require higher-precision amplifiers. Precision and low noise become especially critical in digital systems as the number of bits of resolution increases. A designer of a mixed signal application will have an error budget essential to the performance of his system. As a fellow application engineer has stated to me on several occasions, you can't run a Cadillac engine with a Yugo front end. The op amp conditioning the source signal for the A to D must have less error than the resolution of that A to D, or that resolution is decreased.

AC performance comes with tradeoffs, not the least of which is power consumption. In fact, power consumption frequently becomes the pivotal parameter in finalizing op amp selection, especially in the ever-growing market of battery powered applications.

## Power Consumption vs. Performance



1-13

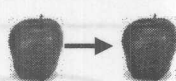
### Power Consumption vs. Performance

Engineers often find themselves having to make difficult decisions trading power consumption for required performance. There are some first-order relationships that drive these decisions.

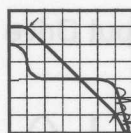
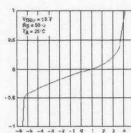
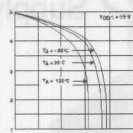
AC performance such as slew rate, bandwidth, and settling time come at the expense of increased power consumption. The noise figure varies inversely to the first stage current; so to achieve a lower noise op amp, higher supply current must be sacrificed. Also, in many families of amplifiers, output drive is proportional to the supply current as well.

Frequently manufacturers offer two or more power options of the same op amp. Making the judicious tradeoffs between lowest power and required ac performance, noise, or output drive is often among the most important decisions a designer must make.

## The Final Cut



### 1. Always compare apples to apples



### 2. Graphed performance often provides valuable insight

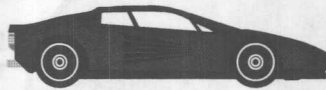
1-14

The final step in choosing an amplifier is usually a matter of a more thorough comparison of key specifications and performance graphs to determine the best fit. A few words of caution:

While op amp configurations are largely standardized, parametric specifications are not. Test conditions may vary, usually to showcase the amplifier at its best. This is called specsmanship. Compounding this is the technology mix: selecting an amplifier based on a comparison of a few specifications fails to comprehend the sometimes subtle but critical characteristics of bipolar, biFET, or CMOS fabrication processes. In this, especially, electronic selection guides can be misleading, yielding a mix of incompatible amplifiers as a consequence of searching a database of raw numbers, as I pointed out earlier. Paper selection guides are often a better place to start as factory "experts" typically group amplifiers so that an "apples to apples" comparison can be made. Be careful not to make apples to oranges comparisons or even apples to different types of apples. They may have the same flavor, but have entirely different texture.

Second, NEVER choose an op amp based solely on specifications! It is a rare circuit that operates with signals and load conditions that are identical to the configurations that the parameters are specified under. It's no coincidence that op amp datasheets are heavy with graphs plotting performance against a number of variables. Unspecified, and sometimes undesirable, characteristics typically turn up in these curves. Understanding how your op amp is configured and extrapolating from the curves back to the specifications is critical in ensuring your selection will perform as expected.

## The Final Cut



**3. Added features come with a price**



**4. Amplifier models often fail to describe real performance**

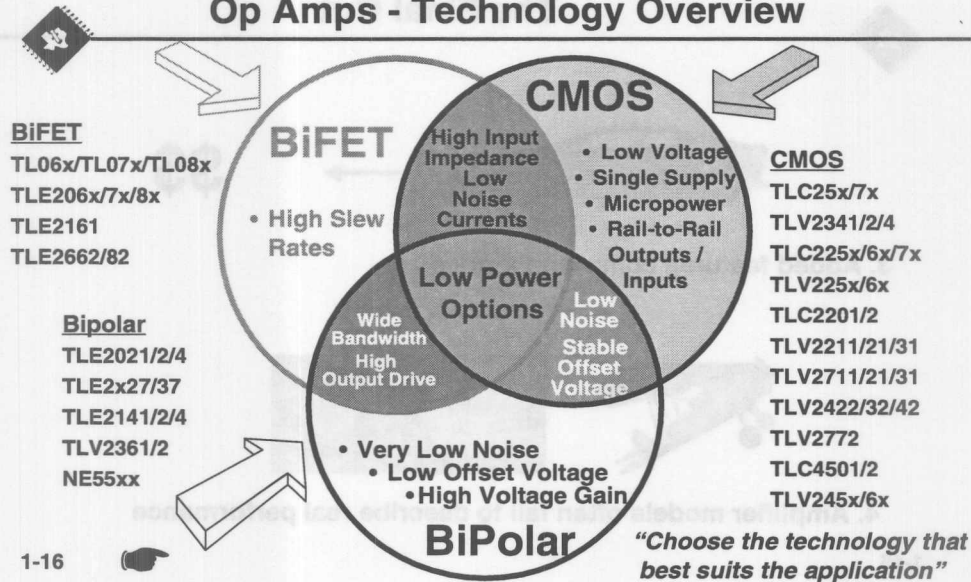
1-15

Be aware, but beware, of special features or added performance. They come at a price and, almost always, with some tradeoff in performance. Don't be hasty to pay for features you don't need.

And finally, a note about models: amplifier models are a poor tool for simulating performance of a real circuit. They are at best useful for making sure nothing has been left disconnected. Models available today are typically derived from the datasheet specifications such that if the test circuit were modeled, the simulator would output the specifications. They completely fail to comprehend boundary conditions or second-order effects, and are of little use in predicting behavior of anything but the most textbook configurations. With op amps, there is no substitute for evaluating the real circuit in the lab.

In summary, choosing an op amp doesn't need to be an intimidating task. Making common sense decisions can lead the design engineer to a few devices from which a more studied selection can be made.

## Op Amps - Technology Overview



## Op Amp Selection Table - What is Available?

**Low Noise Operational Amplifier Selection Guide**

| Operational Amplifiers | #amplifiers | V <sub>CC</sub> (V)<br>(min/max) | V <sub>IO</sub> (μV)<br>(typ/max) | I <sub>CC</sub> (mA)<br>(typ/max) | V <sub>n, typ</sub><br>(nV/Hz)<br>(@ 1kHz) | SR<br>(V/μs)<br>(typ) | GBW<br>(MHz)<br>(min/typ) |
|------------------------|-------------|----------------------------------|-----------------------------------|-----------------------------------|--------------------------------------------|-----------------------|---------------------------|
| <b>Bipolar</b>         |             |                                  |                                   |                                   |                                            |                       |                           |
| THS4001                | S           | ±2.5/±16                         | 2000/8000                         | 7.80/9.50                         | 12.5                                       | 400                   | -- /270                   |
| TLE2027                | S           | ±4/±22                           | 20/100                            | 3.80/5.30                         | 2.5                                        | 2.8                   | 7.0/13.0                  |
| TLE2037                | S           | ±4/±19                           | 20/100                            | 3.80/5.30                         | 2.5                                        | 7.5                   | 35.0/50.0                 |
| TLE2227                | D           | ±4/±22                           | 100/350                           | 7.30/10.60                        | 2.5                                        | 2.5                   | 7.0/13.0                  |
| TLE2237                | D           | ±4/±19                           | 100/350                           | 7.30/10.60                        | 2.5                                        | 5.0                   | 35.0/50.0                 |
| TLE2141                | S           | ±2/±22                           | 200/900                           | 3.50/4.50                         | 10.5                                       | 45                    | 6.0/ --                   |
| TLE2142                | D           | ±2/±22                           | 290/1200                          | 6.90/9.00                         | 10.5                                       | 45                    | 6.0/ --                   |
| TLE2144                | Q           | ±2/±22                           | 600/2400                          | 13.80/18.00                       | 10.5                                       | 45                    | 6.0/ --                   |
| TLV2361                | S           | ±1/±2.5                          | 1000/6000                         | 1.40/2.25                         | 9                                          | 2.5                   | -- /6.0                   |
| TLV2362                | D           | ±1/±2.5                          | 1000/6000                         | 2.80/4.50                         | 9                                          | 2.5                   | -- /6.0                   |
| TLC2654                | S           | ±1.9/±8                          | 5/20                              | 1.50/2.40                         | 13                                         | 2.0                   | -- /1.9                   |
| <b>BiFET</b>           |             |                                  |                                   |                                   |                                            |                       |                           |
| TLE2071                | S           | ±2.5/±19                         | 490/4000                          | 1.70/2.20                         | 11.6                                       | 40                    | 8.0/10.0                  |
| TLE2072                | D           | ±2.5/±19                         | 1100/6000                         | 3.10/3.60                         | 11.6                                       | 40                    | 8.0/10.0                  |
| TLE2074                | Q           | ±2.5/±19                         | 1600/5000                         | 6.50/7.50                         | 11.6                                       | 40                    | 8.0/10.0                  |
| TLE2081                | S           | ±2.5/±19                         | 490/6000                          | 1.70/2.20                         | 11.6                                       | 40                    | 8.0/10.0                  |
| TLE2082                | D           | ±2.5/±19                         | 1100/7000                         | 3.10/3.60                         | 11.6                                       | 40                    | 8.0/10.0                  |
| TLE2084                | Q           | ±2.5/±19                         | 1600/7000                         | 6.50/7.50                         | 11.6                                       | 40                    | 8.0/10.0                  |
| TLE2682                | S           | 3.5/15                           | 1100/7500                         | 8.90/ --                          | 11.6                                       | 40                    | 8.0/10.0                  |

## Low Noise Operational Amplifier Selection Guide (continued)

| Operational Amplifiers | #amplifiers | V <sub>CC</sub> (V)<br>(min/max) | V <sub>IO</sub> (μV)<br>(typ/max) | I <sub>CC</sub> (mA)<br>(typ/max) | V <sub>n, typ</sub><br>(nV/Hz)<br>(@ 1kHz) | SR<br>(V/μs)<br>(typ) | GBW<br>(MHz)<br>(min/typ) |
|------------------------|-------------|----------------------------------|-----------------------------------|-----------------------------------|--------------------------------------------|-----------------------|---------------------------|
| <b>CMOS</b>            |             |                                  |                                   |                                   |                                            |                       |                           |
| TLC2201                | S           | 4.6/16                           | 100/500                           | 1.00/1.50                         | 8                                          | 2.5                   | -- /1.8                   |
| TLC2202                | D           | 4.6/16                           | 100/1000                          | 1.70/2.60                         | 8                                          | 2.5                   | -- /1.9                   |
| TLC2252                | D           | 4.4/16                           | 200/1500                          | 0.070/0.125                       | 19                                         | 0.12                  | -- /0.2                   |
| TLC2254                | Q           | 4.4/16                           | 200/1500                          | 0.14/0.25                         | 19                                         | 0.12                  | -- /0.2                   |
| TLC2262                | D           | 4.4/16                           | 300/2500                          | 0.40/0.50                         | 12                                         | 0.55                  | -- /0.82                  |
| TLC2264                | Q           | 4.4/16                           | 300/2500                          | 0.80/1.00                         | 12                                         | 0.55                  | -- /0.71                  |
| TLC2272                | D           | 4.4/16                           | 300/2500                          | 2.20/3.00                         | 9                                          | 3.6                   | -- /2.18                  |
| TLC2274                | Q           | 4.4/16                           | 300/2500                          | 4.40/6.00                         | 9                                          | 3.6                   | -- /2.18                  |
| TLC4501                | S           | 4/6                              | -- /80                            | 1.00/1.50                         | 12                                         | 2.5                   | -- /4.7                   |
| TLC4502                | D           | 4/6                              | -- /100                           | 2.50/3.60                         | 12                                         | 2.5                   | -- /4.7                   |
| TLV2772                | D           | 2.2/5.5                          | 360/2500                          | 2.00/4.00                         | 17                                         | 10.5                  | -- /5.1                   |
| TLV2252                | D           | 2.7/8                            | 200/1500                          | 0.068/0.125                       | 19                                         | 0.1                   | -- /0.187                 |
| TLV2254                | Q           | 2.7/8                            | 200/1500                          | 0.135/0.25                        | 19                                         | 0.1                   | -- /0.187                 |
| TLV2262                | D           | 2.7/8                            | 300/2500                          | 0.40/0.50                         | 12                                         | 0.55                  | -- /0.67                  |
| TLV2264                | Q           | 2.7/8                            | 300/2500                          | 0.80/1.00                         | 12                                         | 0.55                  | -- /0.67                  |
| TLV2442                | D           | 2.7/10                           | 300/2000                          | 1.50/2.20                         | 18                                         | 1.3                   | -- /1.75                  |
| TLV2231                | S           | 2.7/10                           | 750/3000                          | 0.75/1.00                         | 16                                         | 1.25                  | -- /1.9                   |
| TLV2731                | S           | 2.7/10                           | 700/3000                          | 0.75/1.50                         | 16                                         | 1.25                  | -- /1.9                   |

**Precision Op Amp Selection Guide**

| Op Amps        | #amplifiers | V <sub>CC</sub> (V)<br>(min/max) | V <sub>IO</sub> (μV)<br>(typ/max) | I <sub>CC</sub> (mA)<br>(typ/max) | I <sub>IB</sub> (nA)<br>(typ,max) | CMRR<br>(dB)<br>(min/typ) | V <sub>n, typ</sub><br>(nV/Hz)<br>(@ 1kHz) |
|----------------|-------------|----------------------------------|-----------------------------------|-----------------------------------|-----------------------------------|---------------------------|--------------------------------------------|
| <b>Bipolar</b> |             |                                  |                                   |                                   |                                   |                           |                                            |
| TLE2021        | S           | ±2/±20                           | 120/500                           | 0.20/0.30                         | 25/70                             | 100/115                   | 15                                         |
| TLE2022        | D           | ±2/±20                           | 150/500                           | 0.55/0.70                         | 35/70                             | 95/106                    | 15                                         |
| TLE2027        | S           | ±4/±22                           | 20/100                            | 3.80/5.30                         | 15/90                             | 100/131                   | 2.5                                        |
| TLE2037        | S           | ±4/±19                           | 20/100                            | 3.80/5.30                         | 15/90                             | 100/131                   | 2.5                                        |
| TLE2227        | D           | ±4/±22                           | 100/350                           | 7.30/10.60                        | 15/90                             | 98/115                    | 2.5                                        |
| TLE2237        | D           | ±4/±19                           | 100/350                           | 7.30/10.60                        | 15/90                             | 98/115                    | 2.5                                        |
| TLE2141        | S           | ±2/±22                           | 200/900                           | 3.50/4.50                         | 700/1500                          | 85/108                    | 10.5                                       |
| TLE2142        | D           | ±2/±22                           | 290/1200                          | 6.90/9.00                         | 700/1500                          | 85/108                    | 10.5                                       |
| TLC2654        | S           | ±1.9/±8                          | 5/20                              | 1.50/2.40                         | 50/ --                            | -- /125                   | 13                                         |
| <b>CMOS</b>    |             |                                  |                                   |                                   | I <sub>IB</sub> (pA)              |                           |                                            |
| TLC1078        | D           | 1.4/16                           | 160/450                           | 0.020/0.034                       | 0.6/ --                           | -- /95                    | 68                                         |
| TLC1079        | Q           | 1.4/16                           | 190/850                           | 0.040/0.068                       | 0.6/ --                           | -- /95                    | 68                                         |
| TLC277         | D           | 3/16                             | 200/900                           | 1.40/3.20                         | 0.6/ --                           | -- /80                    | 25                                         |
| TLC279         | Q           | 3/16                             | 200/900                           | 2.70/6.40                         | 0.6/ --                           | -- /80                    | 25                                         |
| TLC2201        | S           | 4.6/16                           | 100/500                           | 1.00/1.50                         | 1/ --                             | -- /110                   | 8                                          |
| TLC2202        | D           | 4.6/16                           | 100/1000                          | 1.70/2.60                         | 1/ --                             | -- /100                   | 8                                          |
| TLC2252        | D           | 4.4/16                           | 200/1500                          | 0.070/0.125                       | 1/ --                             | -- /83                    | 19                                         |
| TLC2254        | Q           | 4.4/16                           | 200/1500                          | 0.14/0.25                         | 1/ --                             | -- /83                    | 19                                         |
| TLC2262        | D           | 4.4/16                           | 300/2500                          | 0.40/0.50                         | 1/ --                             | -- /83                    | 12                                         |
| TLC2264        | Q           | 4.4/16                           | 300/2500                          | 0.80/1.00                         | 1/ --                             | -- /83                    | 12                                         |
| TLC2272        | D           | 4.4/16                           | 300/2500                          | 2.20/3.00                         | 1/ --                             | -- /75                    | 9                                          |
| TLC2274        | Q           | 4.4/16                           | 300/2500                          | 4.40/6.00                         | 1/ --                             | -- /75                    | 9                                          |
| TLC4501        | S           | 4/6                              | -- /80                            | 1.00/1.50                         | 1/ --                             | 90/100                    | 12                                         |
| TLC4502        | D           | 4/6                              | -- /100                           | 2.50/3.60                         | 1/ --                             | 90/100                    | 12                                         |
| TLV2252        | D           | 2.7/8                            | 200/1500                          | 0.068/0.125                       | 1/ --                             | -- /65                    | 19                                         |
| TLV2254        | Q           | 2.7/8                            | 200/1500                          | 0.135/0.25                        | 1/ --                             | -- /65                    | 19                                         |
| TLV2262        | D           | 2.7/8                            | 300/2500                          | 0.40/0.50                         | 1/ --                             | -- /65                    | 12                                         |
| TLV2264        | Q           | 2.7/8                            | 300/2500                          | 0.80/1.00                         | 1/ --                             | -- /65                    | 12                                         |
| TLV2422        | D           | 2.7/10                           | 300/2000                          | 0.10/0.15                         | 1/ --                             | -- /83                    | 23                                         |
| TLV2432        | D           | 2.7/10                           | 300/2000                          | 0.195/0.25                        | 1/ --                             | -- /83                    | 22                                         |
| TLV2442        | D           | 2.7/10                           | 300/2000                          | 1.50/2.20                         | 1/ --                             | -- /75                    | 18                                         |

## Design Considerations Migrating from Dual to Single Supplies



### Migrating from Dual to Single Supplies

- Differences between split and single supply op amps
- Signal biasing techniques
  - Split supply configuration
  - Improper methods for single supply
  - Proper methods for single supply
- Selection of a “virtual ground”
- Summary

1-18

### Introduction

As companies are continuously striving to develop more portable and cost effective products, the number of analog engineers being asked to migrate their split supply amplifiers to a single supply voltage is increasing. The use of amplifiers with a single supply voltage introduces some issues that didn't necessarily need to be considered with split supply designs. Violation of the common-mode input range is one of the most common mistakes. Therefore, proper input signal biasing using a dc bias voltage is a major key to success in single supply systems. This dc bias voltage (sometimes called a virtual ground) can be generated using several methods; each with its own advantages and disadvantages.

## Split versus Single Supply

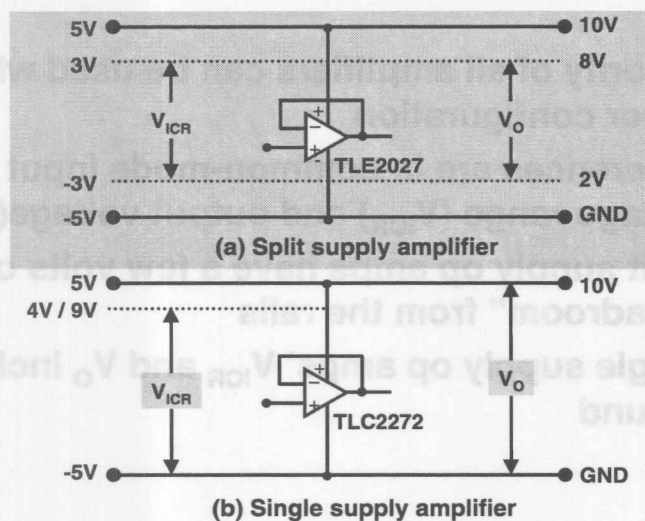
- Majority of all amplifiers can be used with either configuration
- Differences are in common-mode input voltage range ( $V_{ICR}$ ) and output voltage ( $V_O$ )
- Split supply op amps have a few volts of "headroom" from the rails
- Single supply op amps'  $V_{ICR}$  and  $V_O$  include ground

1-19

### Split supply and single supply amplifiers...is there a difference?

Many questions arise when the discussion of whether or not amplifiers specified for split supply can be operated with a single supply and vice versa. Actually, the overwhelming majority of operational amplifiers on the market today can be used with either. The amplifier can be powered by any combination of split or single supply voltages as long as the total voltage across the amplifier doesn't exceed the absolute maximum ratings. The only real differences between split supply amplifiers and those designed for single supply operation are their common-mode input voltage range and output voltage swing. The common-mode input voltage range of an amplifier is defined as the range of input voltages common to both terminals that if exceeded may cause the op amp to cease functioning properly. It is usually symbolized in the datasheet as  $V_{ICR}$  or  $V_{CM}$ . The output voltage range ( $V_O$ ) can be broken up into a high level ( $V_{OH}$ ) and low level value ( $V_{OL}$ ) and defines the maximum voltage range the output of the amplifier can swing.

## Split vs. Single Supply Amplifier



1-20

A split supply amplifier typically has a common-mode input voltage range and output voltage swing that extends to within a few volts of the supply rails. The figure above shows a TLE2027 configured as a voltage follower. Operating from  $\pm 5$  V supplies, the amplifier is able to swing  $\pm 3$  V on the input and output; therefore providing 6 volts of dynamic range. If a small signal biased just above ground is fed into the input, the amplifier will operate on it without issue. Now powering the amplifier with a +10 V single supply, the user will also get 6 volts of usable signal range, since the total voltage applied to the amplifier is the same. However, the common-mode input voltage range and output voltage now swings from +2 V to +8 V. The same signal is now outside of the linear operating range of the amplifier and therefore will not be operated on properly.

A single supply amplifier is designed so the common-mode input voltage range and output voltage swing includes the negative rail (or ground in a single supply system) and extends to within one or two volts of the positive rail. There are also rail-to-rail amplifiers available that have a  $V_{ICR}$  and  $V_O$  that includes both supply rails. Figure 1b shows the TLC2272 rail-to-rail output amplifier in the same voltage follower configuration. The common-mode input voltage range is 0V to 9V and the output swings from 0 V to +10V with a +10 V single supply (or  $V_{ICR} = -5$  V to 4V and  $V_O = -5$  V to 5V with  $\pm 5$  V supplies). Therefore, any signals near ground are still within the operating region of the amplifier and will be passed.



## Signal biasing techniques for single supply op amps

- One of the most common mistakes
- Split supply amplifiers are usually referenced to ground
- Need to generate a bias voltage (virtual ground) for single supply systems
- Bias voltage of  $V_{ICR}/2$  will provide max. dynamic range

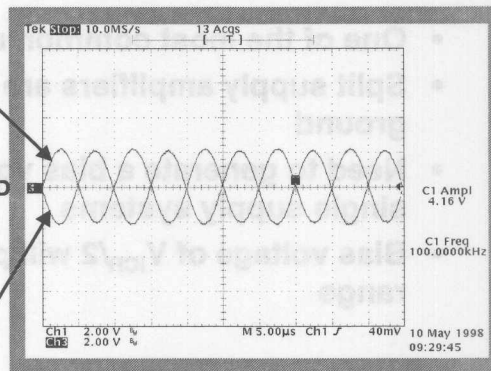
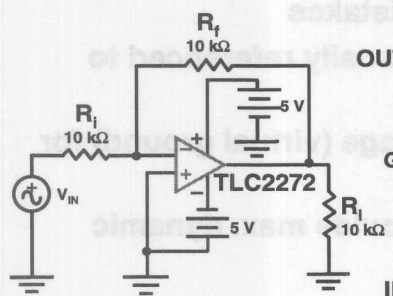
1-21

### Biasing of the input signal in single supply applications

One of the most frequent calls we receive at the factory is from split supply amplifier users having problems using an amplifier with a single supply voltage. The root of the problem usually comes from the violation of the common-mode input voltage specifications of the amplifier. Proper biasing of the input signal, especially in single supply applications is extremely important.



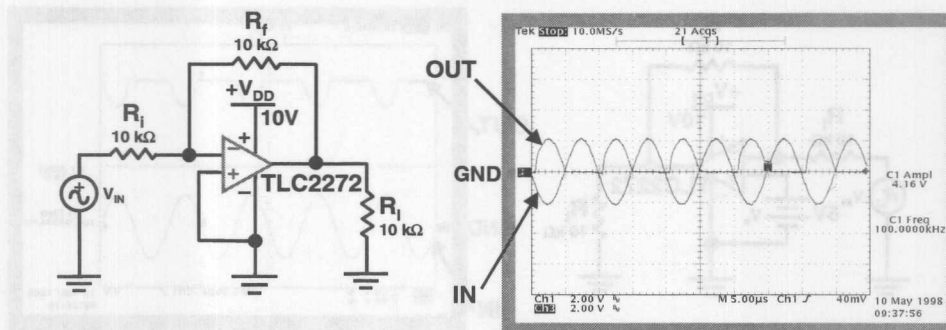
## Op amp configured with an inverting gain of 1 powered by dual $\pm 5\text{V}$ supplies



1-22

The figure above shows the TLC2272 in an inverting configuration with a gain of -1. The positive input pin and load are tied to ground. The input waveform is a 4 V peak-to-peak, 100kHz-sine wave referenced to ground. Since the amplifier is using  $\pm 5\text{ V}$  supplies, the signal is well within the linear region and the output is therefore an inverted version of the input.

# Improper signal biasing for a single supply amplifier (#1)



- Amplifier is powered by a +10V supply with the input waveform, IN+, and  $R_L$  referenced to GND
- $V_{IN} = 4.0V_{pp}$  @ 100kHz
- Output is a half-wave rectified signal

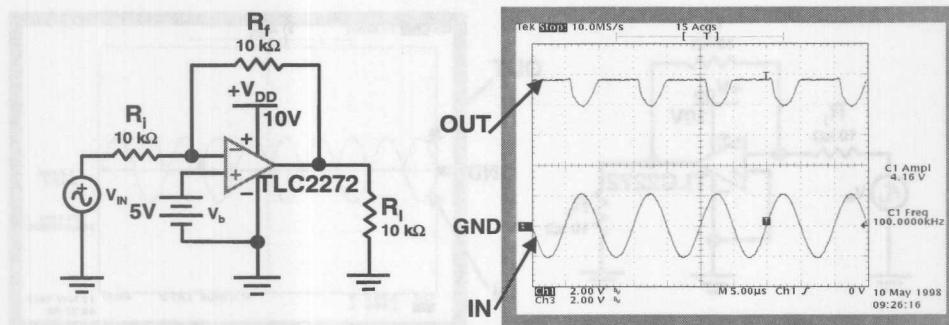
1-23

The figure above shows this same amplifier with a gain of  $-1$  now operating from a single +10 V supply. The same ground referenced signal is applied to the amplifier and, both the positive input and load are tied to ground. The resulting output waveform is now a half-wave rectified version of the input. This is obviously not what we are looking for. The amplifier is unable to operate on the positive portions of the waveform since the resulting output is at a voltage potential more negative than the lower supply rail. This causes the output to saturate just above the negative supply rail (ground in this case). All negative input voltages will drive the output into its normal positive output swing.

The second portion of the equation represents the gain of the amplifier at the inverting input terminal. It can be easily identified as the gain equation usually used for inverting amplifier configurations. The first term represents the gain at the non-inverting input terminal. In a split supply application, the positive input is usually connected to ground and therefore the dc bias voltage ( $V_d$ ) is zero, leaving the typical inverting amplifier gain equation. However, since we are biased at a point other than ground this term must be taken into consideration. In our example, this dc voltage is gained up and causes the output to saturate just below the positive supply rail. The output remains saturated for all negative portions of the input signal. All positive inputs on the inverting terminal will subtract from the dc output voltage. Again, this is clearly not what we had hoped for. The resulting waveform can be seen in figure 3b.

The previous figure illustrates two very common mistakes made when attempting to bias the input signal in a single supply application. Now we will analyze a few simple methods of proper biasing.

## Improper signal biasing for a single supply amplifier (#2)



- Voltage is applied to IN+ in an attempt to bias the input signal
- Both dc and ac are gained up causing the output to saturate into the top rail

$$V_o = V_B \left( \frac{R_f}{R_i} + 1 \right) - V_i \left( \frac{R_f}{R_i} \right)$$

1-24

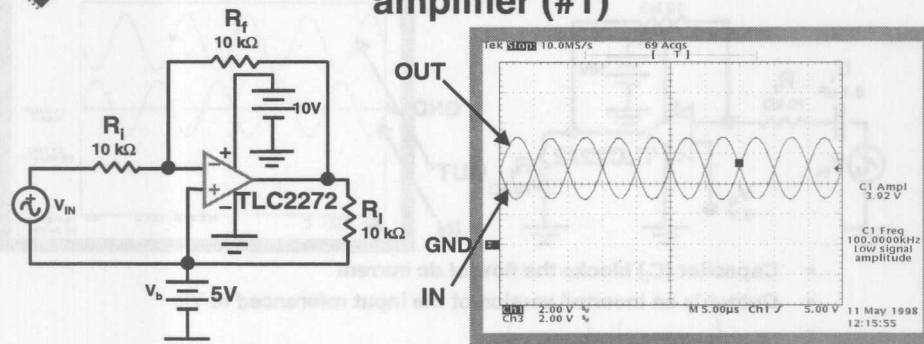
This figure shows, the amplifier with a dc bias voltage (virtual ground) equal to half of the supply voltage (in this case +5 V) applied to the positive input pin in an attempt to bias up the input signal to mid rail. Using Kirchhoff's junction rule at the negative input of the op amp, the following equation can be derived for the output voltage of this amplifier.

$$V_o = V_B \left( \frac{R_f}{R_i} + 1 \right) - V_i \left( \frac{R_f}{R_i} \right)$$

The second portion of the equation represents the gain of the amplifier at the inverting input terminal. It can be easily identified as the gain equation usually used for inverting amplifier configurations. The first term represents the gain at the non-inverting input terminal. In a split supply application, the positive input is usually connected to ground and therefore the dc bias voltage (\$V\_B\$) is zero, leaving the typical inverting amplifier gain equation. However, since we are biased at a point other than ground this term must be taken into consideration. In our example, this dc voltage is gained up and causes the output to saturate just below the positive supply rail. The output remains saturated for all negative portions of the input signal. All positive inputs on the inverting terminal will subtract from the dc output voltage. Again, this is clearly not what we had hoped for. The resulting waveform can be seen in figure 3b.

The previous figure illustrates two very common mistakes made when attempting to bias the input signal in a single supply application. Now we will analyze a few simple methods of proper biasing.

## Proper signal biasing for a single supply amplifier (#1)



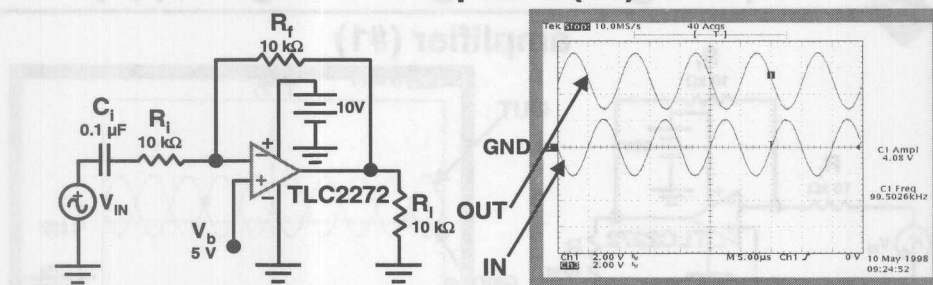
- Bias voltage is applied to  $V_{IN}$ ,  $IN+$ , and  $R_L$
- Input and output waveforms swing freely about  $V_B$
- Amplifier sees the same scenario if powered by  $\pm 5V$  and ground referenced

1-25

This figure shows the same inverting gain stage we have been discussing in the previous examples. The input waveform, positive input pin and load are now connected to a virtual ground equal to  $V_{CC}/2$ . With the virtual ground being set at  $V_{CC}/2$ , the circuit is now equal distant from both supply rails, allowing for maximum dynamic range. The signal is able to swing freely about the virtual ground without clipping.

Again, the first term represents the gain of the non-inverting input terminal. Assuming our virtual ground is a pure dc voltage (i.e. no ac noise, etc), the impedance of the capacitor is essentially infinite, which makes the gain factor in this equation go to zero, leaving only  $V_B$ . Therefore the dc output of this amplifier will be equal to the bias voltage. The gain at the inverting terminal of the op amp remains the same with one exception. With the inclusion of the capacitor, the gain of this circuit is now frequency dependent. There is an RC high pass filter created on the input by  $R_I$  and  $C_I$ . The values of these components determine the low frequency cutoff for the system. The frequency at which the gain has been attenuated by -3dB can be calculated using the following equation.

## Proper signal biasing for a single supply amplifier (#2)



- Capacitor (\$C\_i\$) blocks the flow of dc current
- Output is an inverted version of the input referenced to \$V\_B\$
- $$V_o = V_b \left( \frac{R_f}{\frac{1}{sC_i} + R_i} + 1 \right) - V_i \left( \frac{R_f}{\frac{1}{sC_i} + R_i} \right)$$
- Capacitor makes the system frequency dependent
- Low frequency cutoff point; \$f = 1/2\pi C\_i R\_i\$ (\$f = 159\text{Hz}\$)

1-26

Another example of proper input signal biasing is shown in the figure 4b. The configuration is almost identical to the one analyzed in figure 3b, but a capacitor has been added to the input. The capacitor blocks the flow of dc current and prevents the amplifier from gaining up the dc bias voltage on the non-inverting input pin. All ac current passes through the capacitor, so the output waveform is an inverted version of the input biased at \$V\_B\$ (in this case + 5V). This can also be explained using the output voltage equation derived earlier. Adding the impedance of the capacitor, the equation is as follows.

$$V_o = V_B \left( \frac{R_f}{\frac{1}{sC_i} + R_i} + 1 \right) - V_i \left( \frac{R_f}{\frac{1}{sC_i} + R_i} \right)$$

Again, the first term represents the gain of the non-inverting input terminal. Assuming our virtual ground is a pure dc voltage (i.e. no ac noise, etc), the impedance of the capacitor is essentially infinite, which makes the gain factor in this equation go to zero, leaving only \$V\_B\$. Therefore the dc output of this amplifier will be equal to the bias voltage. The gain at the inverting terminal of the op amp remains the same with one exception. With the inclusion of the capacitor, the gain of this circuit is now frequency dependent. There is an RC high pass filter created on the input by \$R\_i\$ and \$C\_i\$. The values of these components determine the low frequency cutoff for the system. The frequency at which the gain has been attenuated by -3dB can be calculated using the following equation.

$$f(-3dB) = \frac{1}{2\pi R_i C_i}$$

For our circuit  $C_i = 0.1\mu F$  and  $R_i = 10k\Omega$ , making a low frequency cutoff point of 159Hz. Any signals lower than this frequency will be attenuated at 20dB/decade.

In figure 4c, a capacitor has also been added at the output of the amplifier. This output capacitor blocks all dc current across the load. This changes the dc bias point across the load from  $V_B$  to ground. The capacitor forms an RC network with the load resistor and will also cause signal frequencies near its low frequency limit to attenuate. In this example, the capacitor and resistor values are the same as in figure 4b so the low frequency cutoff point is again 159 Hz. With the inclusion of the second RC network, signals at the cutoff frequency will now be attenuated by -6dB instead of -3dB.

The three previous examples demonstrate the proper way to bias the input signal in a single supply application. The first example is probably the most desirable as no external components are required (other than the virtual ground). However, if the application doesn't allow the input waveform, load, and positive input pin of the amplifier to be referenced to a virtual ground, then examples two and three would be more suitable. The designer must always keep in mind the addition of capacitors make the circuit frequency dependent.



### **Selection of a “virtual ground”**

- Critical to select the proper method for the application
- Key parameters for effective virtual ground
  - Power dissipation
  - Load/supply Regulation
  - Output impedance
- What are the key concerns and how much are you willing to pay?

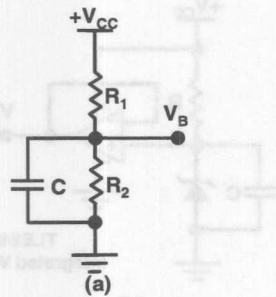
1-27

### **Methods for generating a virtual ground**

We have spent some time discussing both proper and improper methods for biasing single supply amplifiers using a dc bias voltage. However, little time has been dedicated to how this virtual ground is generated. In the examples presented earlier we were assuming this dc bias voltage was ideal. We all know this is never the case though. We will now look at several examples of virtual grounds and their inherent advantages and disadvantages.

Some parameters that should be evaluated when selecting a virtual ground are power dissipation, load and input regulation, and output impedance. Ultimately, the decision on which virtual ground to use will come down to what key care-about the engineer has for his/her particular application and how much they are willing to pay for them.

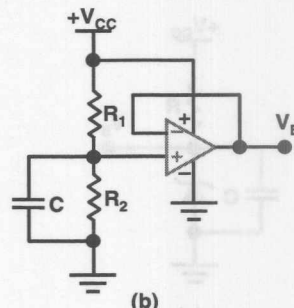
## Generating a "Virtual Ground"



(a)

- | <u>Advantages</u> | <u>Disadvantages</u> |
|-------------------|----------------------|
| • Low Cost        | • Supply rejection   |
|                   | • Power dissipation  |
|                   | • High $Z_o$         |
|                   | • Load regulation    |

1-28



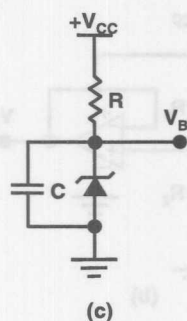
(b)

- | <u>Advantages</u> | <u>Disadvantages</u>      |
|-------------------|---------------------------|
| • Load regulation | • Supply rejection        |
| • Low $Z_o$       | • Increase in board space |
|                   | • Component cost          |
|                   | • Power dissipation       |

Probably the most widely used technique for generating a virtual ground is a resistor divider plus a bypass capacitor. It is also probably the most cost effective solution available, as the price of resistors and capacitors are usually much less than integrated circuits. However, among its disadvantages are poor load regulation and low supply rejection. If the load is tied to the virtual ground, any high source or sink current requirements will cause errors in the dc bias voltage. Also, any type of noise ripple generated from the power supply will feed through the divider and introduce errors into the system. The level of power dissipation of the divider can be calculated using the total series resistance of the divider and the supply voltage. For a 1-k $\Omega$  divider with a +5 V power supply, the power dissipation is 12.5 mW. This is shown in section a of the figure above.

Using an amplifier to buffer this resistor divider will solve the load regulation problem. The amplifier is able to handle load current demands much more effectively than the divider network. Unfortunately, an additional component is needed which will increase the cost of your system. A large increase in board space used to be a major concern of designers when considering this method. However, with the recent introduction of amplifiers in extremely small packages, like SOT23, the extra real estate needed is minimized. The supply current of the additional amplifier also takes away from battery life in portable applications. This configuration is shown in section b.

## Generating a "Virtual Ground"



(c)

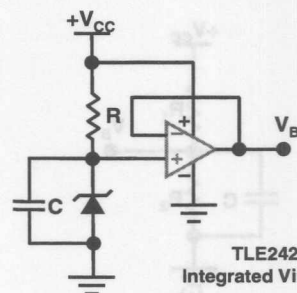
### Advantages

- Load regulation
- Supply rejection

### Disadvantages

- Power hungry
- High  $Z_o$

1-29



(d)

### Advantages

- Load regulation
- Supply rejection
- Low  $Z_o$

### Disadvantages

- Component cost
- Power dissipation
- Board space increase

Another method for generating a virtual ground is by using a voltage reference. This can be seen in the figure above (c.). The active device significantly increases input regulation over the previous two methods. However, a drawback of the voltage reference is its high power consumption. For the reference to offer a very stable dc voltage, enough bias current must be available at all times. This equates into constant levels of dc current, which increases your total power consumption. For this reason, this is not the most ideal case especially in portable applications.

This reference can also be buffered with an amplifier. The input and load regulation from the reference and amplifier respectively is by far the best among the four solutions. Added components, power dissipation and cost are the penalties. The figure above (d) shows this configuration.

The selection of a virtual ground is really dependent on the needs of the particular application. If the system will demand high source and sink current capabilities from the virtual ground then one may need to select an option with a buffer. If input regulation is a critical parameter then use of a voltage reference might be the best option. Less demanding applications may only need a simple, low cost divider network.

## Summary

- Split and single supply amplifiers vary in  $V_{ICR}$  and  $V_O$
- Improper signal biasing is a common mistake
- Single supply amplifiers should be biased with a virtual ground
- Selection of a virtual ground depends on key concerns and cost goals

1-30

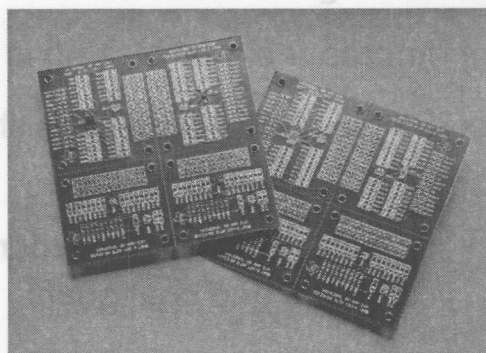
## Conclusion

The number of designers migrating from split supply to single supply amplifiers is at an all time high. When using a single supply voltage, the engineer will be introduced to new design issues. In order to be successful designing with these single supply products, a good understanding of  $V_{ICR}$  limitations and input signal biasing is critical. Proper selection of a virtual ground is also important. Several examples were presented that cover a majority of single supply applications.

## Evaluating Operational Amplifiers

### Universal Op Amp EVM

- Quick circuit evaluation with surface mount parts
- Standard circuit elements plus prototyping area.
- 2 Layer ground plane PWB
- 4 Snap-apart areas
- Multiple package types
- Area 100 & 200:
  - Dual op amps
  - SOIC, TSSOP, MSOP
- Area 300 & 400
  - Single op amps
  - SOT23-5



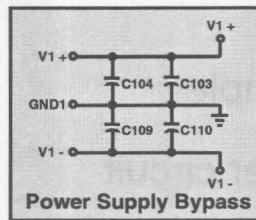
1-32

### Universal Op Amp EVM Description

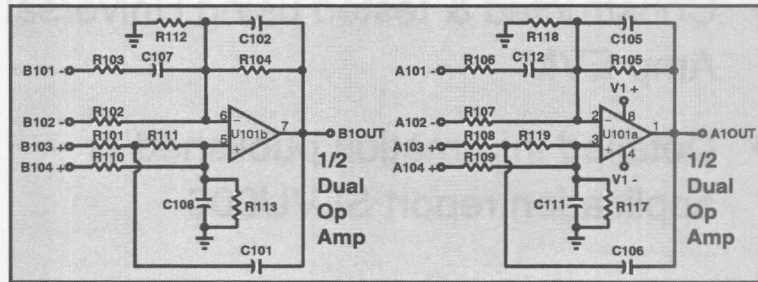
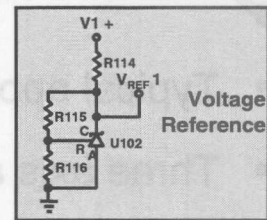
Evaluating applications circuits using operational amplifier normally requires the use of a breadboard or prototype printed wiring board(PWB). A breadboard quite often does not approximate real application due to lack of ground planes and proper signal routing. Breadboards do not normally lend themselves to the use of surface mount components. A prototype PWB is often a time and resource consuming effort. The Universal Op Amp Evaluation Module (EVM) is designed to provide quick easy evaluation of surface mount op amps with excellent signal and noise performance.

The EVM consists of four separate circuits on a snap apart PWB. Each section contains an identical circuit. The sections provide different package layouts to accommodate dual op amps in SOIC, TSSOP and MSOP packages. Single op amps in the SOT23-25 packages are also accommodated.

# Universal Op Amp EVM Area Schematic



Area 100  
SOIC



1-33

## Universal Op Amp EVM Schematic

The schematic above is for one of the four EVM sections. This is the first section (100). Section 100 accommodates dual op amps and provides connections for standard biasing and feedback resistors. Resistors and capacitors associated with amplifier compensation and filter circuits are also provided. All of the passive components are accommodated in surface mount packaging. Additionally a prototype area with uncommitted PWB pads allows additional circuit configurations. Each section has the same circuit configuration. Sections 100 & 200 have dual circuits. Sections 300 & 400 have single circuits.

A complete application report is available describing the EVM and the implementation of standard amplifier and filter circuits.

 **Accelerometer Application**

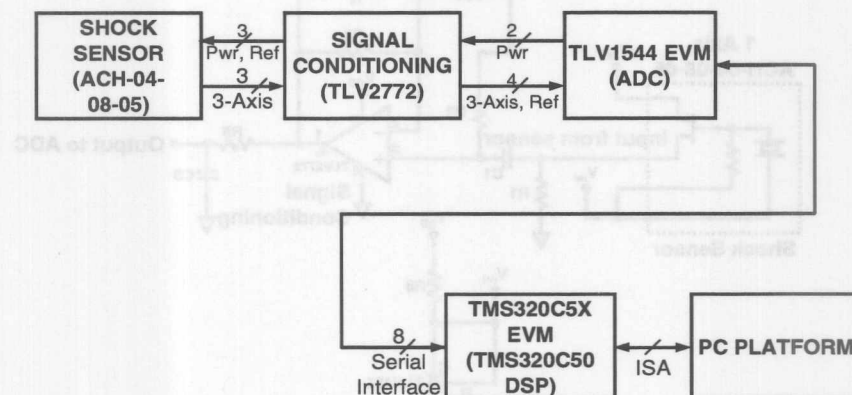
- Typical application example
- Three axis accelerometer circuit
- Constructed & tested using Universal op Amp EVM
- Detailed information published in application report SLVU006

1-34

**Universal Op Amp EVM - Accelerometer Application**

An application circuit interfacing a three axis accelerometer to the input of an analog to digital converter is available. This application report describes a practical implementation of the EVM and the circuit performance. The application report describes a complete system for measuring acceleration in three axis.

## Accelerometer Application



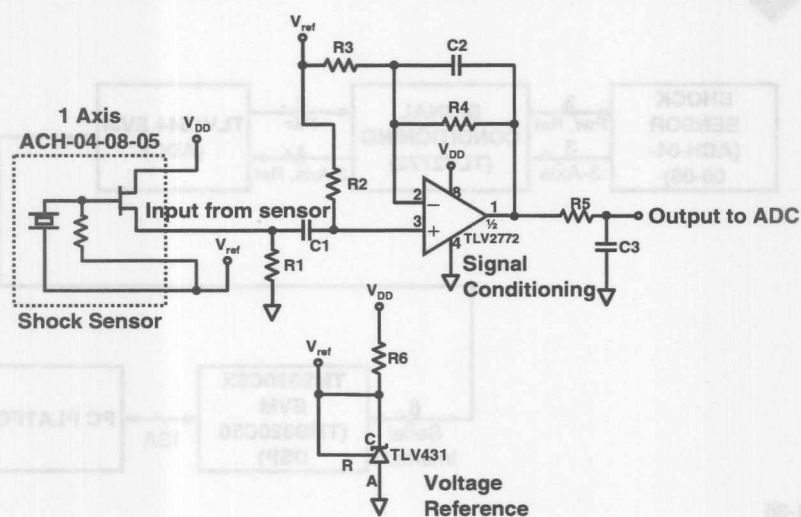
1-35

### Accelerometer System Diagram

- The accelerometer system consists of the accelerometer (shock sensor), sensor signal conditioning, analog to digital conversion, digital signal processing and user interface. The system implemented using three EVMs. Two sections of a Universal Op Amp EVM are used for signal conditioning of the sensor output. A TLV1544 EVM provides the analog to digital conversion function. The digital output of the TLV1544 EVM interfaces directly to a TMS320C5X EVM for the Digital Signal Processing function. A PC connects to the DSP EVM and provides user interface.

A complete circuit description, software routines, timing performance and sensitivity data are included in the complete application report.

## Accelerometer Schematic



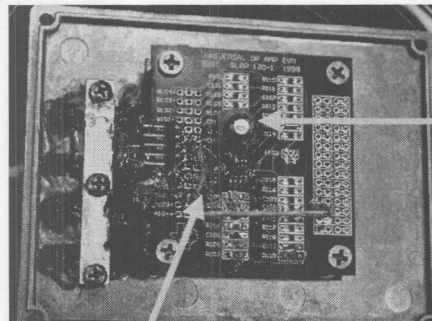
1-36

### Sensor Signal Conditioning

The shock sensor consists of accelerometers (X,Y & Z axis) mounted in a single package. The schematic above shows the signal conditioning for one of the sensors outputs. The sensor output signal is from an FET buffer located in the sensor assembly. The signal is amplified and filtered with a single TLV2272 op amp channel using the Universal Op Amp EVM. This is a single supply circuit. The sensor is biased with a virtual ground generated with a TLV431 shunt regulator.

A complete circuit description, software routines, linearity performance and sensitivity data are included in the complete application report.

## Op Amp EVM - Accelerometer Circuit

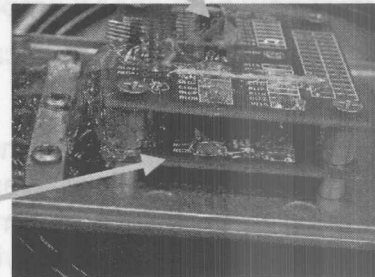


**Z Axis Amplifier**

**X & Y Axis Amplifiers**

**Accelerometer is mounted on lower board**

**Bypass capacitor**



1-37

The illustration above is a photograph of the amplifier circuits constructed for the accelerometer signal conditioning. The three circuits were built using two Op Amp EVM sections mounted in a sandwich configuration. The sensor is mounted on the lower board and is not visible. After construction and initial testing clear RTV was applied to the boards prior to running vibration tests.

## High Speed Amplifiers

High speed amplifiers, although similar in basic function to the general purpose op amp, are very different in both performance and application. This section will cover:

- What is a high speed amplifier?
- What parameters are important?
- What are the two configurations and their advantages?
- Several new high speed amplifier products.
- A high speed amplifier application in a data acquisition system.

When someone says to you, "I need an op-amp" what do you think of? If your like most people, you think of classic op-amp. But what if you needed to amplify a video signal or receive a communications signal? These classic op-amps will not suffice. This presentation will serve to focus your attention on the next generation of operational amplifiers - High Speed.



### High Speed vs Standard Op Amps

- **What is high speed?**
  - **Bandwidth > 50 MHz**
  - **Slew rate > 100 V/ $\mu$ s**
- **What makes it different?**
  - **Bipolar (BiCom) process instead of CMOS or BiCMOS**
  - **Different parameters are important**
  - **Much more stringent board layout requirements**

1-39

### What is a high speed amplifier?

In the operational amplifier market, High Speed is generally defined as having a bandwidth of 50 MHz or greater and a slew rate of at least 100 V/ $\mu$ S. CMOS or BiCMOS is typically limited to 15 MHz and below. These processes are not fast enough to fit into this High Speed category.

Welcome to the world of the BiCOM process (Bi-polar complementary). BiCOM-I is a 30-Volt process which incorporates transistors that have a  $f_{max}$  of several GHz. This is the backbone of the High Speed Amplifier line at Texas Instruments.

Because the frequencies of interest start at 50 MHz, PCB requirements have to change. We have to worry about line impedance matching, reflections, stray capacitance, and lead inductance. This requires a new way of thinking when laying out a circuit. This presentation is not intended to clarify all of these issues, but it is still an important change from the classic op-amp of yesterday.

Now that we have all of this speed, there are going to be a few changes in the way we classify an op-amp. The parameters carry over from the classic op-amp, but the order of importance is changed.



## High Speed Op Amp Parameters

### Important

- Bandwidth
- Slew rate
- Settling time
- THD
- Differential gain/phase
- Noise

### Not as Important

- Input impedance
- Offset voltage
- Offset current
- PSRR
- CMRR

1-40

### What parameters are important?

The most important parameter of a High Speed Op-amp is the bandwidth. This is typically the -3dB point of the output signal and is the first step in classifying the device.

The slew rate is the next most important parameter. This tells us how fast the output can change within a given amount of time. The typical units are Volts per micro-second, with high-speed stipulating a minimum of 100 V/uS.

The settling time can also be a very important factor in sampling systems. This lets you know when the output has settled to within 0.1% or 0.01% of the final value. The most obvious use for this knowledge is in Analog-To-Digital converters.

Passing a pure signal through an amplifier without any distortion is almost always an important parameter. There are several things which influence distortion. These are ; current out of the op-amp, frequency, amplitude, and whether the system is a single-ended or differential output. The differential output system will generally minimize the second-order harmonics of the amplifier and causes the third-order harmonics to dominate.

In conjunction with distortion, differential gain and differential phase come into play. This is generally utilized for video systems (such as NTSC or PAL).

One final important parameter to high-speed amplifiers is the internal noise. This is especially important for receiving very small signals from an antenna or sensor. In-order to maximize the Signal-To-Noise Ratio (SNR), this receiver amplifier has to have a low internal noise source in conjunction with a high gain.

Typically, the input impedance is not important for high-speed systems. This is because most high-speed systems use either 50-ohm or 75-ohm termination resistors. This is done to reduce reflections over a transmission line.

Most high-speed systems AC couple the signals by utilizing a DC blocking capacitor. Obviously then, the input offset voltage and input offset currents are not very important parameters.

When dealing with signals over 10 MHz, EMI radiation typically occurs. Coupled with the fact that bypass capacitors have a limited frequency usefulness and trace inductance, it is easy to see why the Power Supply Rejection Ratio (PSRR) of the op-amp is not a very important factor. This typically has to be controlled external to the device and can involve some serious trial and error to find a proper solution.

Finally, Common Mode Rejection Ratio (CMRR) is not a very important parameter. This is due to the fact that most interference signals within a differential system do not require a CMRR greater than 60dB (1000 to 1 SNR).

 High Speed Amplifier Applications

---

- **Communication**
  - ADSL/HDSL/VDSL
  - Cellular
  - DBS
  - CATV
- **Imaging**
  - Medical
  - Scanners
  - Copiers
  - Lasers
  - Radar/Sonar
- **Video/Multimedia**
  - Cameras
  - Monitors
  - Distribution
  - Set Top Boxes
  - Conferencing
- **Instrumentation**
  - Oscilloscopes
  - Spectrum Analyzers
  - Automatic Test Equipment
  - Data Acquisition

1-41

**Where do you use high speed amplifiers?**

So where do you find High Speed Amplifiers? They are found everywhere. Some are obvious, such as within video equipment and communication systems. Others are not so obvious and rather obscure. This can include things such as the front end of an oscilloscope or within imaging systems.

The list shows a partial list of where High-Speed amplifiers can be found. This is by no means a complete list, but it should get you thinking about where high speed amplifiers are found.

As you can see in the list, one of the areas of interest is ADSL, HDSL, and VDSL communications. High Speed amplifiers are generally used within the line interface of these systems. Texas Instruments has a whole line dedicated to these systems and it is beyond the scope of this discussion. For more information about this, please talk with the High Speed Marketing representative listed at the end of this presentation.

Now that we have discussed some general parameters of high speed amplifiers and where to find them, let's look a little closer at the op-amp itself.

## Two Major High Speed Amplifier Architectures

### Voltage Feedback

- Fixed, lower slew rates
  - Fixed, lower dominant pole current
- Lower bandwidths
- Easier to use
  - Traditional op amp architecture

### Current Feedback

- Variable, higher slew rates
  - Variable, higher dominant pole current
- Higher bandwidths
- Better distortion
- Harder to use
  - Different design rules than traditional op amp

#### Internal Dominant Pole Governing Equation:

$$I = C \, dV / dt$$

- OR -

$$dV / dt = I / C$$

1-42

## Amplifier Architectures

The first thing you will notice when you dive into this field is that there are actually two main types of High Speed amplifiers. This includes the Voltage Feedback amplifier (VFB), which includes 99.9% of the classic amplifiers, and the Current Feedback amplifier (CFB). For most people, this CFB amplifier is a brand new concept and most people shy away from it. But, it is not that bad. In fact, the CFB amplifier was actually one of the first amplifiers ever to be created. But ease of use and lack of applications caused the architecture to be left behind in the dust.

So why do we need it now? To answer this we need to recall what the definition of high speed was... a bandwidth greater than 50 MHz and a slew rate of greater than 100 V/uS. VFB amplifiers can do pretty good, especially with new technology and processes. But there are internal limits based on the architecture alone.

Because the inputs of a VFB amplifier are high impedance, the internal compensation capacitor (a.k.a the dominant pole) has to be charged and discharged by the internal bias currents which are fixed. Utilizing physics, the fastest slew rate is governed by the following equation:

$$I = C \, dV/dt$$

Knowing that C and I are internal and fixed and solving for the slew rate we get :

$$dV/dt = I / C$$

This is fixed and real values show a typical slew rate of 200 to 1000 V/uS. Obviously there are other factors which influence slew rate, but this is probably one of the most important aspects. The slew rate of a voltage feedback amplifier will work for a lot of applications, but not all of them.

Current Feedback Amplifiers on the other hand, utilizes a low impedance input front-end. It uses the feedback current to charge and discharge the internal compensation capacitor. Thus, the limitation of a fixed charge current is eliminated and the slew rate can be greatly enhanced. In fact, the slew rate is directly proportional to the amplifier output voltage swing and inversely proportional to the feedback resistor.

Because bandwidth is set by the same internal capacitor, bandwidth is generally based on the same principles as stated above. Thus, VFB amps generally have lower bandwidths than CFB amps.

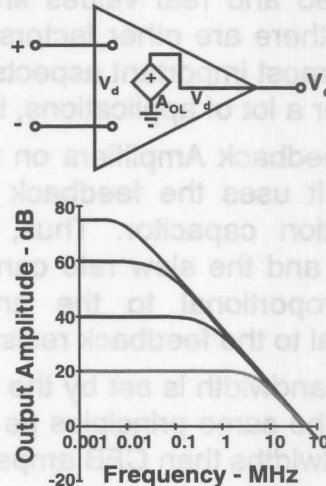
With a higher slew rate and a higher bandwidth, CFB amplifiers generally have an advantage when it comes to distortion. This is due to the fact that they can respond quicker to any non-linearities within it's own architecture. Thus eliminating distortion.

So why not use a current feedback amplifier all of the time? The problem is that a CFB amp uses the feedback current to charge and discharge the dominant pole capacitor. If you allow too much current to flow into the feedback, the dominant pole frequency gets shifted to a much higher frequency than it was designed for. This will cause the output to overshoot and eventually oscillate. Thus, you cannot use a CFB amplifier as a pure buffer with the output shorted to the inverting node. In addition, you cannot have a capacitor directly in this feedback path. The capacitor's impedance will become very small at it's resonant frequency and the op-amp **will** oscillate.

Now that we understand the concepts behind the two architectures, let's look at each one in more detail individually.

## Voltage Feedback Amplifiers

- High impedance differential input stage (i.e. no current flow at input)
- Bandwidth a function of closed loop gain - GBWP
- Internal slew rate limitations
- VF amps are the easiest to use
  - Traditional design techniques
- Applications
  - Lower frequencies
  - High feedback input impedance
  - THS4001 is VF



1-43

### Voltage feedback

First, let's talk about the classic voltage feedback amplifier. The voltage feedback amplifier (VFB) has a high impedance input stage. The amplifier first looks at the difference in voltage ( $V_d$ ) at the inverting and non-inverting terminals. The output then multiplies the difference ( $V_o$ ) by the open loop gain ( $A_{OL}$ ). With negative feedback from the output to the inverting node, we get a closed loop amplifier.

One of the main characteristics of a VFB amplifier is the bandwidth is indirectly related to the gain. As the gain is increased, the bandwidth is divided by the gain. This is known as Gain Bandwidth Product - or GBWP.

For example, if we look at the graph on the lower right corner, it shows a -3dB bandwidth of about 100 MHz at a gain of one. If we set the gain to 40 dB, or 100, then the bandwidth is divided by 100, or  $100\text{MHz} / 100 = 1\text{ MHz}$ .

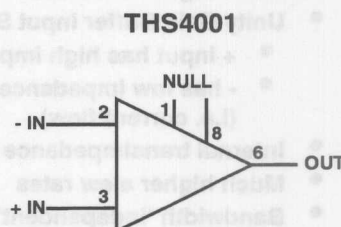
As stated previously, the VFB amplifier does have internal slew rate limitations based on its architecture. Because of this, VFB amps are generally used in lower bandwidth systems. And because it has high input impedances, the VFB amplifier is extremely easy to use. Making an integrator or a simple buffer is no problem with a VFB op-amp. This is because the op-amp does not rely on the current flowing into or out of the input stage.

Now that we know what a voltage feedback amplifier is, let's take a look at Texas Instruments first amplifier, the THS4001.

### THS4001 High Speed Voltage Feedback Amplifier

- **Very High Speed**
  - 300 MHz Bandwidth (Gain = 1, -3dB)
  - 400 V/ $\mu$ s Slew Rate
  - 30-ns Settling Time (0.1%)
- **High Output Drive**
  - $I_o = 100\text{mA}$
- **Very Low Distortion**
  - THD = -72 dBc @ 1 MHz
- **Gain & Phase Accuracy**
  - Differential Gain Error = .04%
  - Differential Phase Error = .15°
- **Evaluation Modules Available**

Fastest 30-V Voltage  
Feedback Amplifier on  
the Market.



1-44

The THS4001 is a 300 MHz, 400 V/ $\mu$ s voltage feedback amplifier. This is the world's fastest 30-Volt voltage feedback amplifier on the market today. Coupled with a 30 nSec 0.1% settling time, the THS4001 can make an excellent front-end amplifier in an Analog-to-Digital converter system.

The high output current drive of 100 mA makes this a very versatile op-amp. It can be used to drive heavy loads or termination lines at full output voltages.

Another key aspect of the THS4001 is its distortion. It has a Total Harmonic Distortion (THD) of -72dBc at 1MHz. This is a very respectable number for this class of amplifier and can be utilized to ensure signal integrity.

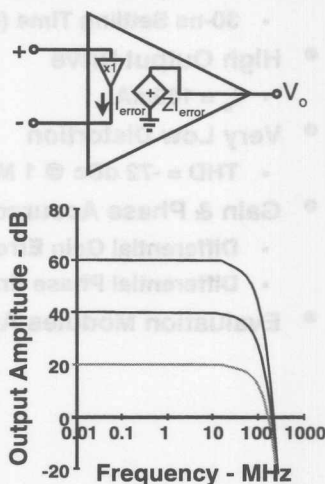
This brings up the next feature of the THS4001, a strong video specification. It has a differential gain error of 0.04% and a differential phase error of 0.15 degrees. What this means is that when a NTSC or PAL carrier frequency is DC shifted from 0 volts to 0.7 Volts (or 100 IRE), the gain and phase of the carrier is changed by the aforementioned specifications. Again, these are very respectable numbers. In fact, customer feedback has shown that coupled with the high output drive of this amplifier, differential gain and phase remain fairly constant when going from one distribution line (150 ohm load) to two distribution lines (75 ohm load).

This is all fine and dandy, but most designers hate to create a high speed test board with surface mount op-amps. To circumvent this, TI has created an Evaluation Module (EVM) for the THS4001. This is a pre-built, tested circuit which allows a designer to evaluate the THS4001 within minutes of receiving the EVM.

That concludes the voltage feedback portfolio, but we still need to discuss the current feedback system. So, let us first look at some key features of the current feedback amplifier in greater detail.

## Current Feedback Amplifiers

- Much higher slew rates
- Unity Gain Buffer Input Stage
  - + input has high impedance
  - - has low impedance (i.e. current flow)
- Internal transimpedance stage
- Much higher slew rates
- Bandwidth 'independent' of gain
- Harder to use
  - *Must* have feedback resistor
  - *NO* capacitor in feedback path
- Applications
  - ADSL, HDSL, VDSL
  - THS3001 and THS6002 are CF



1-45

## Current feedback

The first thing you will notice is that the input stage is quite different. The non-inverting input has a high input impedance, just like the VFB amplifier. But, the inverting stage is low impedance, typically less than 20 ohms. This means that current **will** flow into this pin. The output will then multiply the error current ( $I_{error}$ ) by the open loop transimpedance ( $Z$ ). With a feedback resistor placed between the output and the inverting pin, we form a closed loop system.

The first thing you will notice is that the feedback resistor limits the amount of current flow into or out of the inverting pin. And because bandwidth is determined by the amount of current available to charge the internal compensation capacitor, the feedback resistance plays the key role in determining the bandwidth of the system. Typically, as the feedback resistor is increased, the bandwidth will be decreased.

Additionally, the slew rate will also be affected by this same concept. To find out exactly what the feedback current will be, we get the following equation :

$$I_{FEEDBACK} = (V_{OUT} - V_{INVERTING\ NODE}) / R_{FEEDBACK}$$

Remember that the slew rate is determined by the current available to charge the internal dominant pole capacitor. Thus, the slew rate is determined by the output swing and the feedback current into the inverting node.

The last key feature of this system can be seen in the frequency response graph of a typical current feedback amplifier. There is not a gain bandwidth product like there is in a VFB amplifier. Thus, once you get an acceptable response out of a CFB amplifier, you simply need to change the gain resistor to change the overall system amplification, not the feedback resistor. Again, the feedback resistor controls the response of the CFB amplifier.

As stated before, the drawback to the CFB amplifier is the fact that it can be harder to use. But, careful planning will make this amplifier as easy to use as the VFB amplifier. So, if you need an extremely high slew rate, gain independent, high bandwidth amplifier, the CFB amplifier makes a logical choice.

Now that we better understand what a current feedback amplifier is, let's take a look at Texas Instruments first CFB amplifier, the THS3001.

## THS3001 High-Speed Current Feedback

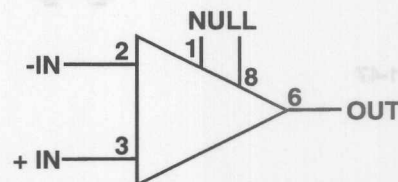
### Amplifier

- Very High Speed
  - 420 MHz Bandwidth (Gain = 1, -3dB)
  - 6500 V/ $\mu$ s Slew Rate
  - 40-ns Settling Time (0.1%)
- High Output Drive
  - $I_o = 100\text{mA}$
- Very Low Distortion
  - THD = -96 dBc @ 1 MHz
- Gain & Phase Accuracy
  - 115 MHz -0.1dB BW (Gain = 2)
  - Differential Gain Error = .01%
  - Differential Phase Error = .02°
- Evaluation Modules Available

1-46

**Fastest 30-V Current  
Feedback Amplifier on  
the Market.**

THS3001

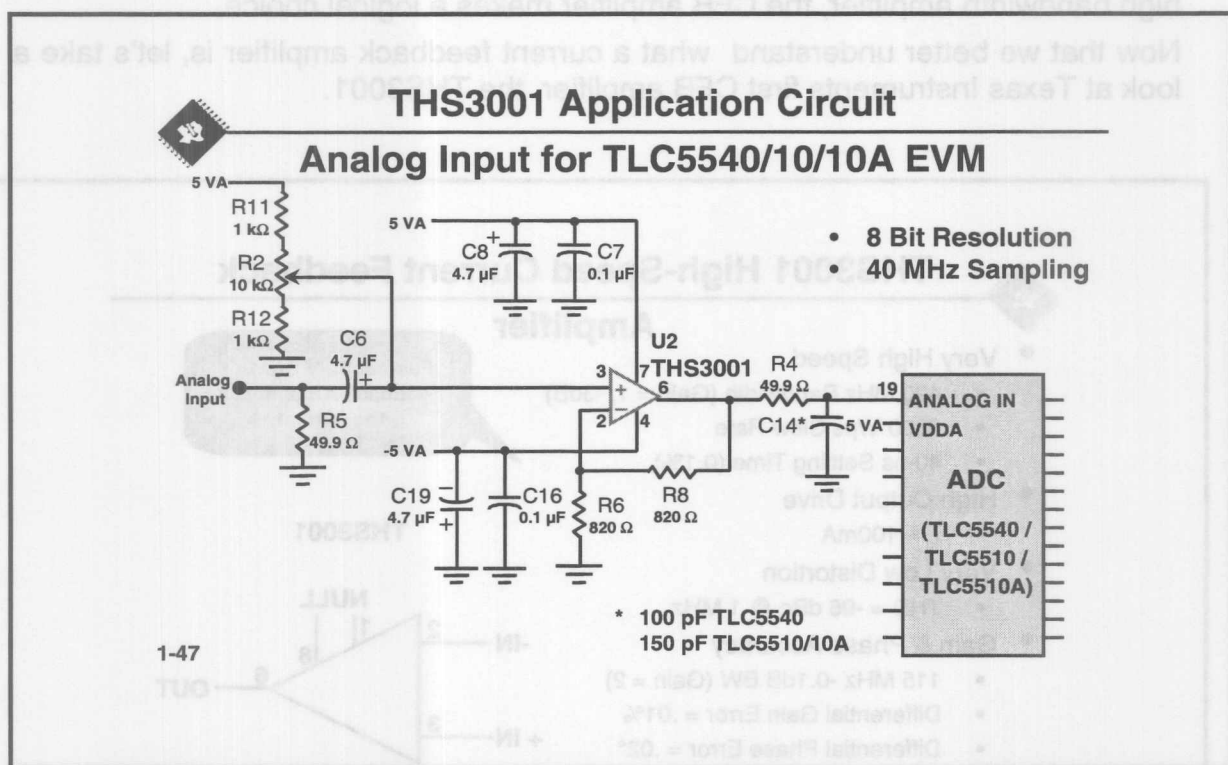


The THS3001 is a 420 MHz, 6500 V/ $\mu$ S current feedback amplifier. This is the world's fastest 30-Volt current feedback amplifier on the market today. Coupled with a 40 nSec 0.1% settling time, the THS3001 can make an excellent front-end amplifier in an Analog-to-Digital converter system.

Another key aspect of the THS3001 is its distortion. It has a Total Harmonic Distortion (THD) of -96dBc at 1MHz. This is an extremely good distortion specification and can be utilized to ensure signal integrity. Not many amplifiers on the market today can boast such a good specification.

This low distortion brings up the next feature of the THS3001, the video specifications. It has a differential gain error of 0.01% and a differential phase error of 0.02 degrees. Additionally, the THS3001 has a -0.1dB bandwidth of 115 MHz with a gain of 2, which is what most video systems are utilizing. Again, these are extremely good numbers. Coupled with an output current drive of 100 mA, the THS3001 can be used to drive multiple transmission lines with very little signal degradation.

Just like the THS4001, the THS3001 has an Evaluation Module (EVM) available. This is also pre-built, tested circuit which allows a designer to evaluate the THS3001 in gains of +2 or -1. This simple EVM will allow the designer to quickly evaluate the THS3001 with very little effort.



## High Speed Amplifier Application

Here you can see the front-end of an analog - to - digital converter (ADC). This particular converter requires a single supply and thus the input signal must also be uni-polar. To create this, the THS3001 is DC shifted to the mid-rail, creating a virtual ground to the ADC input. A signal is then AC coupled into the THS3001. The THS3001 will then amplify the DC bias and AC input signal by two. To help eliminate any glitches, a simple low pass filter is placed between the THS3001 and the ADC. This also helps in isolating the capacitive load placed on the THS3001. Without the 49.9 ohm resistor (R4) the THS3001, with just about every other high speed amplifier, will have a tendency to oscillate.

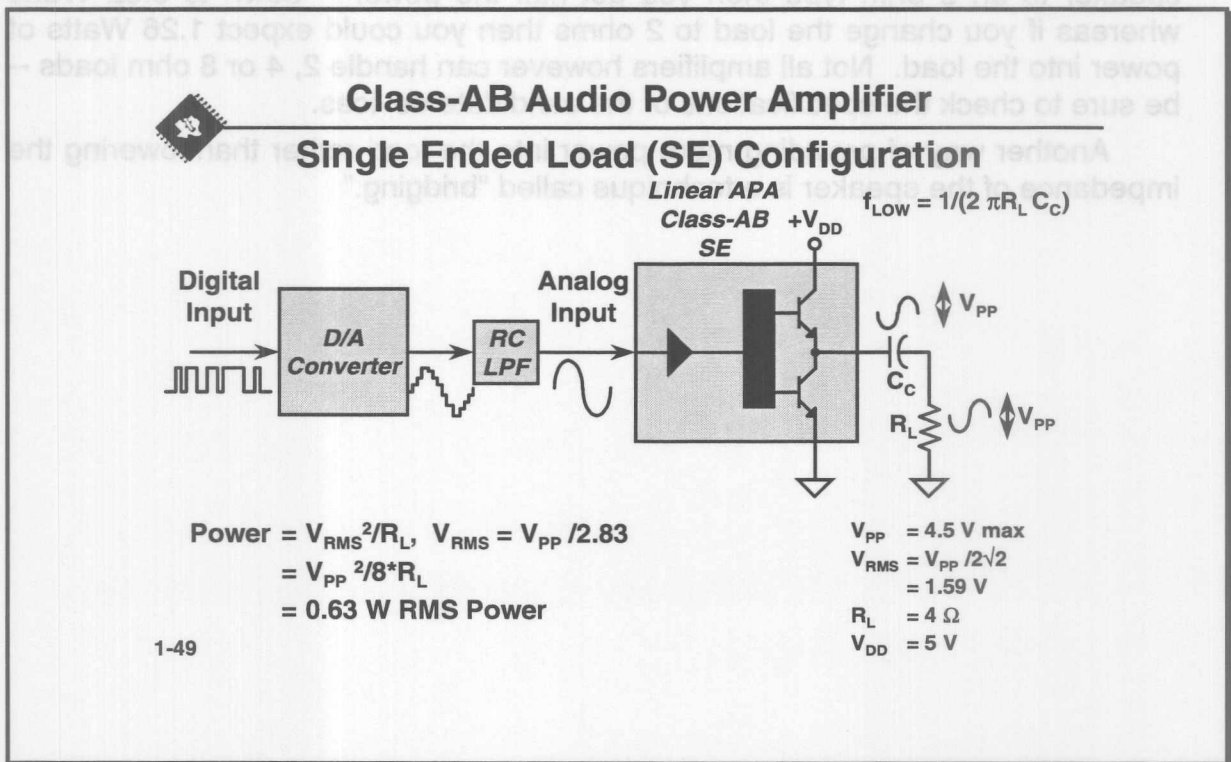
Some general rules should be discussed at this point. The first is that proper power supply bypassing must be used with a high speed amplifier. This is done

by placing bulk capacitors C8 and C19 on the power supply busses. Additionally, high frequency capacitors, such as the 0.1uF capacitors used above, should be placed as close as possible to the amplifier's power input pins. This will help supply the high-frequency currents required by the amplifier. Failure to do so will result in ringing or an increase in distortion.

One final rule which is **very** important is that the inverting node trace of the high speed amplifier must be as short as possible. This will help minimize any stray capacitance at this node. Additionally, removing a ground plane underneath this trace will also help decrease the stray capacitance. Failure to do so will cause peaking to occur in the frequency response. This will create an unstable system which will have a tendency to overshoot and possibly oscillate.

There are numerous other high frequency design rules which should be adhered to, but they are beyond the scope of this presentation. More information can be found within the application sections of the THS datasheets.

## Audio Power Amplifiers



### Class-AB With Single Ended Load (SE) Configuration

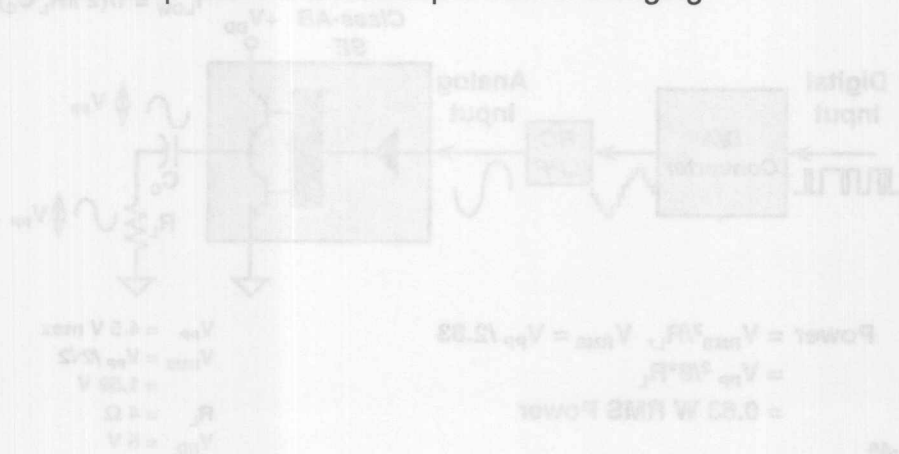
Audio Power Amplifiers (APA) are a special type of Operational Amplifier optimized to drive low impedance loads, typically speakers or headphones, at frequencies from 20 to 20 kHz. In the diagram you see a representation of a

typical computer audio output channel employing the most common type of APA, the Class AB linear amplifier. From the title, you can see that we call it Single Ended, this refers to the fact that the amplifier drives only one end of the load while the other end is typically connected to ground.

In the diagram, the D/A Converter accepts digital sound data from the Sound Chip, or other source, and converts it into a linear representation of the original sound waveform. The RC Low Pass Filter removes conversion noise from the D/A output and provides an analog waveform to the APA.

In terms of power provided to the load, the equation is straight forward if you remember to convert the Voltage to an RMS value by dividing the peak to peak number by  $2 \times (2)^{1/2}$  or 2.83. Then it is just  $V_{rms}$  squared divided by R. Also remember, that when determining the peak power capability of an amplifier, that most APAs can not approach the supply rails or distortion is significantly increased (Clipping). So, for a +5 volt supply into a 4 ohm speaker we get about 4.5 Volt maximum peak to peak swing which translates into 1.59 volts RMS (quite a difference in peak vs rms power if you happen to forget to make the conversion). Plugging the numbers into the equation you get 0.63 Watts of RMS power into a 4 ohm load from a +5 Volt power supply. If you change the speaker to an 8 ohm type then you get half the power -- down to 0.32 Watts whereas if you change the load to 2 ohms then you could expect 1.26 Watts of power into the load. Not all amplifiers however can handle 2, 4 or 8 ohm loads -- be sure to check the specifications of the candidate devices.

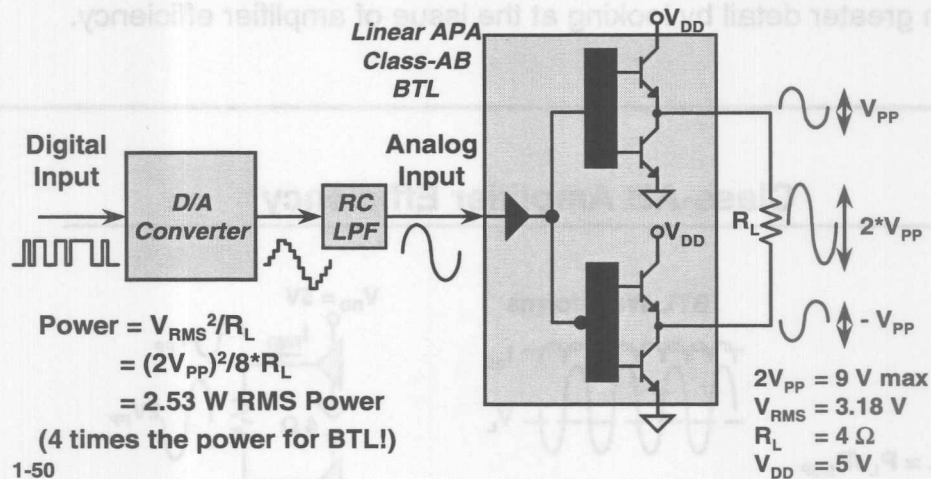
Another way of providing more power into the load rather than lowering the impedance of the speaker is a technique called "bridging."



Class-AB With Single Ended Load (SE) Configuration

Audio Power Amplifiers (APA) are a special type of Operational Amplifier optimized to drive low impedance loads, typically speakers or headphones, at frequencies from 20 to 20 kHz. In the diagram you see a representation of a

## Class-AB Audio Power Amplifier Bridge Tied Load (BTL) Configuration



### Class-AB With Bridge Tied Load (BTL) Configuration

In this diagram we see a linear APA in a Bridge Tied Load (BTL) configuration. A BTL amplifier actually consists of two linear amplifiers driving both ends of the load differentially. There are several potential benefits to this configuration but, for now, let us consider power to the load. The differential drive to the speaker means that as one side is slewing up the other side is slewing down and vice versa. This in effect doubles the available voltage swing on the load. When you plug twice the voltage into the power equation, where voltage is squared, then you get 4 times the output power from the same supply rail and load impedance.

In a typical computer sound channel running from 5 volts supplies, bridging raises the power into a 4 ohm speaker from .63 watts to 2.5 Watts. In sound power, that is a 6 dB improvement -- which is loudness you can really hear. Other advantages are there also. In the single supply SE configuration a coupling capacitor is required to block the DC offset from reaching the load (unless you are using bipolar supplies). These capacitors can be quite large (in the neighborhood of 40 to 1000 uF) so, are expensive and have the additional drawback of limiting low frequency performance. This limiting effect happens due to the high pass filter network created with the speaker impedance and the coupling capacitance and is calculated with the equation  $f_L = 1 \text{ divided by } 2 \pi RC$ . For example, a 120 uF cap with a 4 ohm speaker would attenuate low frequencies below 330 Hz -- no bass drums in that output! The BTL

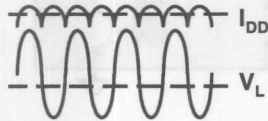
configuration cancels the DC offsets which eliminates the need for the blocking caps. Low frequency performance is then limited only by the input network and speaker response.

BTL does carry a penalty though and that penalty is increased internal power dissipation -- up by a factor of four over SE configurations of the same supply voltage. In the next slide we will investigate power dissipation of linear amps in greater detail by looking at the issue of amplifier efficiency.

## Class-AB Amplifier Efficiency



BTL Waveforms

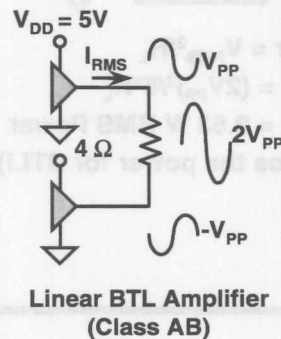


$$\text{Eff.} = P_L / P_{\text{SUP}}$$

(....after many many steps....)

$$\begin{aligned} \text{Eff.}_{\text{BTL}} &= \pi V_P / 2V_{\text{DD}} = \pi (P_L R_L / 2)^{1/2} / 2V_{\text{DD}} \\ &= 22 \% @ P_L = .25 \text{ W}, P_{\text{dis}} = 0.89 \text{ W} \\ &= 31 \% @ P_L = .5 \text{ W}, P_{\text{dis}} = 1.11 \text{ W} \\ &= 44 \% @ P_L = 1 \text{ W}, P_{\text{dis}} = 1.27 \text{ W} \\ &= 63 \% @ P_L = 2 \text{ W}, P_{\text{dis}} = 1.17 \text{ W} \\ &= 70 \% @ P_L = 2.5 \text{ W}, P_{\text{dis}} = 1.07 \text{ W} \end{aligned}$$

1-51



## Class-AB Amplifier Efficiency

Linear amplifiers are notoriously inefficient. The primary cause of inefficiency in a linear amplifier is the voltage drop across the output stage transistors. The drop occurs for two reasons, one is that even at maximum output swing from a 5 volt supply we said the output voltage would only swing 4.5 volts and the other is due to the sinewave nature of the output waveform. The equation to calculate efficiency starts out simply enough as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the rms values of power in the load, and in the amplifier, you must understand the shapes of the current and voltage wave forms as shown above. Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are very different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape whereas in BTL it is a full wave rectified, this means rms conversion factors are different. Examination of the transistor block diagrams in the previous slide will help clarify

the point, keeping in mind that for most of the waveform both the push and pull transistor are not on at the same time.

What we see from the example calculations is that the efficiency is quite horrible for lower power levels resulting in a nearly flat internal power dissipation over the normal operating range. What is a little surprising at first is the fact that the internal dissipation at full output power is less than in the half power range. Try using that as an explanation to a neighbor next time they complain about your loud music. "Sorry man, just trying to reduce the power dissipation in my amplifiers." Also remember that the above example is mono -- double everything for stereo! So, for a stereo 2.5 W audio system with a 4 ohm load and 5 V supply the maximum draw on the power supply will be almost 7.25W. Also, this equation only works for pure sine waves, and not too many real people listen to sine waves (We at TI do but we are strange characters for the most part).

A final "all is not lost" point to remember about linear amplifiers, whether they be SE or BTL configured, is how to manipulate the terms in the efficiency equation to your advantage when possible. Note that in the efficiency equation  $V_{cc}$  is in the denominator. This means that as  $V_{cc}$  goes down, efficiency goes up. Consider this example, if you replaced the 5 V supply with a 12 V supply in the above calculations, then efficiency at 2.5 W would fall to 29% and internal power dissipation would rise to 6.12 W. Use the right supply voltage and speaker impedance for your application -- Over kill will kill you over and over!

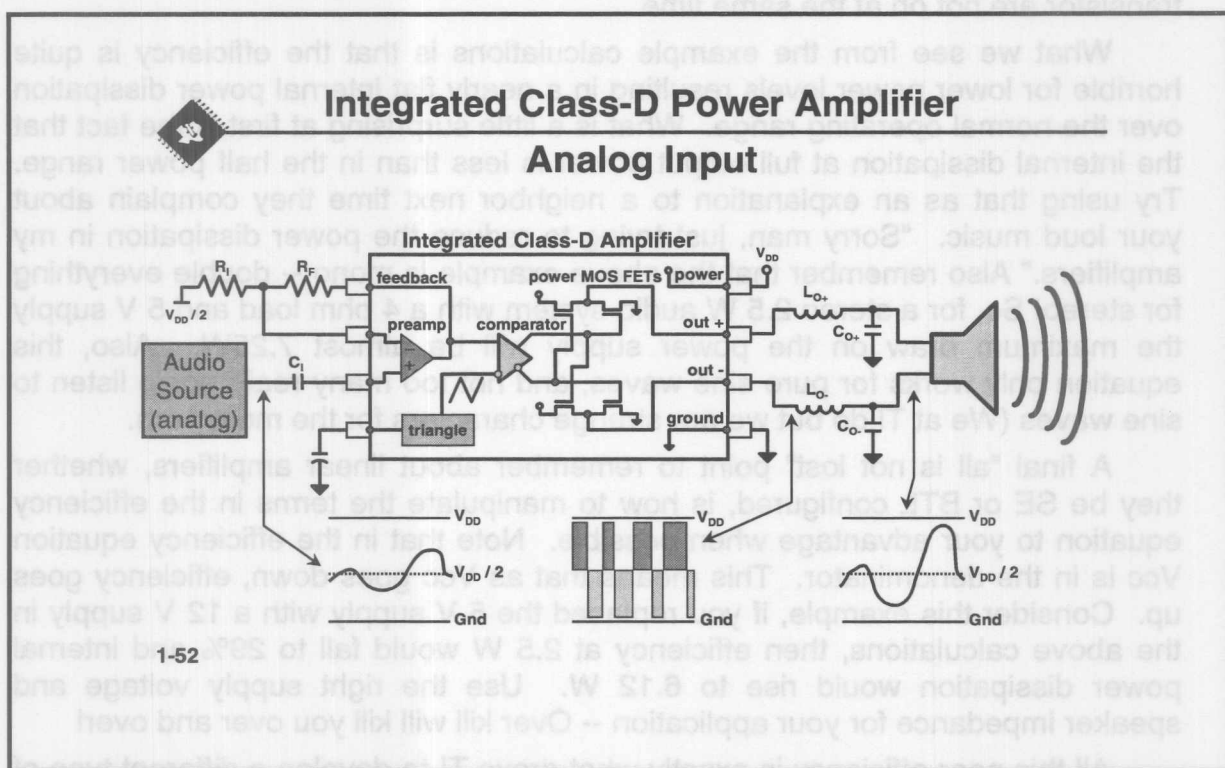
All this poor efficiency is exactly what drove TI to develop a different type of amplifier -- Class-D.

## Integrated Class-D Power Amplifier

Class-D amplifiers are switch-mode power delivery circuits much like switch-mode voltage regulators. Where regulators have a DC reference that sets the output voltage Class-D amplifiers use the audio input signal as the reference and therefore the output follows the input signal. Being similar to switch-mode power supplies much of the theory of how switch-mode power supplies operate applies directly to Class-D amplifiers. This is helpful since there is not a wealth of information available on Class-D -- Yet!

In the diagram above you see one implementation of an integrated Class-D amplifier. The word "integrated" is important. Discrete implementations of Class-D have been around for many years but until recently the technology required to place the sensitive analog circuitry on the same piece of silicon with a high Power FET was not available.

Class-D relies on a technique called Pulse Width Modulation (PWM) to sample the input and then recreates the Audio Signal at the load. PWM resembles digital data in that it has an on state and an off state. This is the key to efficiency -- when the FET is on, it has a low resistance and therefore delivers power efficiently. When it is off it delivers no power and so there is no loss. So, the Class-D amplifier turns on for a period of time (a pulse width) that is determined by the level of the input signal, grabs an efficient pulse of power, and then delivers it to the load. An output filter then smoothes these pulses of power back into a time linear signal before it gets to the speaker.



### Integrated Class-D Power Amplifier

Class-D amplifiers are switch-mode power delivery circuits much like switch-mode voltage regulators. Where regulators have a DC reference that sets the output voltage Class-D amplifiers use the audio input signal as the reference and therefore the output follows the input signal. Being similar to switch-mode power supplies much of the theory of how switch-mode power supplies operate applies directly to Class-D amplifiers. This is helpful since there is not a wealth of information available on Class-D -- Yet!

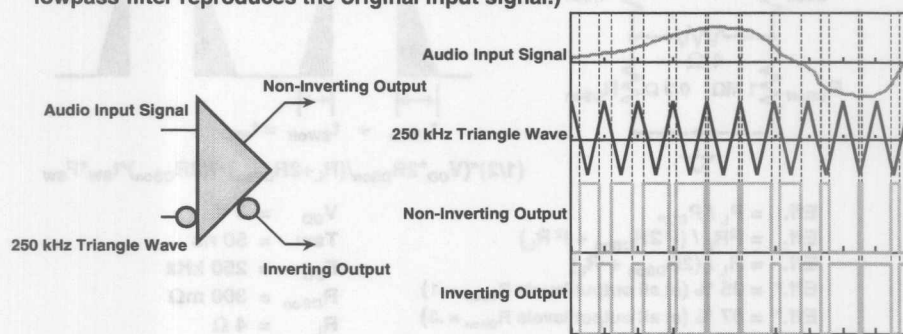
In the diagram above above you see one implementation of an integrated Class-D amplifier. The word "integrated" is important. Discrete implementations of Class-D have been around for many years but until recently the technology required to place the sensitive analog circuitry on the same piece of silicon with a high Power FET was not available.

Class-D relies on a technique called Pulse Width Modulation (PWM) to sample the input and then recreate the Audio Signal at the load. PWM resemble digital data in that it has an on state and an off state. This is the key to efficiency - when the FET is on, it has a low resistance and therefore delivers power efficiently. When it is off it delivers no power and so there is no loss. So, the Class-D amplifier turns on for a period of time (a pulse width) that is determined by the level of the input signal, grabs an efficient pulse of power, and then delivers it to the load. An output filter then smooths these pulses of power back into a time linear signal before it gets to the speaker.

Recap - The integrated Class-D amplifier samples the input waveform and creates discrete time pulses that represent the level of the signal. The pulses are then used to modulate the power FETs on and off to take efficient pulses of power from the supply and deliver them to the load. The output filter then smoothes the output back into a time linear waveform.

## Basic PWM Generator

Where the triangle crosses the input signal the comparator switches, creating a PWM waveform of the input signal at the frequency of the triangle wave. (Passing the PWM waveform through a lowpass filter reproduces the original input signal.)



1-53

## Basic PWM Generator

One must feel comfortable with the concept of PWM and how it is generated in order to have a good understanding of class-D operation. The diagram above presents a linear approach to PWM. A comparator simply compares a triangle wave with the input signal to create a "sampled" PWM representation of the waveform.

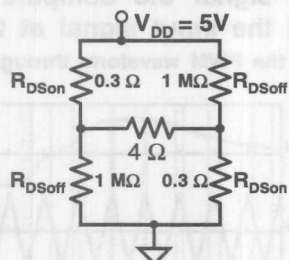
In the linear implementation the widths of the individual pulses can be infinitely variable -- therefore this is not technically a "digital" amplifier. The PWM signal can be created by sampling the input signal with an A/D converter (or using the digital output of a CD player for example) and creating a number for the signal level at a point in time. This number can then be used to generate a pulse width proportional to the magnitude of the number. This pulse could then replace the linear PWM in the block diagram on the previous page. One would then have a "digital" amplifier since the output pulse widths would then be limited in dynamic range by the resolution of the number (i.e. - number of bits).

Either technique is valid -- depending on the architecture of the system. The linear input Class-D that uses either the comparator or the data converter front end is more drop in compatible with current linear Audio Power Amps whereas the Digital input Class-D would be more applicable to systems where all of the music is already in a digital format.

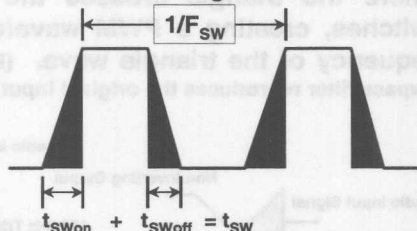
## Class-D Amplifier Efficiency

(1st order approximations)

Conduction Losses



Switching Losses



$$(1/2) * (V_{DD}^2 * 2R_{DSon} / (R_L + 2R_{DSon})^2) * t_{SW} * F_{SW}$$

$$\begin{aligned} \text{Eff.} &= P_L / P_{SUP} \\ \text{Eff.} &= I^2 R_L / (I^2 2R_{DSon} + I^2 R_L) \\ \text{Eff.} &= R_L / (2R_{DSon} + R_L) \\ \text{Eff.*} &= 95 \% \text{ (at all output levels } R_{DSon} = .1) \\ \text{Eff.*} &= 87 \% \text{ (at all output levels } R_{DSon} = .3) \end{aligned}$$

\*(not including switching and filter losses)

$$\begin{aligned} V_{DD} &= 5 \text{ V} \\ T_{SW} &= 50 \text{ ns} \\ F_{SW} &= 250 \text{ kHz} \\ R_{DSon} &= 300 \text{ m}\Omega \\ R_L &= 4 \Omega \\ P_{SW} &= 4.4 \text{ mW} \end{aligned}$$

1-54

## Class-D Amplifier Efficiency

Previously, we stated that the switch-mode amplifier grabs pulses of power and efficiently delivers them to the load. We are now going to look at two of the major factors that limit the efficiency in Class-D amplifiers --  $R_{DSon}$  losses and switching losses.

If the power FETs had an on resistance (DSOn - Drain to Source on resistance) and they switched from off to on and on to off instantly, then Class-D amplifiers would be 100% efficient.  $R_{DSon}$  robs the system of a set percentage of efficiency. The formula basically comes down to a ratio of the FET on resistances and the load resistance.

Switching losses are more complicated. As the FET ramps on and off it goes through a mid-resistance level that dissipates a lot of power. The longer the ramp, the more power it dissipates. Also, the switching frequency controls the switching losses. If one changes the switching speed from 250 kHz to 500 kHz then there are twice as many transitions in a given period of time and therefore the switching losses double!

The switching loss calculated above (4.4 mW) does not seem significant when compared to an amplifier that puts out 2 Watts for example. But, an amplifier that is rated for 2 W rms probably only runs at a fraction of that power when playing music. Amps are normally rated with Sine waves which have very little dynamic range from the peak to average power ratings (3 dB for a sin wave - known as the Crest Factor). Music though, can typically run at ratios of 15 to 21 dB (factors of 32 to 128). So, for a full power music signal the average power can be low - on the order of the switching losses. This is especially true when listening to the amplifier at less than full volume (which most of us normally do.).

|          | Tone   | Music  |
|----------|--------|--------|
|          | 3 dB   | 15 dB  |
| Class-AB | 83.3 % | 19.4 % |
| Class-D  | 88.1 % | 74.9 % |

Calculated Efficiency\*

\* results from TI Audio Power Program files: JEL\_A\_M\_Tot\_100s  
playing on a 5 Volt TTL Amplifier

1-55

## Crest Factor

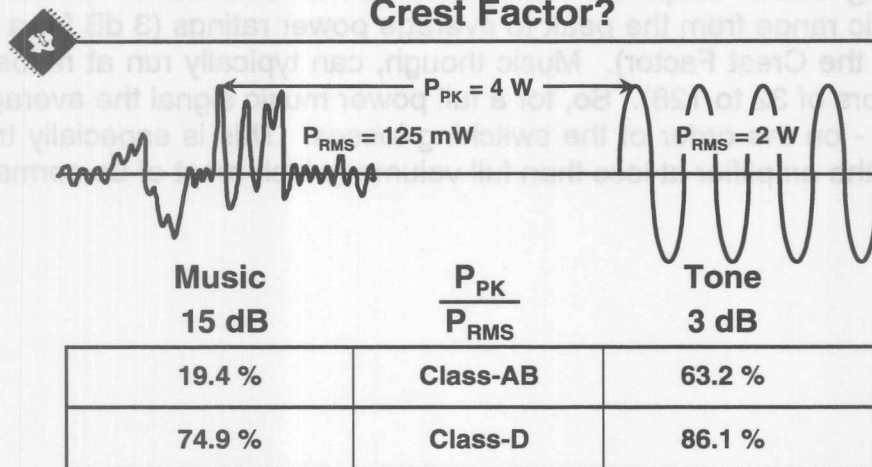
The diagram above is an example of how real music differs from sine waves (tones) in assessing the performance of an amplifier in terms of efficiency. The waveforms indicate that a tone has a nicely behaved envelope whereas the music has a widely varying envelope. This is typically referred to as dynamic range. The dynamic range of a signal is measured by Crest Factor which is:

$$\text{Crest Factor} = 10 \log(P_{\text{peak}}/P_{\text{avg}})$$

A high crest factor means that the difference between the peaks and the normal loudness is very high. You may also hear this referred to as Headroom at times. Since the switching losses of Class-D amplifiers are negligible in comparison to full power sine waves the efficiency at first appears quite high, but it is also high for linear amplifiers. When real music is applied then the efficiency number change quite drastically.

The example above is derived for two full power cases. The results are even more dramatic at normal listening levels. Consider your home stereo - it is a good bet that you rarely turn the volume up beyond about level 3 of 10 (unless you are listening to Beethoven). That means that peak powers are probably 6 or 8 dB down so for the example above that makes the music rms power drop from 125 mW to 15 to 30 mW. That 4.4 mW of switching losses then becomes a big loss percentage wise.

## Crest Factor?



### Calculated Efficiency\*

\* results from TI Audio Power Program files: JZZ\_2\_M, Tst\_1khz  
playing on 5 Volt BTL Amplifiers

1-55

## Crest Factor

The diagram above is an example of how real music differs from sine waves (tones) in assessing the performance of an amplifier in terms of efficiency. The waveforms indicate that a tone has a nicely behaved envelope whereas the music has a widely varying envelop. This is typically referred to as dynamic range. The dynamic range of a signal is measured by Crest Crest factor which is:

$$\text{Crest Factor} = 10\text{LOG}(P_{pk}/P_{rms})$$

A high crest factor means that the difference between the peaks and the normal loudness is very high. You may also hear this referred to as Headroom at times. Since the switching losses of Class-D amplifiers are negligible in comparison to full power sine waves the efficiency at first appears quite high, but it is also high for linear amplifiers. When real music is applied then the efficiency number change quite drastically.

The example above is derived for two full power cases. The results are even more dramatic at normal listening levels. Consider your home stereo - it is a good bet that you rarely turn the volume up beyond about level 3 of 10 (unless you are listening to Bolero!). That means that peak powers are probably 6 or 9 dB down so for the example above that makes the music rms power drop from 125 mw to 15 to 30 mW. That 4.4 mW of switching losses then becomes a big loss percentage wise.

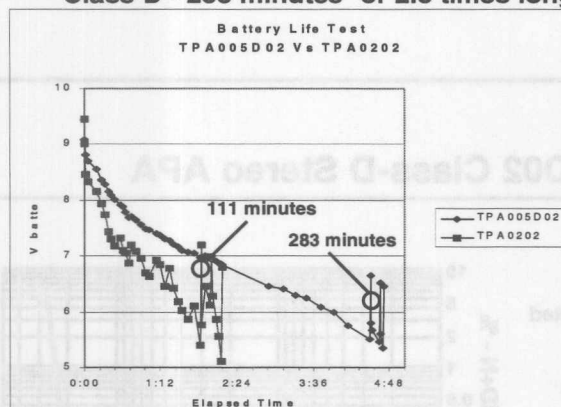
But, also keep in mind that linear amplifier efficiency drops faster than does class-D. Our analysis generally show that over normal listening levels Class-D maintains 2 to 3 times the efficiency. The next diagram documents a real live test we performed to prove out our simulated results.

## Battery Life

**Linear - 111 minutes\***

**Class-D - 283 minutes\* or 2.5 times longer**

\*Times measured to first under-voltage lockout of DC/DC module on PnP



**A head to head test of TI's Linear and Class-D 2W stereo solutions\*\*:**

**Linear - TPA0202**

**Class-D - TPA005D02**

**Both set-up on the PnP platform with Bass/Treble volume control modules, DC/DC converter modules and Rayovac 9-V Alkaline batteries.**

\*\* Standing supply current for both setups adjusted to 44 mA. Peak power ~ 1.5W.

1-56

## Battery Life

For the test we configured two PnP evaluation platforms. One with a TPA005D02 EVM and the other with a TPA0202 EVM. Using a standard Rayovac 9-Volt battery in each system and routing the exact same audio signal into both systems we let it run and monitored the battery voltage.

The DC/DC converter module will automatically shutdown when the battery voltage drops below about 5.2 volts (Under Voltage Lockout - UVLO) so we used that as an indicator that the battery had crapped out. The spikes you see on the battery voltage waveforms happen when the UVLO event happen the load o the battery goes away and the voltage drifts up until the load is reapplied. We reset the system, allowing three UVLOs to determine a good level of deadness.

Just like we had simulated with the Audio Power Program, the Class-D amplifier lasted 2.5 times longer. The Audio Power Program displays on the results screen rms current. If you know the AmpHr rating of the battery then, knowing the amps you can easily determine how long the battery will last.

In an application like Notebook Computer the battery life is probably more affected by the processor and other high power devices inside other than the

APA. In boombox mode however (mode where processor does not come on the play CDs) the APA does become the primary source of power drain so one could expect longer battery life.

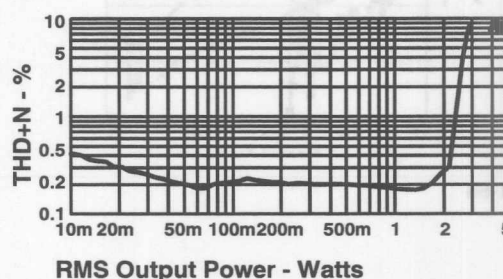
Class-D technology also makes things like rechargeable outdoor speakers for parties that use a walkman as the audio source a good possibility. Any application where the APA is a large percentage of the power drain makes Class-D attractive.

Other than battery life, Heat is yet another big factor in APA system design. Increased efficiency leads to higher powers for a give heat level or smaller heat sinks which could mean smaller enclosures - lots of things become more feasible with increased efficiency!

## TPA005D02 Class-D Stereo APA

### Product Highlights

- Industry's first fully integrated stereo Class-D amplifier
- Extremely efficient Class-D operation triples operating battery life
- Shutdown control ensures minimum power consumption
- 2-W stereo bridge-tied load (BTL) output with low THD+N (0.5%) provides clear, powerful sound levels



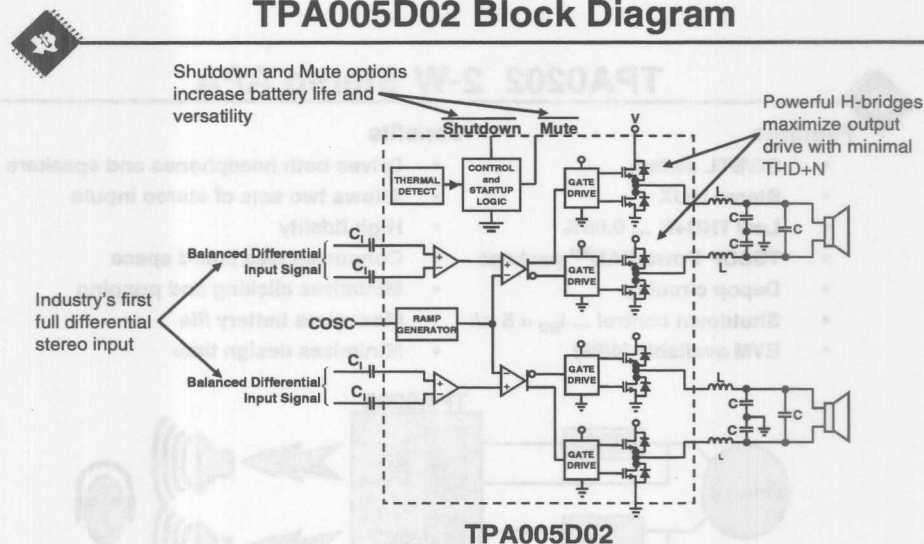
Test Conditions:

- 5-V supply
- 1-kHz frequency
- 4-Ω load

1-58

TI announced the industry's first, stereo Class-D amplifier on August, 17 1998. TI's 20+ years in designing switch-mode power supplies and experience with linear audio are two of the factors that helped expedite the release date. Another is TI's leading DMOS process which enables the low THD+N levels, high output drive and feature rich devices!

## TPA005D02 Block Diagram



1-59

This is a simplified block diagram of the TPA005D02. The key things to point out the shutdown control and mute options. The shutdown control nulls supply current (quiescent current) to only 400  $\mu\text{A}$  while the mute adds another option for the designer to incorporate. The TPA005D02 also has thermal and undervoltage protection.

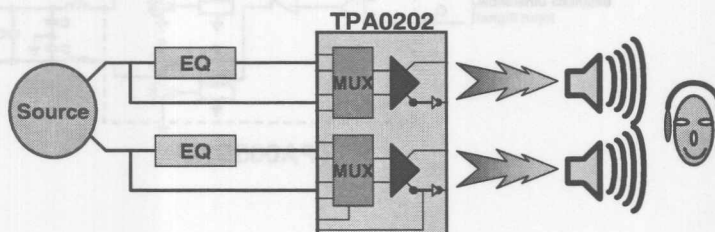
## TPA0202 2-W Stereo APA

### Features

- SE/BTL switch
- Stereo MUX
- Low THD+N ... 0.05%
- TSSOP PowerPAD™ package
- Depop circuitry
- Shutdown control ...  $I_{DD} = 5 \mu A$
- EVM available (4/98)

### Benefits

- Drives both headphones and speakers
- Allows two sets of stereo inputs
- High fidelity
- Consumes less board space
- Minimizes clicking and popping
- Maximizes battery life
- Minimizes design time



1-60

The TPA0202 is the latest generation designed for Note PCs. However, its differentiated feature set has won it design-ins in several mass market applications including P.O.S. terminals.

Key specs include 2-W output drive, SE/BTL switch, low 0.05% THD+N and versatile stereo input MUX. Designers also like the small thermally enhanced TSSOP PowerPAD package. As PCBs become more and more tightly packed, package sizes must continue to shrink. The dilemma is how to dissipate the heat generated in the amplifier as the surface area of the chip continues to shrink. This can be accomplished in two ways, make the amplifier more efficient (Class-D) and/or design innovative packaging to pull the heat from the die without large expensive heat sinks (PowerPAD).

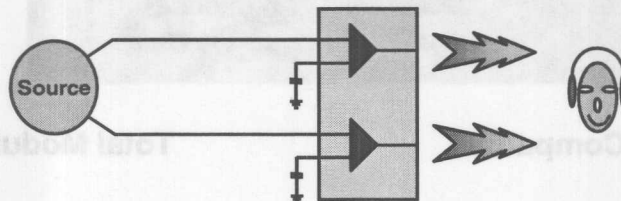
## TPA1x2 APA Headphone Drivers

### Features

- Ultra-low THD+N: <0.005% & High PSRR: 81db @ 1kHz (TPA152)
- 75-mW to 150-mW stereo output drive
- Internal mid-rail generator
- Depop circuitry
- Multiple pinouts

### Benefits

- Low THD+N and high PSRR provide high-fidelity sound
- Powerful output drive for any headphone application
- Minimizes external components
- Nulls “pops” and “clicks”
- Drops into many existing sockets

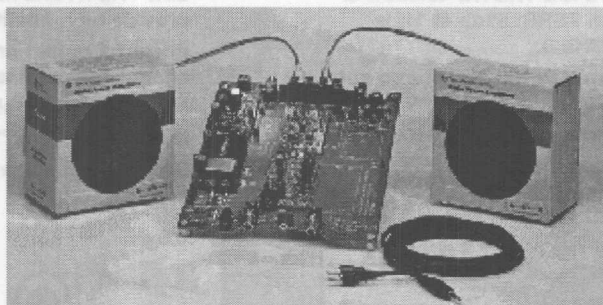


The TPA1x2 family includes the hi-fi TPA152, TPA102, TPA112, and TPA122. This family is targeted at headphone applications. These devices were designed with the most popular pinouts to help facilitate the design.

The TPA152 provides the best performance in the family with THD+N levels below 0.005% and PSRR above 81dB. Every member includes an internal mid-rail generator which minimizes external components by integrating the voltage divider circuit. Other improvements include integrated depop circuitry that eliminates the “popping” and “clicking” when the device switches power levels.



## Plug-n-Play Audio EVMs

**Easy to Use****Complete System****Roadmap Compatible****Total Modularity**

1-62

TI's APA Plug 'n Play kit is a one of kind and another example of the innovation driving the audio roadmap.

This kit allows designers to quickly evaluate ANY released TI audio power amplifier in seconds. And every new TI APA will have an EVM that plugs directly into the base platform. Each EVM comes with a user's guide which includes the reference design used on the board and a bill-of-materials. All you need to quickly evaluate and choose which TI APA works best for your application.

You can order the APA kit from your local authorized TI distributor or directly from TI's web site at:

<http://www.ti.com/sc/docs/msp/tools/audio.htm>



## Audio Power Analysis Program

- Power/thermal analysis
- Real music .WAV files
- System flexibility
- Windows based
- Free from the WEB

1-63

### System Definition Screen

**Audio - Linear**

File Show Mode Device Help

Source File: F:\ST0822.WAV File Info Calc

**Power Analysis**

Supply Voltage (V): 15.0 Level: 110 % Device: None

Load Impedance: 4.0

Vo Peak-to-Peak (V): 12.0

Quiescent Cur (mA): 0

Byte Skip Factor (1-1000): 10

Generate Output File: ☐

Thermal Analysis: ☒

**Thermal Analysis**

System Thermal Impedance (JA): 0 Deg C/Watt

Thermal Fuser Time: 50 Deg C/Sec

Thermal Fall Time: 2 Deg C/Sec

Max Ambient Temp: 40 Deg C

Output Mode: ☒ Stereo ☐ Mono

Audio Consideration: ☒ Back-to-Back Load ☐ Single Ended

Output Mode: ☒ Stereo ☐ Mono

[Enter file name (path) or browse via File - Open]

[www.ti.com/sc/docs/msp/pran/app\\_supp.htm](http://www.ti.com/sc/docs/msp/pran/app_supp.htm)

The Audio Power Analysis Program allows designers to quickly and accurately calculate power consumption and thermal data from real audio waveforms. Determining these results by hand involves very time consuming, complex calculus or grossly simplified sinewave approximations that often mislead the designer to over build part of the circuit.

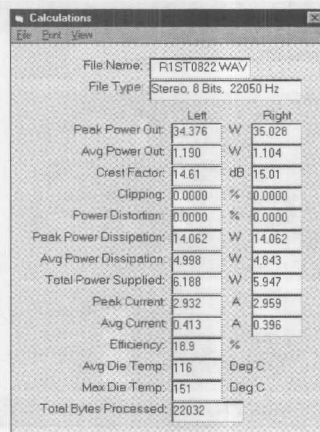
The software package is completely Windows based, will perform calculations on any .wav file and is downloadable FREE from TI's website! The web URL is:

**[http://www.ti.com/sc/docs/msp/pran/app\\_supp.htm](http://www.ti.com/sc/docs/msp/pran/app_supp.htm)**

Results for a typical .wav file are shown on the following foil.

## Audio Power Program - results

### System Results Screen



The screenshot shows a window titled 'Calculations' with a menu bar (File, Print, View). It displays results for a file named 'R1ST0822.WAV' (Stereo, 8 Bits, 22050 Hz). The results are organized into two columns: 'Left' and 'Right'. The data is as follows:

|                         | Left      | Right    |
|-------------------------|-----------|----------|
| Peak Power Out:         | 34.376 W  | 35.026 W |
| Avg Power Out:          | 1.190 W   | 1.104 W  |
| Crest Factor:           | 14.61 dB  | 15.01 dB |
| Clipping:               | 0.0000 %  | 0.0000 % |
| Power Distortion:       | 0.0000 %  | 0.0000 % |
| Peak Power Dissipation: | 14.062 W  | 14.062 W |
| Avg Power Dissipation:  | 4.998 W   | 4.643 W  |
| Total Power Supplied:   | 6.188 W   | 5.947 W  |
| Peak Current:           | 2.932 A   | 2.959 A  |
| Avg Current:            | 0.413 A   | 0.395 A  |
| Efficiency:             | 18.9 %    |          |
| Avg Die Temp:           | 116 Deg C |          |
| Max Die Temp:           | 151 Deg C |          |
| Total Bytes Processed:  | 22032     |          |

- Output power
- Crest factor
- Distortion
- Power dissipation
- Power supply currents
- Efficiency
- Die temperatures

1-64

This graphic and the prior one are actual screen captures from the Audio Power Analysis Program. As you can see the program displays the results in a neat, clean tabular format. Everything a designer needs; from crest factor to the die temperature is included.

Time to market directly impacts the success of our customers. The emphasis on our APA suite of design tools is focused on helping customers design first-to-market, innovate solutions.

# Audio Power Amplifiers - TPA

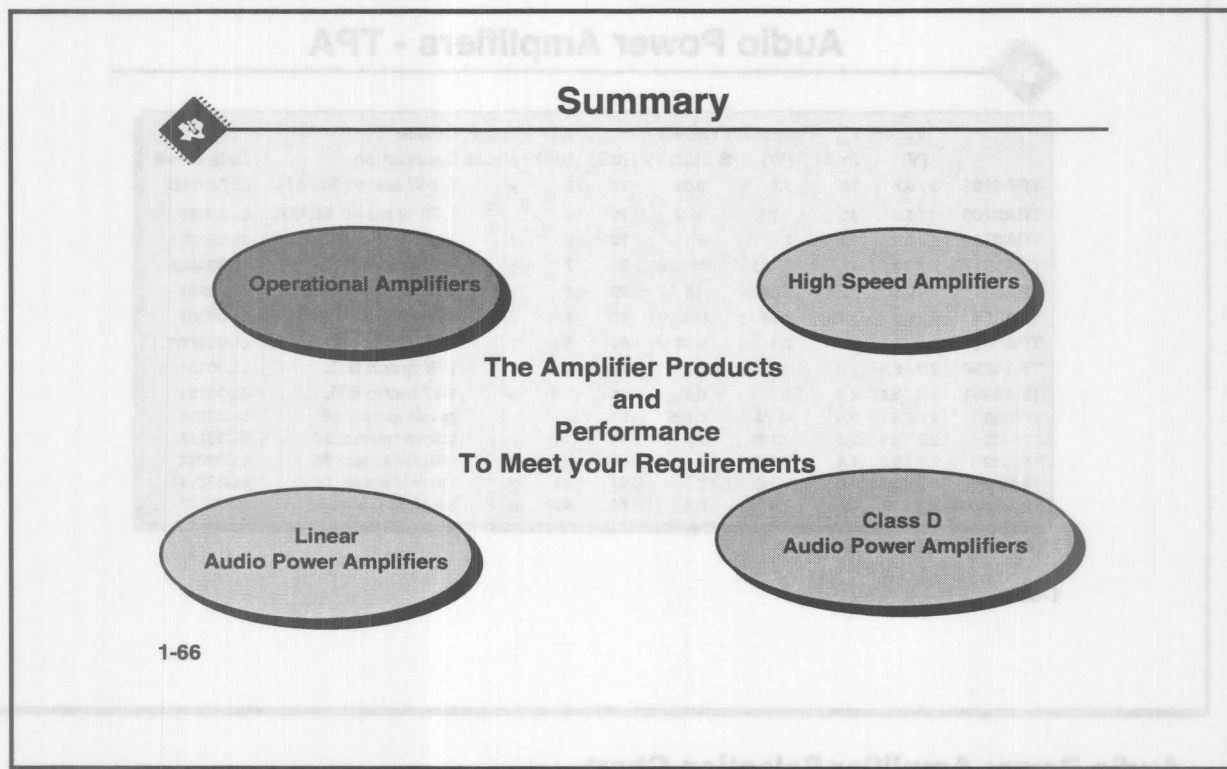
|           | V <sub>CC</sub><br>(V) | I <sub>DD</sub><br>(mA) | Output/ch<br>(W) | THD+N<br>@ 1kHz (%) | K <sub>SVR</sub><br>(dB) | I <sub>SD</sub><br>(μA) | Head-<br>phone | Device<br>Description | Data Sheet |
|-----------|------------------------|-------------------------|------------------|---------------------|--------------------------|-------------------------|----------------|-----------------------|------------|
| TPA0102   | 3 / 5.5                | 19                      | 1.5              | 0.05                | 75                       | 5                       | y              | 1.5-W stereo SE/BTL   | SLOS166D   |
| TPA0103   | 3 / 5.5                | 19                      | 1.75             | 0.05                | 75                       | 5                       | y              | 1.75-W mono SE/BTL    | SLOS167    |
| TPA0202   | 3 / 5.5                | 19                      | 2                | 0.1                 | 75                       | 5                       | y              | 2-W stereo SE/BTL     | SLOS205    |
| TPA1517   | 9.5/18                 | 40                      | 6, 4.5           | 10, 0.2             | 52                       | 7                       | n              | 6-W stereo BTL        | SLOS162A   |
| TPA301    | 2 / 5.5                | 1.25                    | 0.35             | 0.5                 | 70                       | 1                       | y              | 350-mW mono BTL       | SLOS208    |
| TPA311    | 2 / 5.5                | 1.25                    | 0.35             | 0.5                 | 70                       | 100                     | y              | 350-mW mono SE/BTL    | SLOS207    |
| TPA302    | 2.7 / 5.5              | 4                       | 0.3              | 0.06                | 65                       | 0.6                     | y              | 350-mW stereo SE      | SLOS174A   |
| TPA4860   | 2.7 / 5.5              | 3.5                     | 1                | 0.2                 | 56                       | 0.6                     | n              | 1-W mono BTL          | SLOS164    |
| TPA4861   | 2.7 / 5.5              | 3.5                     | 1                | 0.2                 | 56                       | 0.6                     | n              | 1-W mono BTL          | SLOS163    |
| TPA152    | 2 / 5.5                | 5.5                     | -0.75            | 0.005               | 81                       | -                       | y              | 75 mW stereo, SE      | SLOS210    |
| TPA102    | 2.5 / 5.5              | 1.5                     | 0.150            | 2                   | 68                       | 10                      | y              | 150 mW stereo, SE     | SLOS213    |
| TPA112    | 2.5 / 5.5              | 1.5                     | 0.150            | 2                   | 68                       | -                       | y              | 150 mW stereo, SE     | SLOS212    |
| TPA122    | 2.5 / 5.5              | 1.5                     | 0.150            | 2                   | 68                       | 10                      | y              | 150 mW stereo, SE     | SLOS211    |
| TPA005D02 | 4.5 / 5.5              | 25                      | 2.0              | 0.4                 | 60                       | 400                     | n              | 2W class-D stereo     | SLOS227    |

(@ +5V, 25°C, typ)

1-65

## Audio Power Amplifier Selection Chart

Conclusion  
Texas Instruments has the amplifiers you need. The task is to select the functionality required, then identify and rank the key areas for your system. The properties you identify can then be matched against available technologies and performance. Selecting the right amplifier is not difficult when approached systematically, and the right amplifier selection is key to optimum performance in signal conditioning.

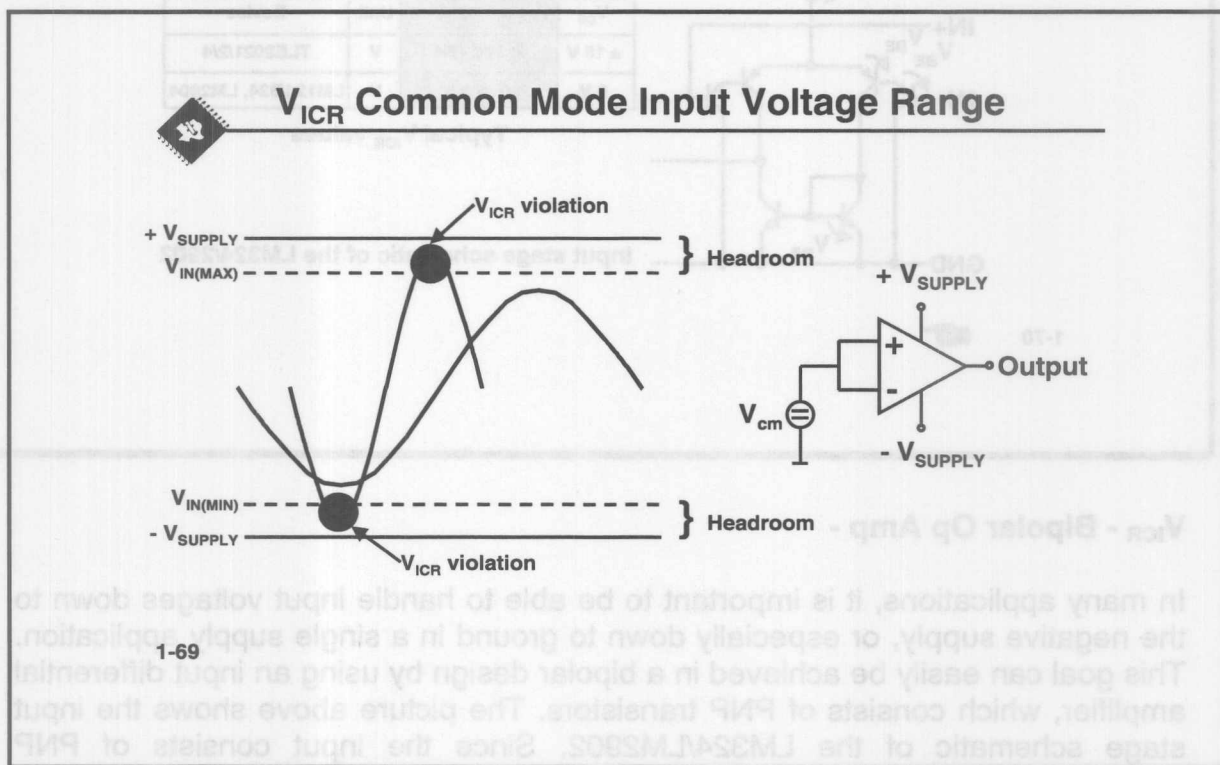


## Conclusion

Texas Instruments has the amplifiers you need. The task is to select the functionality required, then identify and rank the key care abouts for your system. The properties you identify can then be matched against available technologies and performance. Selecting the right amplifier is not difficult when approached systematically, and the right amplifier selection is key to optimum performance in signal conditioning.

## Reference Material

### Input Stage Considerations



### Common-Mode Input Voltage Range $V_{ICR}$

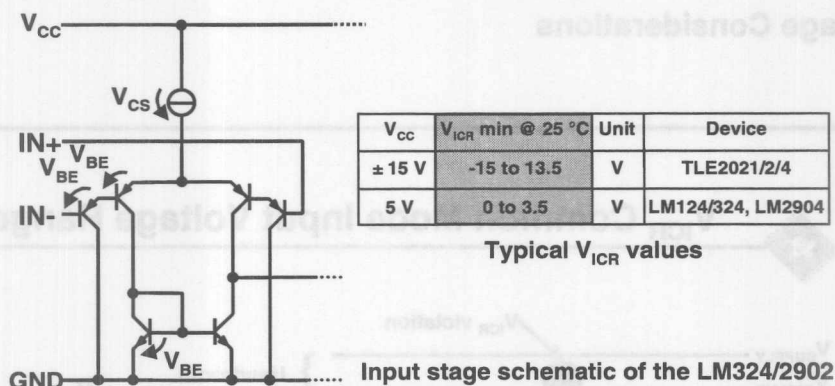
Op amp input topologies typically require some voltage headroom from either the positive or negative supply rail, or both, for proper biasing. Taking a signal outside the specified common-mode voltage range ( $V_{ICR}$ ) can cause unanticipated behaviour ranging from an exponential increase in dc offset error to phase inversion at the output. Failure to recognise  $V_{ICR}$  restrictions, especially when moving from wide split supplies to lower voltage single supply designs is probably the most common error designers make. This is especially true when using BiFET op amps, which are ill suited for low voltage single supply designs.

The problems which are caused by the Common-Mode Input Voltage Range are often neglected or even unknown.

Therefore, the next pages cover a discussion of the Common Mode Input Voltage Range for each of the today's different technologies and their limitations.

## $V_{ICR}$ Common Mode Input Voltage Range

### Bipolar Op Amp



1-70

### $V_{ICR}$ - Bipolar Op Amp -

In many applications, it is important to be able to handle input voltages down to the negative supply, or especially down to ground in a single supply application. This goal can easily be achieved in a bipolar design by using an input differential amplifier, which consists of PNP transistors. The picture above shows the input stage schematic of the LM324/LM2902. Since the input consists of PNP transistors, a linear operation is only possible if the voltage at the base is 0.7 V more negative than the voltage at the emitter. Therefore, it is possible to apply an input voltage which goes down to the negative supply.

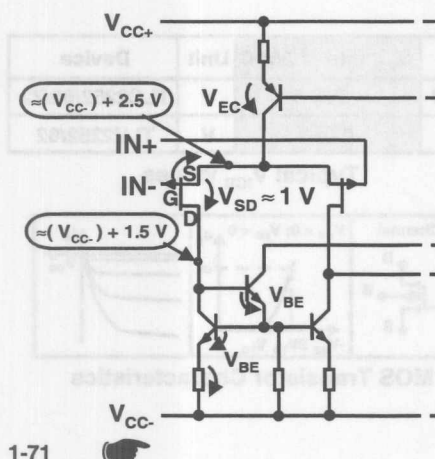
However, on the other hand we can see directly the limitation of the  $V_{ICR}$  in the positive direction. The picture shows the voltage drop  $V_{CS}$  at the current source ( $\approx 400$  mV for a bipolar, non cascaded current source) and the two voltage drops  $V_{BE}$ , each of 0.7 V. The resulting maximum voltage at the input of the op amp is therefore around 2 V below the positive supply voltage.

The table shows the behaviour of different op amps and different supply voltages. It can be seen that the headroom from the positive supply is nearly independent of the supply voltage.



## $V_{ICR}$ Common Mode Input Voltage Range

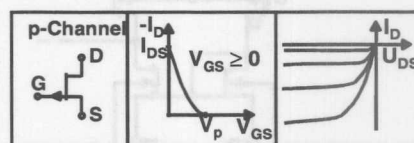
### BiFET Op Amp



1-71

| $V_{CC}$   | $V_{ICR}$ typ @ 25° C | Unit | Device         |
|------------|-----------------------|------|----------------|
| $\pm 15$ V | -11.9 to 15           | V    | TL071, TLE2071 |
| $\pm 5$ V  | -1.9 to 5             | V    | TLE2071/81     |

Typical  $V_{ICR}$  values



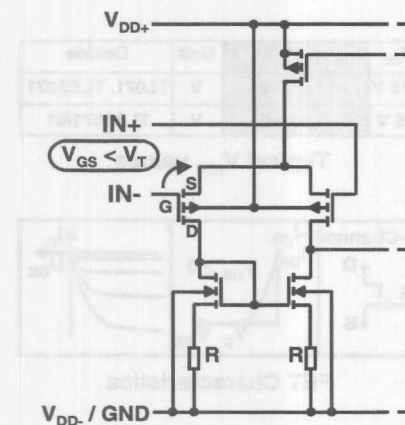
FET Characteristics

### $V_{ICR}$ - BiFET Op Amp -

- Texas Instruments BiFET op amps combine P-type JFETs on the input stage with bipolar transistors. The picture above shows the input stage of the BiFET op amp TL071/82. For this kind of op amp, a linear operation is only possible, if the gate-source voltage  $V_{GS} \geq 0$ . Therefore, the  $V_{ICR}$  includes the positive supply rail, but **not** the negative supply rail. The picture shows the voltage drop at the resistor R, the two voltages  $V_{BE}$  at the current mirror which is built up by two NPN transistors (each of them with a 0.7 V base-emitter voltage) and the voltage  $V_{SD}$  at the FET transistor. To operate a FET transistor in the area where its drain current  $I_D$  is mostly dependent on the gate-source voltage  $V_{GS}$  and not on the source-drain voltage  $V_{SD}$ , a minimum voltage  $V_{SD}$  of  $\approx 1$  V is required. This can be seen in the characteristic  $V_{SD}$  versus  $I_D$ . The resulting headroom to the negative supply voltage at the input of the op amp is around  $V_{CC-} + 2.5$  V.

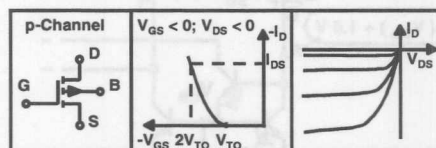
## VICR Common Mode Input Voltage Range

### Advanced LinCMOS™



| $V_{CC}$  | $V_{ICR}$ min @ 25° C | Unit | Device        |
|-----------|-----------------------|------|---------------|
| $\pm 5$ V | -5 to 4               | V    | TLC2252/62/72 |
| 3 V       | 0 to 4                | V    | TLV2252/62    |

Typical  $V_{ICR}$  values



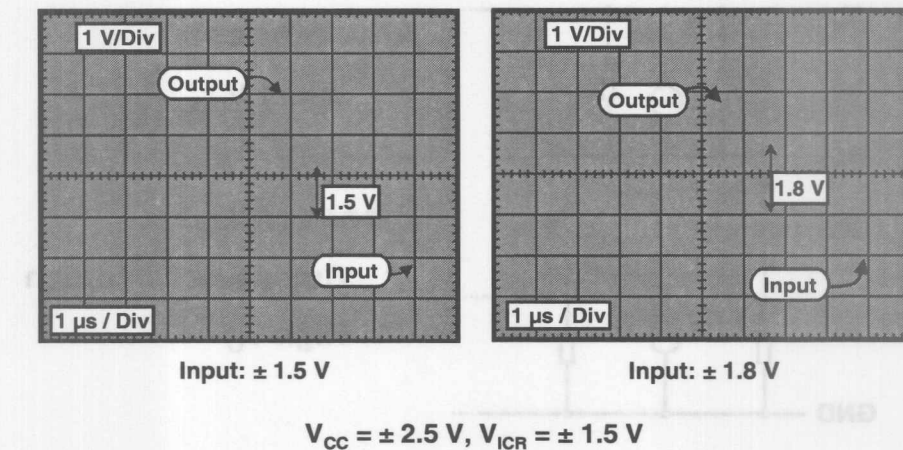
MOS Transistor Characteristics

1-72

## $V_{ICR}$ - CMOS Op Amp -

- Texas Instruments CMOS op amps combine p-channel MOS transistors in the input stage. The picture above shows the input stage of the TLC/TLV2262 CMOS op amp. A linear operation is only possible, if the voltage  $V_{GS} < V_T$  (see the characteristic of this p-channel MOS transistor). This means that the applied common-mode voltage may reach the negative supply/GND while functioning properly.
- TI CMOS op amps are therefore well suited for single supply applications where small signals near ground have to be measured and amplified. However, the common-mode voltage in the positive direction is limited by the threshold voltage  $V_T$  of the input transistors. The table shows the headroom to the positive supply of around 800 mV to 1.5 V.

## TLV2362 - Common-Mode Input Voltage Range



1-73

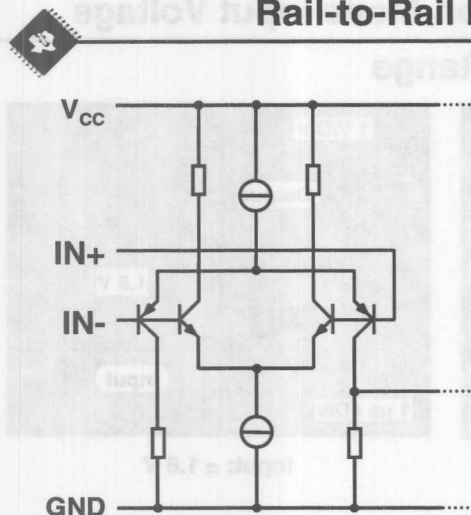
### TLV2362 – Common-Mode Input Voltage Range

The reasons for restrictions in the Common-Mode Input Voltage Range  $V_{ICR}$  were explained in detail for the different technologies on the pages before. The effect of an input voltage which exceeds the  $V_{ICR}$  can be seen on this picture. The measurement shows the curves of the input and output of the op amp TLV2362 which is operated as a voltage follower. The common-mode input voltage range of the TLV2362 is specified with  $\pm 1.5 \text{ V}$  when operating at  $\pm 2.5 \text{ V}$  supplies with a temperature of  $25^\circ\text{C}$ . The picture on the left shows that the output provides the expected output voltage with an input voltage of  $1.5 \text{ V}_P$ . However, if the input voltage is increased to  $1.8 \text{ V}_P$ , which means that the common-mode input voltage range is exceeded, the output voltage shows a phase inversion. This can be seen in the picture on the right.

#### The main specifications of this op amp are:

- Low Supply Voltage Operation  $V_{CC\pm} = \pm 1 \text{ V Min}$
- Wide Bandwidth,  $7 \text{ MHz typ}$  at  $V_{CC\pm} = \pm 2.5 \text{ V}$
- High Slew Rate  $3\text{V}/\mu\text{s typ}$  at  $V_{CC\pm} = \pm 2.5 \text{ V}$
- Wide Output Voltage Swing,  $\pm 2.4 \text{ V typ}$  at  $V_{CC\pm} = \pm 2.5 \text{ V}, R_L = 10\text{k}\Omega$
- Low Noise,  $8 \text{ nV}/\sqrt{\text{Hz typ}}$  at  $f = 1 \text{ kHz}$
- Available in SOT-23 (TLV2361) and TSSOP (TLV2362) packages

### Rail-to-Rail Input Amplifier



1-74

#### Advantages:

- Wider  $V_{ICR}$

#### Disadvantages:

- Crossover Distortion
- High  $V_o$

### Rail-to-Rail Input Amplifier

The problem with the limited Common-Mode Input Voltage Range  $V_{ICR}$  can be overcome with a so called Rail-to-Rail input stage. Such an input stage allows an input voltage from the negative supply voltage to the positive supply voltage. This feature can be achieved with two differential input pairs, one built up from PNP transistors and the other from NPN transistors. Therefore, the input switches its operation from one input pair to the other input pair depending on the input voltage.

However, in such designs the input offset voltage may increase dramatically in comparison to the conventional input stage. Especially in DC-applications where a low input offset voltage is required, a Rail-to-Rail input op amp may not fulfil the requirements in terms of DC-parameters. In addition to that, there exists a crossover distortion in the switching region between the two input pairs. The applications for a Rail-to-Rail input are limited. These could be high level sensing applications or an op amp which is configured to work as a buffer.

Nevertheless, Texas Instruments is also developing the full Rail-to-Rail input op amp, because in some specific applications this feature is important.

## TLV24x2 - Wide-Input-Voltage Op Amp

### TLV24xx

#### Rail-to-Rail Output

$V_{ICR} = 0$  to  $4.5$  V (min),  $V_{CC} = 5$  V

$V_{IO} = 950$   $\mu$ A max at  $T_A = 25^\circ$  (TLV24xxA)

$R_O = 600$   $\Omega$

### TLV2432

125  $\mu$ A / channel (max)

Gain Bandwidth = 0.5 MHz typ

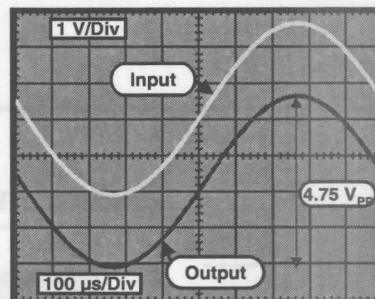
Low noise 18 nV /  $\sqrt{\text{Hz}}$  typ at 1 kHz

### TLV2442

750  $\mu$ A / channel (typ)

High Gain Bandwidth = 1.8 MHz typ

Low noise 16 nV /  $\sqrt{\text{Hz}}$  typ at 1 kHz



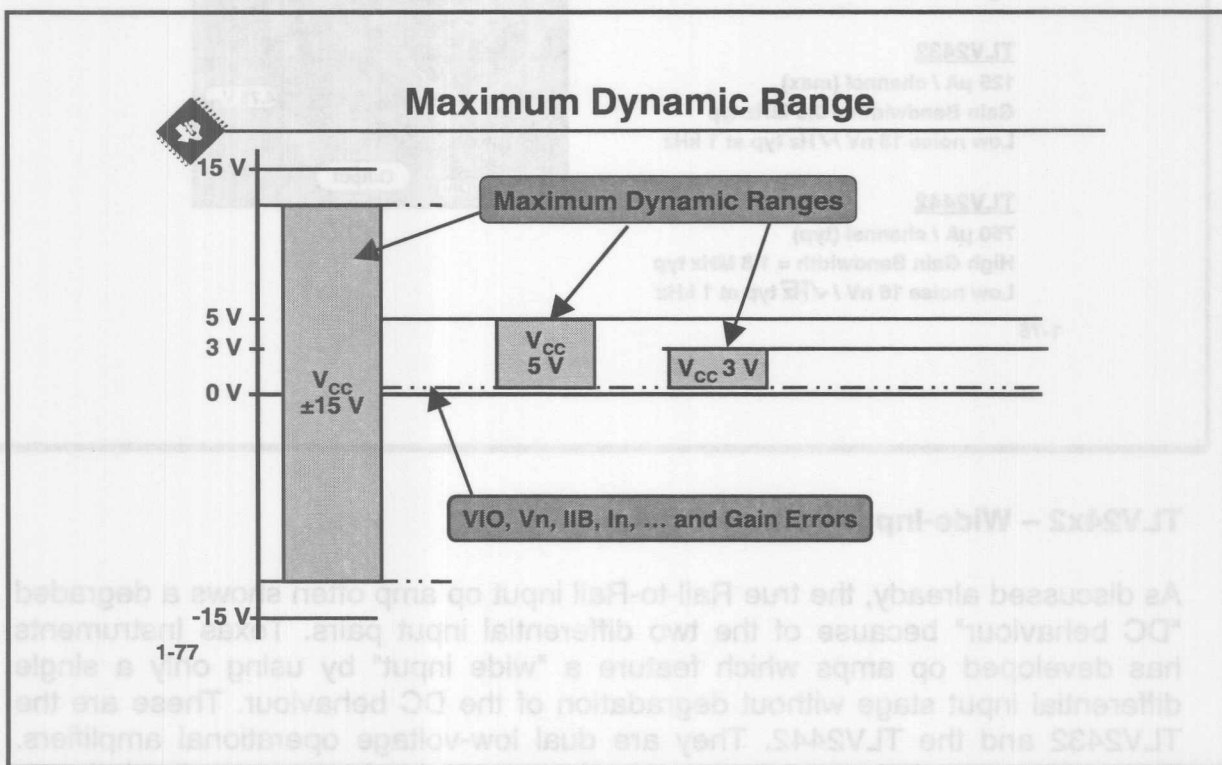
1-75

## TLV24x2 – Wide-Input-Voltage Op Amp

As discussed already, the true Rail-to-Rail input op amp often shows a degraded "DC behaviour" because of the two differential input pairs. Texas Instruments has developed op amps which feature a "wide input" by using only a single differential input stage without degradation of the DC behaviour. These are the TLV2432 and the TLV2442. They are dual low-voltage operational amplifiers. The common-mode input voltage range for this device has been extended over that of typical standard CMOS amplifiers making it suitable for a wider range of applications. In addition, the devices exhibit Rail-to-Rail output performance for increased dynamic range in single- or split-supply applications. This family is fully characterised for 3-V and 5-V supplies and is optimised for low-voltage operation. The TLV2432 requires only 100  $\mu$ A (typ) of supply current per channel, making it ideal for battery powered applications. Both, the TLV2432 and the TLV2442 have also an increased output drive over previous Rail-to-Rail operational amplifiers to drive 600- $\Omega$  loads for telecom applications.

## Output Stage Considerations

The op amp output stage is critical to performance and therefore must be considered when choosing an op amp. Maximum dynamic range, rail-to-rail operation, and drive capability are all related to the output stage and are discussed in the following section.

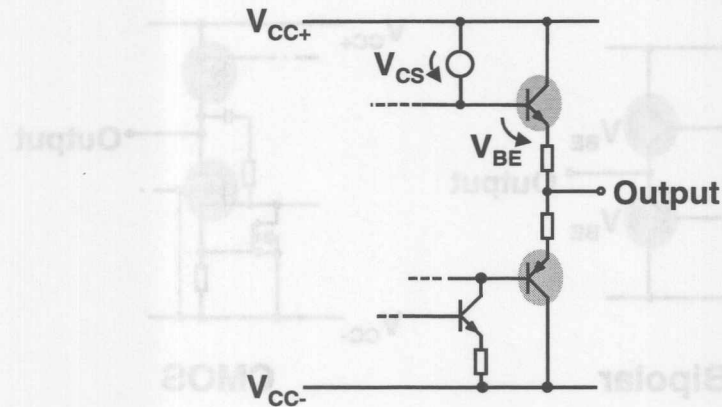


## Maximum Dynamic Range

A very important parameter in system design is the signal-to-noise ratio (SNR) and the dynamic range. These are first of all limited by the supply voltage used. The diagram shows the maximum dynamic range for the different supply voltages of  $\pm 15$  V, single supply  $+5$  V and  $+3$  V. It can be seen that the reduction to  $+5$  V or  $+3$  V reduces the maximum dynamic range of the op amp considerably and will ultimately limit the performance of the system. In addition to the supply voltage, the dynamic range is limited to the sum of the op amp's errors caused by the input offset voltage, input bias current, gain, etc. It is obviously that for a single supply voltage of  $+5$  V or  $+3$  V, it is important that as much of the reduced supply voltage is available for a useful signal output swing of the op amp. This can be obtained by using Rail-to-Rail amplifier. The output of the Rail-to-Rail op amps can be driven up to the supply voltages.



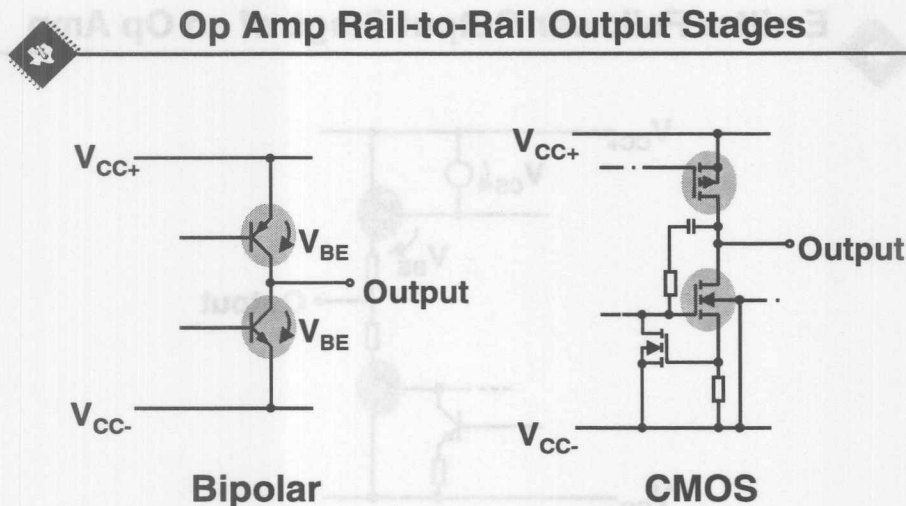
## Emitter Follower Output Stage of an Op Amp



1-78

## Emitter Follower Output Stage of an Op Amp

The circuit diagram shows a typical emitter follower stage which is widely used in op amps. The output voltage of this op amp is limited, because of the voltage drop of a few hundred mV ( $\approx 400$  mV for a bipolar, non-cascaded current source) across the current source and the forward voltage of the output transistor's base-emitter diode of 0.7 V. Therefore the available signal peak-to-peak swing at the output of the op amp is reduced. This is not a problem if a power supply of  $\pm 15$  V or  $\pm 12$  V is used in a system. However, if a single supply of +5 V or even +3 V is used, the headroom between signal and supply rail will dramatically reduce the output swing of the op amp and will therefore also reduce the dynamic range and the SNR of the system.



1-79

### Rail-to-Rail Output Stage of an Op Amp

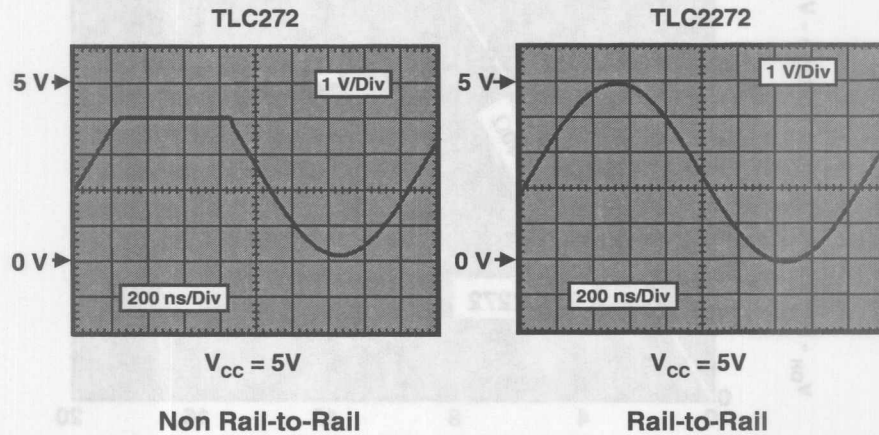
A solution to the problem of having headroom at the output between the signal and the supply rails, especially in a single supply low voltage system is an op amp which has a Rail-to-Rail output stage. This allows the output to swing close to the supply rails, which improves the dynamic range and signal to noise ratio. A bipolar Rail-to-Rail output stage can be designed by using a common-emitter output stage. In such a stage, the output swing is limited to the saturation voltage  $V_{CE}$  of the output transistors. The saturation voltage depends on the amount of load current, which might result into a saturation voltage of a few mV up to 500 mV.

The signal swing in a CMOS Rail-to-Rail op amp is limited only to the voltage drop caused by the resistance  $R_{DS(on)}$  of the output stage transistor. Therefore it is possible to achieve a signal swing very close to the supply rails of the op amp. However, in this case also the maximum peak-to-peak value depends on the load which has to be driven by the output of the op amp.



## Op Amp Output

### Rail-to-Rail vs non Rail-to-Rail



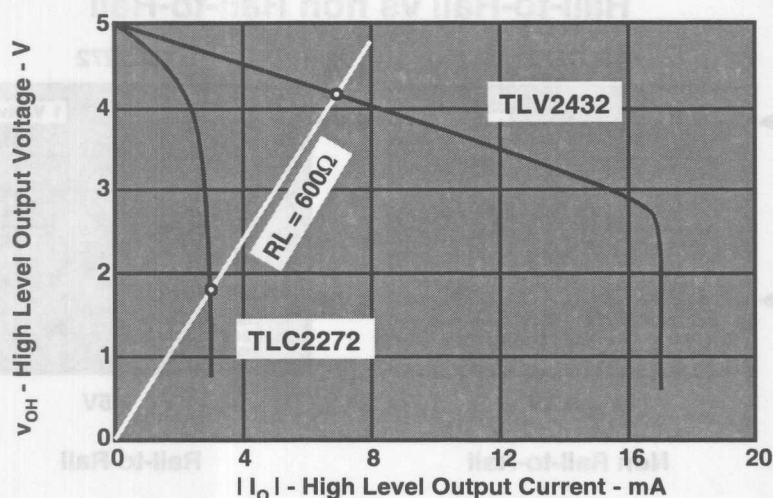
1-80

### Rail-to-Rail vs non Rail-to-Rail

The measurement shows the different behaviour of a Rail-to-Rail op amp versus a non Rail-to-Rail op amp. The TLC2272 which is Rail-to-Rail capable at the output is able to deliver an output signal which goes near to the 5-V supply voltage. The TLC272 clips the positive signal at around 4 V. This is equivalent to a reduction in the dynamic range of approximately 2 dB. It is therefore recommended for single supply application to choose Rail-to-Rail op amps, if the SNR and dynamic range is important.



### Output Drive Capability



1-81

### Output Drive Capability

- The maximum output drive capability of a CMOS op amp is less than that of a bipolar one. This might introduce a problem for Rail-to-Rail op amps which have to source a higher current at high output voltages. This might be the case when interfacing to A/D converters on 5V supplies. For CMOS op amps which cannot deliver that current, distortion is generated. Texas Instruments has now introduced CMOS op amps which are able to deliver a higher output current. This is also important for driving a flash A/D converter, where the input can be seen as a capacitance which switches between the analog input and the internal comparators of the converter. If the analog voltage is different to the charge of the capacitor at the time when the capacitor switches to the analog input, a high current from the op amp is required.



## Advanced LinCMOS™ Rail-to-Rail Output Op Amps

| DEVICE    | SUPPLY (V)<br>(Rated) (Min) | V <sub>OH</sub> (Min)<br>I <sub>OUT</sub> = 20 $\mu$ A | V <sub>IO</sub> (max)<br>mV | GBW<br>MHz | Feature          |
|-----------|-----------------------------|--------------------------------------------------------|-----------------------------|------------|------------------|
| TLC2201/2 | $\pm 5/+5$ 4.6              | 4.8                                                    | 0.6                         | 1.9        |                  |
| TLC2252/4 | $\pm 5/+5$ 4.4              | 4.98                                                   | 1.5                         | 0.2        |                  |
| TLC2262/4 | $\pm 5/+5$ 4.4              | 4.99                                                   | 1.5                         | 0.71       |                  |
| TLC2272/4 | $\pm 5/+5$ 4.4              | 4.99                                                   | 1.5                         | 2.18       |                  |
| TLC4501   | $\pm 5/+5$ 4                | 4.99                                                   | 0.08                        | 4.7        | Self Calibrating |
| TLC4502   | $\pm 5/+5$ 4                | 4.99                                                   | 0.1                         | 4.7        | Self Calibrating |
| TLV2252/4 | +3/+5 2.7                   | 2.98/4.98                                              | 1.5                         | 0.18       |                  |
| TLV2262/4 | +3/+5 2.7                   | 2.99/4.98                                              | 1.5                         | 0.67       |                  |
| TLV2422   | +3/+5 2.7                   | 2.98/4.97                                              | 2                           | 0.052      | Wide Input       |
| TLV2432   | +3/+5 2.7                   | 2.98/4.97                                              | 2                           | 0.5        | Wide Input       |
| TLV2442   | +3/+5 2.7                   | 2.98/4.97                                              | 2                           | 1.8        | Wide Input       |
| TLV2772   | +2.7/+5 2.2                 | 2.6(0.07 mA)/<br>4.9(1.3 mA)                           | 2.5                         | 5.1        |                  |

1-82


  
Fastest CMOS

## Advanced LinCMOS™ Rail-to-Rail Output Op Amps

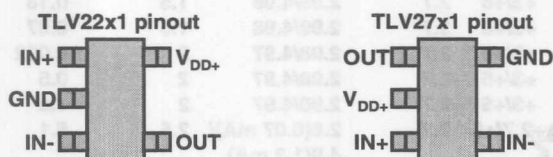
Texas Instruments manufactures a growing number of Rail-to-Rail output operational amplifiers. The TLC22xx devices are specified for a single 5-V supply and for a  $\pm 5$ -V supply. The TLV22xx and TLV24x2 are specified for a single 3-V supply and for a single 5-V supply.



## Advanced LinCMOS™

### SOT-23 Rail-to-Rail Output Op Amps

| DEVICE  | SUPPLY (V)    | $V_{OH}$ (Min)        | $V_{IO}$ (max) | GBW | Feature |                |
|---------|---------------|-----------------------|----------------|-----|---------|----------------|
|         | (Rated) (Min) | $I_{OUT} = 20\ \mu A$ | mV             | MHz |         |                |
| TLV2211 | +3/+5         | 2.7                   | 2.94/4.95      | 3   | 0.065   | Micropower     |
| TLV2221 | +3/+5         | 2.7                   | 2.97/4.88      | 3   | 0.48    | Very Low Power |
| TLV2231 | +3/+5         | 2.7                   | 2.87/4.9       | 3   | 1.9     | Low Power      |
| TLV2711 | +3/+5         | 2.7                   | 2.94/4.95      | 3   | 0.065   | Micropower     |
| TLV2721 | +3/+5         | 2.7                   | 2.97/4.88      | 3   | 0.48    | Very Low Power |
| TLV2731 | +3/+5         | 2.7                   | 2.87/4.9       | 3   | 1.9     | Low Power      |



1-83

### Advanced LinCMOS™ SOT-23 Rail-to-Rail Output Op Amps

Texas Instruments also introduced several Rail-to-Rail op amps in the SOT-23 package. These are basically 2 families, the TLV22x1 and the TLV27x1. Both families have op amps in a 'Micropower', 'Very Low Power' or 'Low Power' version. The two families are different in their pinning as shown in the picture.

## SOT-23 Op Amps



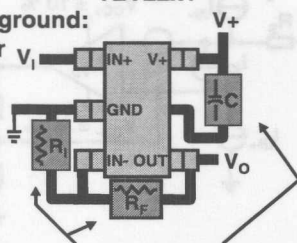
Inputs isolated by ground:  
reduced leakage or  
coupling

Optimized for amplifier feedback  
and decoupling: easy routing and  
component placement

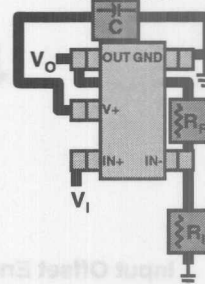
**Texas Instruments has the Footprint you need !**

1-84

TLV22x1



TLV27x1

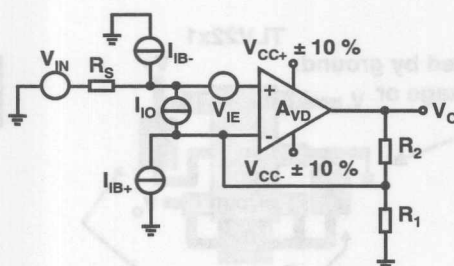


### Layout Consideration of SOT-23 Packages

As already mentioned before, the Texas Instruments SOT-23 op amps are available in two different package options. The pinout of the op amp on the left side of the picture offers several advantages, because the inputs are isolated by the ground pin. This reduces leakage and coupling. The pinout is furthermore optimised for amplifier feedback offering easy routing and component placement.

## DC-Considerations of Operational Amplifiers

### DC Input Referred Errors



#### Input Offset Errors:

$$V_{IE} = V_{IO} + V_{CMRR} + V_{KSVR} + V_N$$

$$I_{IB} = (I_{IB+} + I_{IB-})/2$$

$$I_O = |I_{IB+} - I_{IB-}|$$

#### Gain Related Error: (Non-inverting Amplifier)

$$A = \left(1 + \frac{R_2}{R_1}\right) \left(\frac{1}{1 + \frac{1}{A_{VD}\beta}}\right)$$

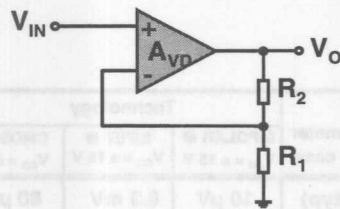
$$\beta = R_1 / (R_1 + R_2)$$

1-86

### DC Input Referred Errors

The DC accuracy of an analog system is mainly limited by two parameters. These are the input offset errors and the gain-related error. The total input offset voltage is caused by the input offset voltage, the input bias current, the common-mode rejection ratio and the supply voltage rejection ratio of the op amp. The total input offset voltage raises a DC output error. A further important parameter is the open loop voltage Gain  $A_{VD}$  of the op amp. Ideally, this gain is infinite, however in reality it will be typically in the range of 100 dB at DC and rolls off at frequencies above 100 Hz. The following pages give a detailed analysis of the influence of the input offset error and gain error on the output voltage of the op amp.

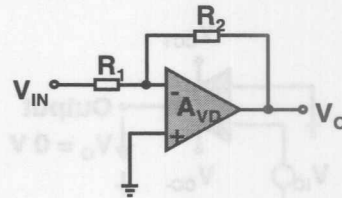
## Signal Gain



Non-inverting Amplifier Gain

$$A = \left(1 + \frac{R_2}{R_1}\right) \left(\frac{1}{1 + \frac{1}{A_{VD}\beta}}\right)$$

$$\beta = R_1 / (R_1 + R_2)$$



Inverting Amplifier Gain

$$A = -\left(\frac{R_2}{R_1}\right) \left(\frac{1}{1 + \frac{1}{A_{VD}\beta}}\right)$$

1-87



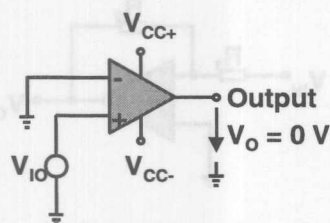
## Gain Errors

Every op amp has a particular open loop gain which is called  $A_{VD}$ . Ideally, as already seen before, this gain would be infinite, but in reality it will for many op amps be 100 dB at DC and rolls off at frequencies above around 100 Hz. The frequency at which  $A_{VD}$  reaches 0 dB is known as the Unity Gain Bandwidth of the op amp. The gain limits the accuracy of an op amp and the bandwidth limits the maximum operating frequency. The closed loop gain results from the feedback which is used in the op amp circuitry.

Bipolar op amps have typically the lowest  $V_{IO}$  and temperature drift. CMOS devices can achieve offset voltages of around 100  $\mu$ V, which is better than BIFET, but cannot compete with the best bipolar devices. However, chopper stabilised CMOS op amps achieve a very low input offset voltage down to 1  $\mu$ V (max). One of the latest CMOS op amps introduced by Texas Instruments integrates a self calibration to allow a maximum  $V_{IO}$  of 40  $\mu$ V. This technology is described on the following page.

Input Offset Voltage ( $V_{IO}$ )

Input offset voltage is amplified by op amp gain



For a 5 V ADC:

10 bit: 1 LSB = 4.88 mV

12 bit: 1 LSB = 1.22 mV

| Parameter<br>(best case)         | Technology                               |                                        |                                  |
|----------------------------------|------------------------------------------|----------------------------------------|----------------------------------|
|                                  | BIPOLAR @<br>$V_{CC} = \pm 15 \text{ V}$ | BIFET @<br>$V_{CC} = \pm 15 \text{ V}$ | CMOS @<br>$V_{CC} = 5 \text{ V}$ |
| $V_{IO}(\text{typ})$             | 10 $\mu\text{V}$                         | 0.3 mV                                 | 80 $\mu\text{V}$                 |
| $V_{IO}(\text{max})$             | 25 $\mu\text{V}$                         | 1.5 mV                                 | 200 $\mu\text{V}$                |
| $\frac{\Delta V_{IO}}{\Delta T}$ | 0.1 $\mu\text{V}/^\circ\text{C}$         | 5 $\mu\text{V}/^\circ\text{C}$         | 0.5 $\mu\text{V}/^\circ\text{C}$ |

1-88

Input Offset Voltage ( $V_{IO}$ )

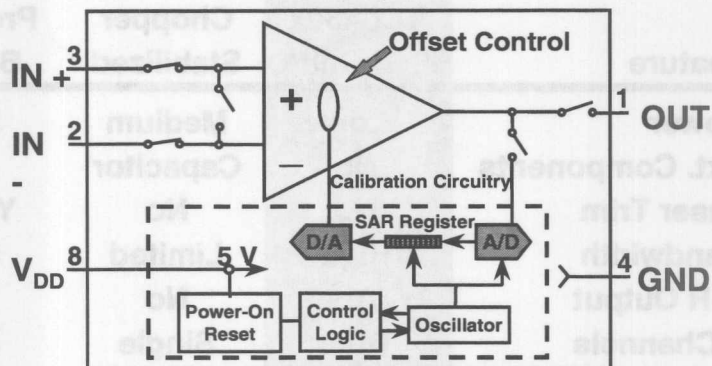
An ideal op amp, where the inputs are both connected to ground, would provide theoretically an output voltage of 0 V, because the differential and common-mode voltage in that case is zero. However, the real op amp shows an output voltage which is not equal to zero. A small input offset voltage  $V_{IO}$  between the differential inputs is imaginable, and causes the output voltage.

The input offset voltage  $V_{IO}$  of an operational amplifier is the voltage that must be applied between the two input terminals to get an output voltage of 0 Volt, as shown in the picture. The voltage  $V_{IO}$  may be positive or negative and this is caused mainly by the mismatch of the input transistors of the op amp's differential input stage. The voltage  $V_{IO}$  is amplified with the gain of the amplifier. This may be the open loop gain, or the gain at which the op amp is adjusted. In addition, the input offset voltage is also dependent on the ambient temperature. The best devices vary around 0.1  $\mu\text{V}/^\circ\text{C}$  and this may go up to several tenths of  $\mu\text{V}/^\circ\text{C}$ .

Bipolar op amps have typically the lowest  $V_{IO}$  and temperature drift. CMOS devices can achieve offset voltages of around 100  $\mu\text{V}$ , which is better than BiFET, but cannot compete with the best bipolar devices. However, chopper stabilised CMOS op amps achieve a very low input offset voltage down to 1  $\mu\text{V}$  (max). One of the latest CMOS op amps introduced by Texas Instruments integrates a self calibration to allow a maximum  $V_{IO}$  of 40  $\mu\text{V}$ . This technology is described on the following page.

# TLC4501/2 Self-Calibrating (Self-Cal™)

## CMOS Op Amp



### Self-Calibration:

- Disconnect and short amp inputs
- Measure offset error with A/D
- Store error measurement
- Apply compensation with D/A

1-89

## TLC4501/2 Self-Calibrating (Self-Cal™) CMOS Op Amp

Texas Instruments has introduced the CMOS operational amplifier TLC4501 and TLC4502 which integrate a new self-calibrating (Self-Cal™) technology. This technology allows a compensation of the input offset voltage down to a value of 40  $\mu\text{V}$  maximum for the TLC4501A. This gives a big improvement in comparison with the standard CMOS op amps, which have typically an input offset voltage of around 1 mV. The picture shows the block diagram of this self-calibrating op amp. After power-up, the differential inputs of the TLC4501/2 are connected to each other, so that the inputs are disconnected from the real input and the differential voltage is forced to zero. This self-calibrating feature requires typically 300 ms. The voltage at the output of the op amp is, during this time, connected to an A/D converter, which converts the input offset voltage of the op amp into a digital format. The input offset cancellation uses a current-mode D/A converter, whose full-scale output allows for an adjustment of approximately  $\pm 5$  mV to the input offset voltage.

The performance of the TLC4501 and TLC4502 in terms of input offset voltage is:

| Op Amp   | TLC4501              | TLC4501A             | TLC4502               | TLC4502A             |
|----------|----------------------|----------------------|-----------------------|----------------------|
| $V_{IO}$ | $\pm 80 \mu\text{V}$ | $\pm 40 \mu\text{V}$ | $\pm 100 \mu\text{V}$ | $\pm 50 \mu\text{V}$ |

**Self-Cal™ Op Amp vs other Techniques**

| Feature         | TLC450x<br>Self-Cal™ | Chopper<br>Stabilized | Precision<br>BiPolar |
|-----------------|----------------------|-----------------------|----------------------|
| Power           | Low                  | Medium                | High                 |
| Ext. Components | No                   | Capacitor             | No                   |
| Laser Trim      | No                   | No                    | Yes \$\$             |
| Bandwidth       | High                 | Limited               | High                 |
| R-R Output      | Yes                  | No                    | No                   |
| # Channels      | Dual                 | Single                | Dual                 |
| Cost            | Low                  | \$ \$                 | \$ \$                |

1-90

**Self-Cal™ Op Amp vs other Techniques**

While chopper op amps and some precision bipolar op amps can achieve lower input offset voltages than the Self-Cal amplifier, the TLC4501/2 offers significant advantages over both:

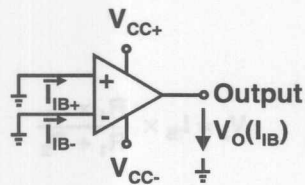
Chopper amplifiers suffer from bandwidths limited by the chopping frequency. They also introduce switching noise onto the signal and the ground plane. The TLC4501 and the TLC4502 have no chopping circuitry. Furthermore, choppers typically require external storage capacitors and are generally expensive.

High precision bipolar op amps lack the high impedance inputs preferred for sensing very small signals from high impedance sensors. High input currents lead to dc errors when large resistance's are used. Furthermore, bipolar op amps tend to consume more power.

The TLC4501/2 CMOS architecture doesn't show these disadvantages. Moreover, the TLC4501/2 require no laser trimming and are therefore less expensive than high precision bipolar amplifiers.

|                        |                         |                        |                        |          |
|------------------------|-------------------------|------------------------|------------------------|----------|
| TLC4502A               | TLC4502                 | TLC4501A               | TLC4501                | Op Amp   |
| $V_{IO} \pm 0.8 \mu V$ | $V_{IO} \pm 0.01 \mu V$ | $V_{IO} \pm 0.5 \mu V$ | $V_{IO} \pm 0.8 \mu V$ | $V_{IO}$ |

# Input Bias Current ( $I_{IB}$ )



$$I_{IB} = \frac{I_{IB+} + I_{IB-}}{2}$$

| Parameter                              | Technology                             |                                      |                                      |
|----------------------------------------|----------------------------------------|--------------------------------------|--------------------------------------|
|                                        | TLE2037I<br>(BIPOLAR)                  | TLE2071<br>(BiFET)                   | TLC2201<br>(CMOS)                    |
| $I_{IB}(\text{typ}, 25^\circ\text{C})$ | 15 nA                                  | 20 pA                                | 1 pA                                 |
| $I_{IB}(\text{max}, 25^\circ\text{C})$ | 90 nA                                  | 175 pA                               |                                      |
| $I_{IB}(\text{max})$                   | 150 nA                                 | 5 nA                                 | 150 pA                               |
| $\frac{\Delta I_{IB}}{\Delta T}$       | Fairly Stable<br>over tempe-<br>rature | Double for<br>every 10°C<br>increase | Double for<br>every 10°C<br>increase |

1-91

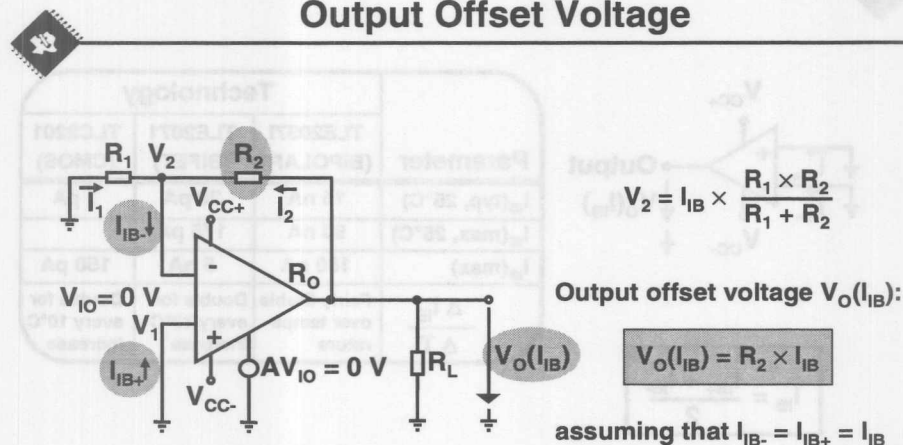
## Input Bias Current

The input bias current  $I_{IB}$  is defined as the average of the currents  $I_{IB+}$  and  $I_{IB-}$  into the two input terminals, as shown in the picture.  $I_{IB+}$  is here the current into the noninverting input and  $I_{IB-}$  is the current into the inverting input. These currents are the bias currents of the input transistors of the differential amplifier.

Bipolar op amps have typically a very high input bias current of several hundred nano-amperes compared to BiFET and CMOS op amps. This is the reason why bipolar op amps are not well suited for high impedance applications. BiFET and CMOS op amps have a very high input impedance and therefore a very low input bias current of typically around 1 pA or even less at a temperature of 25°C. This makes the BiFET and CMOS op amps ideal for high impedance applications. However, the input bias current doubles for every 10°C increase in temperature, which may cause a significant output offset voltage, if the op amp is used in a high temperature environment with a large feedback resistor.

The following page shows the impact of the input bias current on the output offset voltage.

## Output Offset Voltage



Input bias current can cause an output offset voltage.

1-92

### Output Offset Voltage caused by the Input Bias Current

The input bias current of an op amp may cause an output offset voltage at the output, if the input bias current is not compensated. The circuit shows an op amp in the inverting or noninverting configuration. The equation for the output offset voltage  $V_{IOB}$ , which is caused by the input bias current of an op amp in the inverting or noninverting configuration, will be derived. For the calculation of the voltage  $V_{IOB}$ , the input offset voltage  $V_{IO}$  is assumed to be zero. The currents  $I_{IB-}$  and  $I_{IB+}$  are flowing into the inverting and noninverting inputs of the op amp. Since the noninverting input is connected to ground, the voltage  $V_1 = 0$ . The output resistance  $R_O$  of the op amp is very small and can therefore be neglected. Because of that the resistors  $R_1$  and  $R_2$  can be seen in parallel. The voltage  $V_2$  can now be calculated as follows:  $V_2 = \frac{R_1 \times R_2}{R_1 + R_2} \times I_{IB-}$ .

Considering the node at  $V_2$ , it can be written:  $I_1 + I_2 = I_{IB-}$ , or

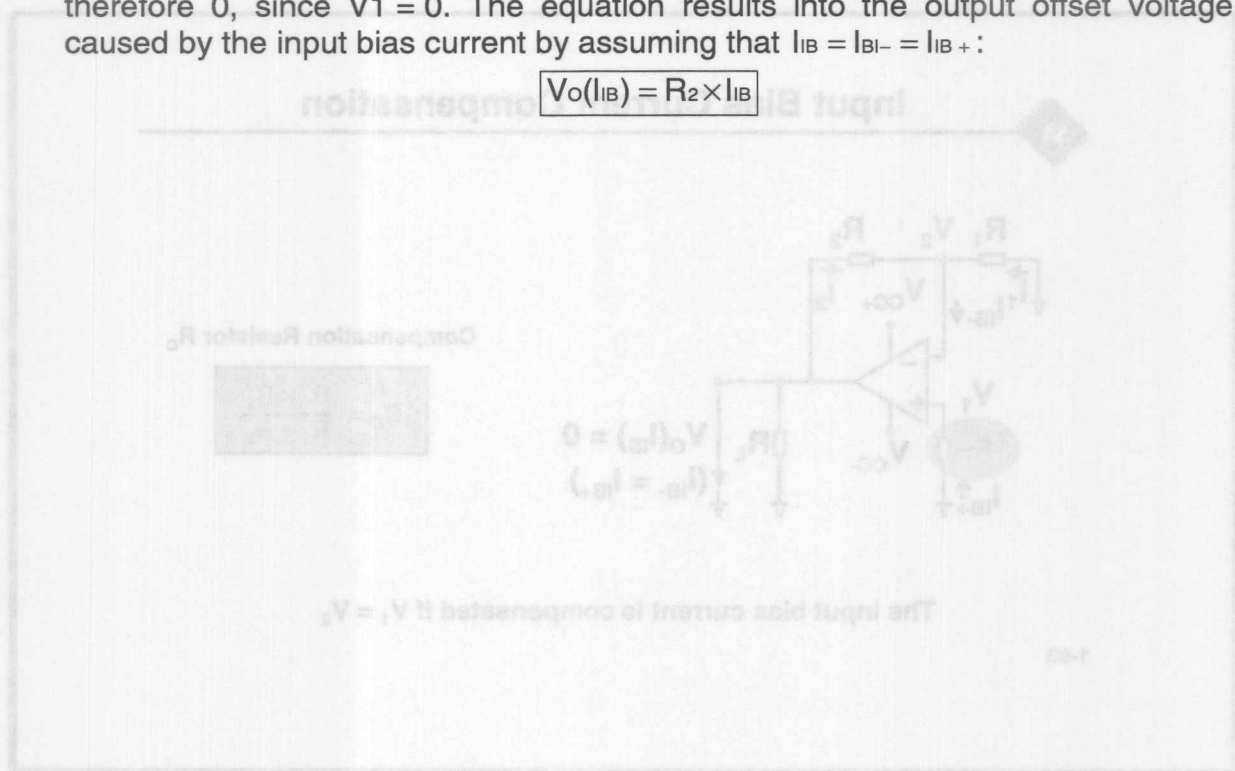
$$\frac{0 - V_2}{R_1} + \frac{V_O(I_{IB}) - V_2}{R_2} = I_{IB-}$$

This results in:

$$V_O(I_{IB}) = V_2 \times \left(1 + \frac{R_1}{R_2}\right) + R_2 \times I_{IB-}$$

The differential voltage between the two input terminals is ideally 0.  $V_2$  is therefore 0, since  $V_1 = 0$ . The equation results into the output offset voltage caused by the input bias current by assuming that  $I_{IB} = I_{BI-} = I_{BI+}$ :

$$V_O(I_{IB}) = R_2 \times I_{IB}$$



## Compensation of the Input Bias Current

The effect of the input bias current can be compensated, if the voltage drop  $V_2$  at the inverting and the voltage drop  $V_1$  at the noninverting input of the op amp are equal. As already described before, the voltage  $V_2$  can be calculated as follows:

$$V_2 = \frac{R_1 \times R_2}{R_1 + R_2} \times I_{B-}$$

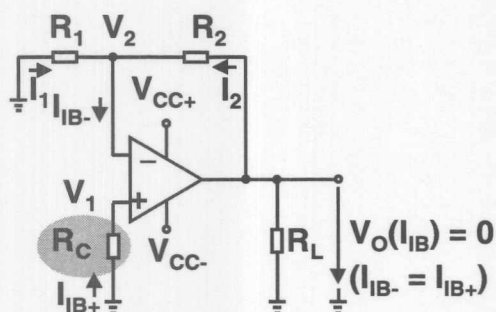
Under the assumption that the input bias current  $I_B$  is equal as well to the bias current flowing into the noninverting input ( $I_{B+}$ ) as to the bias current flowing into the inverting input ( $I_{B-}$ ), the compensation resistor  $R_3$  can be calculated as follows:

$$R_3 = \frac{R_1 \times R_2}{R_1 + R_2}$$

The resulting voltage  $V_1$  is under these conditions equal to the voltage  $V_2$ :

$$V_1 = R_3 \times I_{B+} = \frac{R_1 \times R_2}{R_1 + R_2} \times I_{B+}$$

## Input Bias Current Compensation



Compensation Resistor  $R_C$

$$R_C = \frac{R_1 \times R_2}{R_1 + R_2}$$

The input bias current is compensated if  $V_1 = V_2$

1-93

### Compensation of the Input Bias Current

The effect of the input bias current can be compensated, if the voltage drop  $V_2$  at the inverting and the voltage drop  $V_1$  at the noninverting input of the op amp are equal. As already described before, the voltage  $V_2$  can be calculated as follows:

$$V_2 = \frac{R_1 \times R_2}{R_1 + R_2} \times I_{IB-}$$

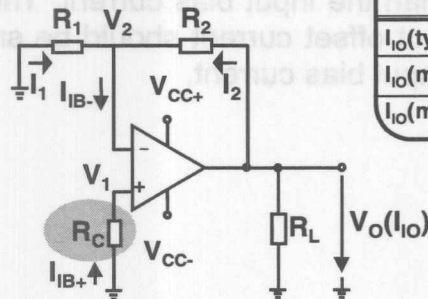
Under the assumption that the input bias current  $I_B$  is equal as well to the bias current flowing into the noninverting input ( $I_{IB+}$ ) as to the bias current flowing into the inverting input ( $I_{IB-}$ ), the compensation resistor  $R_C$  can be calculated as follows:

$$R_C = \frac{R_1 \times R_2}{R_1 + R_2}$$

The resulting voltage  $V_1$  is under these conditions equal to the voltage  $V_2$ .

$$V_1 = R_C \times I_{IB+} = \frac{R_1 \times R_2}{R_1 + R_2} \times I_{IB-}$$

## Input Offset Current ( $I_{IO}$ )



| Parameter                              | Technology           |                    |                   |
|----------------------------------------|----------------------|--------------------|-------------------|
|                                        | TLE2037<br>(BIPOlar) | TLE2071<br>(BiFET) | TLC2201<br>(CMOS) |
| $I_{IO}(\text{typ}, 25^\circ\text{C})$ | 6 nA                 | 15 pA              | 0.5 pA            |
| $I_{IO}(\text{max}, 25^\circ\text{C})$ | 90 nA                | 100 pA             |                   |
| $I_{IO}(\text{max})$                   | 150 nA               | 1.4 nA             | 150 pA            |

Input Offset Current  $I_{IO}$ :

$$I_{IO} = |I_{IB+} - I_{IB-}|$$

Output Offset Voltage caused by  $I_{IO}$ :

$$V_O(I_{IO}) = R_2 \times I_{IO}$$

1-94



## Input Offset Current

We have seen before, that the resistor  $R_C$  is used for compensating the input bias current of the op amp. A complete compensation is only possible, if the individual input bias currents into the terminals of the op amp are equal. In practice, this won't be the case. The maximum difference between the input bias currents  $I_{IB+}$  and  $I_{IB-}$  is called the Input Offset Current, which is defined as follows:

$$I_{IO} = |I_{IB+} - I_{IB-}|$$

The output offset voltage  $V_{O|IO}$  caused by the input offset current can be calculated by applying the superposition theorem. The output offset voltage caused by the voltage  $V_2$  is:  $V_O(I_{IB-}) = -R_2 \times (I_{IB-})$

The output offset voltage caused by the voltage  $V_1$  is:

$$V_O(I_{IB+}) = V_1 \times \left(1 + \frac{R_2}{R_1}\right)$$

With:

$$V_1 = R_C \times (I_{IB+}) = \frac{R_1 \times R_2}{R_1 + R_2} \times (I_{IB+})$$

The equation for  $V_{OIB1}$  results in:

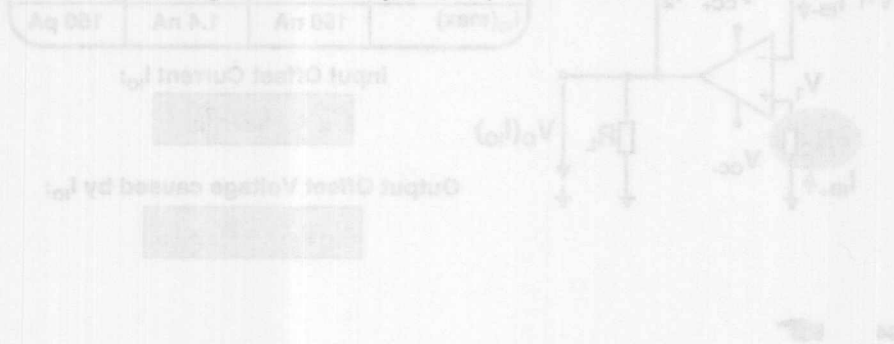
$$V_O(I_{IB+}) = R_2 \times (I_{IB+})$$

The maximum output offset voltage caused by the input offset current can then be calculated by addition of  $V_O(I_{IB+})$  and  $V_O(I_{IB-})$ :

$$V_O(I_{IB+}) + V_O(I_{IB-}) = R_2 \times (I_{IB+}) - R_2 \times (I_{IB-}) = R_2((I_{IB+}) - (I_{IB-}))$$

$$V_O(I_{IO}) = R_2 \times I_{IO}$$

Here again as for the input bias current, the amount of output offset voltage caused by the input offset current is determined by the feedback resistor  $R_2$ . The input offset current is typically smaller than the input bias current. Therefore the output offset which is caused by the input offset current should be smaller than the output offset voltage caused by the input bias current.



## Input Offset Current

We have seen before, that the resistor  $R_1$  is used for compensating the input bias current of the op amp. A complete compensation is only possible, if the individual input bias currents into the terminals of the op amp are equal. In practice, this won't be the case. The maximum difference between the input bias currents  $I_{IB+}$  and  $I_{IB-}$  is called the input offset current, which is defined as follows:

$$I_{IO} = I_{IB+} - I_{IB-}$$

The output offset voltage  $V_O(I_{IO})$  caused by the input offset current can be calculated by applying the superposition theorem. The output offset voltage caused by the voltage  $V_i$  is:

$$V_O(I_{IO}) = -R_2 \times (I_{IB-})$$

The output offset voltage caused by the voltage  $V_i$  is:

$$V_O(I_{IO}) = V_i \times \left(1 + \frac{R_2}{R_1}\right)$$

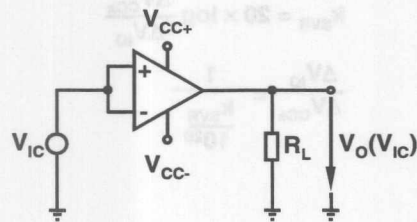
$$V_i = R_1 \times (I_{IB+}) = \frac{R_1 \times R_2}{R_1 + R_2} \times (I_{IB+})$$

With:

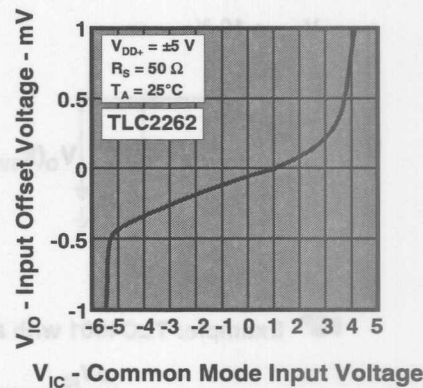
The equation for  $V_O(I_{IO})$  results in:

$$V_O(I_{IO}) = R_2 \times (I_{IB-})$$

## Common-Mode Rejection Ratio (CMRR)



$$\text{CMRR(dB)} = 20 \times \log \frac{\Delta V_{IC}}{\Delta V_{IO}}$$



**Remember:** If CMRR = 80 dB and  $\Delta V_{IC} = 1 \text{ V}$ ,  
then  $\Delta V_{IO} = 100 \mu\text{V}$

1-95

## Common-Mode Rejection Ratio

The common-mode rejection ratio of an ideal op amp is infinite. However in practice, a real op amp produces a small voltage at the output, if a common-mode voltage is applied to the inputs as shown in the picture. The capability to reject the common-mode voltage is called the common-mode rejection ratio, which is defined as follows:

$$\text{CMRR} = 20 \times \log \frac{\Delta V_{IC}}{\Delta V_{IO}}$$

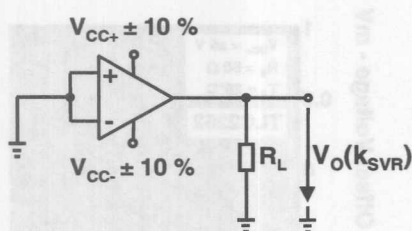
For an op amp with a common-mode rejection ratio of 80 dB, we get:

$$\frac{\Delta V_{IC}}{\Delta V_{IO}} = 10^4$$

This means that a change of the common-mode input voltage of 1V causes a change in the input offset voltage of 100  $\mu\text{V}$ .

Important to mention is that inverting amplifier do not suffer from common-mode rejection ratio effects. This is because the amplifier inputs are permanently at ground for dual supply applications or half the supply voltage in single supply applications. The non-inverting amplifier configuration has a common-mode voltage equal to the input signal.

## Supply Voltage Rejection Ratio ( $k_{SVR}$ )



$$k_{SVR} = 20 \times \log \frac{\Delta V_{CC\pm}}{\Delta V_{IO}}$$

$$\frac{\Delta V_{IO}}{\Delta V_{CC\pm}} = \frac{1}{\frac{k_{SVR}}{10^{20}}}$$

Example: TLC4501 with a typical  $k_{SVR}$  of 100 dB

$$\frac{\Delta V_{IO}}{\Delta V_{CC\pm}} = \frac{1}{\frac{100}{10^{20}}} = 10 \mu V/V$$

1-96

## Supply Voltage Rejection Ratio

The supply voltage rejection ratio  $k_{SVR}$  of an op amp indicates how a change in the supply voltage influences the input offset voltage  $V_{IO}$ . The change in the supply voltage may be caused by a poor supply voltage regulation or a bad supply voltage filtering. The value  $k_{SVR}$  is usually given in dB and we can say:

$$k_{SVR} = 20 \times \log \frac{\Delta V_{CC\pm}}{\Delta V_{IO}}$$

Rearranging this equation, we get:

$$\frac{\Delta V_{IO}}{\Delta V_{CC\pm}} = \frac{1}{\frac{k_{SVR}}{10^{20}}}$$

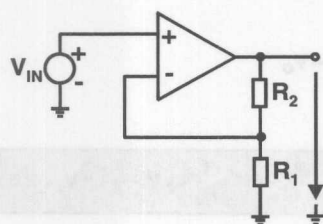
This results as an example for the TLV2262A with a  $k_{SVR}$  of typically 100 dB in:

$$\frac{\Delta V_{IO}}{\Delta V_{DD\pm}} = \frac{1}{\frac{100}{10^{20}}} = 10 \frac{\mu V}{V}$$

In a battery powered system with a supply voltage of  $V_{DD} = 3 V$ , it is possible that the supply voltage may vary up to  $\pm 10\%$ . This results into a supply voltage range from 2.7 V up to 3.3 V. With a supply voltage rejection ratio of 100 dB, the change in the input offset voltage is 3  $\mu V$ . Considering the minimum supply

voltage rejection ratio of 80 dB, we get the maximum change in the input offset voltage of 30  $\mu$ V.

### Total DC Error Non-inverting Amplifier



- Input Bias Current
- Input Offset Current
- Common Mode Rejection Ratio
- Supply Voltage Rejection Ratio

$$V_O = (1 + \frac{R_2}{R_1}) [V_{IN} + V_{IO} + \alpha_{VIO} \times \Delta T + I_{IB} \times (\frac{R_2}{1 + \frac{R_2}{R_1}}) + \frac{V_{IC}}{CMRR} + \frac{\Delta V_{CC}}{K_{SVR}}] \times \frac{1}{1 + \frac{1}{A_{VD}} (1 + \frac{R_2}{R_1})}$$

Noise and input offset voltage long-term drift neglected

1-97



### Total DC Error Noninverting Amplifier

The picture shows an example of a DC error consideration for an op amp which operates as a noninverting amplifier. All the error terms in a DC application which were covered before, are summarised in an equation.

This is the classic differential amplifier and its the simplest way to measure and amplify the potential difference across an op amp is dc-biased will be used because of the single supply operation, and therefore allows a maximum symmetrical voltage swing at the output. The "VIRTUAL GROUND" is the ideal device since it generates exactly the reference voltage  $V_{REF} = 2.5$  V from a voltage in the range of 4 - 40 V. The voltage at the output of the op amp can be calculated as follows:

$$V_O = \frac{R_2}{R_1 + R_2} \times (1 + \frac{R_2}{R_1}) \times V_i - \frac{R_2}{R_2} \times V_i + V_{REF}$$

If the resistors are chosen so

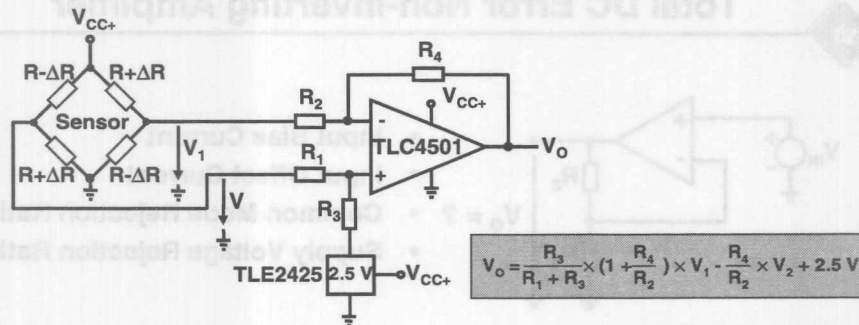
$$\frac{R_2}{R_1} = \frac{R_2}{R_1}$$

an easy practical result is obtained

$$V_O = \frac{R_2}{R_1} \times (V_i - V_i) + V_{REF}$$

## Precision Single Supply Differential

### Amplifier



- Single supply operation
- TLC4501 Self-Cal™ amplifier
- TLE2425 virtual ground reference

1-98

for  $\frac{R_4}{R_2} = \frac{R_3}{R_1}$ :

$$V_o = \frac{R_3}{R_1} \times (V_1 - V_2) + 2.5 \text{ V}$$

## Precision Single Supply Differential Amplifier

This is the classic differential amplifier (subtractor) in a single supply environment and its the simplest way to measure and amplify the potential difference across the bridge diagonal of a Wheatstone Bridge.

This amplifier is a combination of a non-inverting and an inverting amplifier. The op amp is dc-biased with half the supply voltage at the non-inverting input because of the single supply operation, and therefore allows a maximum symmetrical voltage swing at the output. The "TLE2425 Virtual Ground Generator" is the ideal device since it generates exactly the reference voltage  $V_{REF} = 2.5 \text{ V}$  from a voltage in the range of 4 - 40 V. The voltage at the output of the op amp can be calculated as follows:

$$V_o = \frac{R_3}{R_1 + R_3} \times \left(1 + \frac{R_4}{R_2}\right) \times V_1 - \frac{R_4}{R_2} \times V_2 + V_{REF}.$$

If the resistors are chosen so

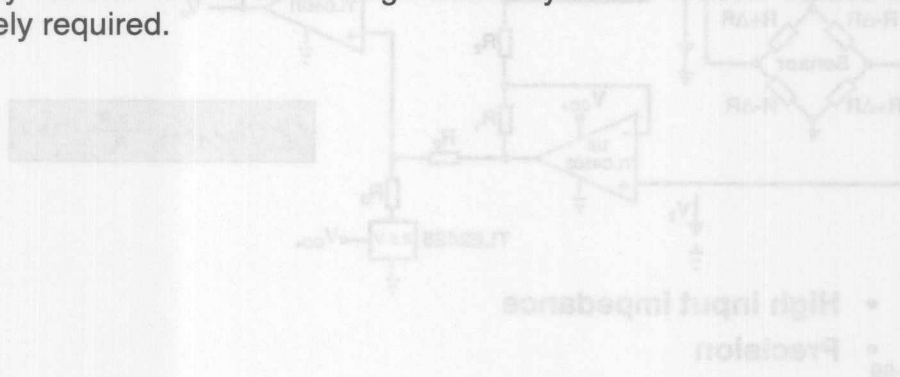
$$\frac{R_4}{R_2} = \frac{R_3}{R_1},$$

an easy practical result is obtained

$$V_o = \frac{R_3}{R_1} \times (V_1 - V_2) + V_{REF},$$

since for an input voltage of  $V_1=V_2$ , the output of the op amp delivers theoretically exactly the middle voltage  $V_O = 2.5 \text{ V}$ .

The disadvantages of this circuit are that its input impedance is unbalanced and the common mode rejection is modified by the source impedances. This circuit is therefore not recommended for high impedance sources. The common mode rejection of the TLC4501 is typically 100 dB. This means that an increase of 1 V in the common mode voltage is similar to a differential voltage between the inputs of  $10 \mu\text{V}$ . More important is that the Common Mode Rejection is also driven by resistor tolerances. A high accuracy in the resistor values is therefore absolutely required.

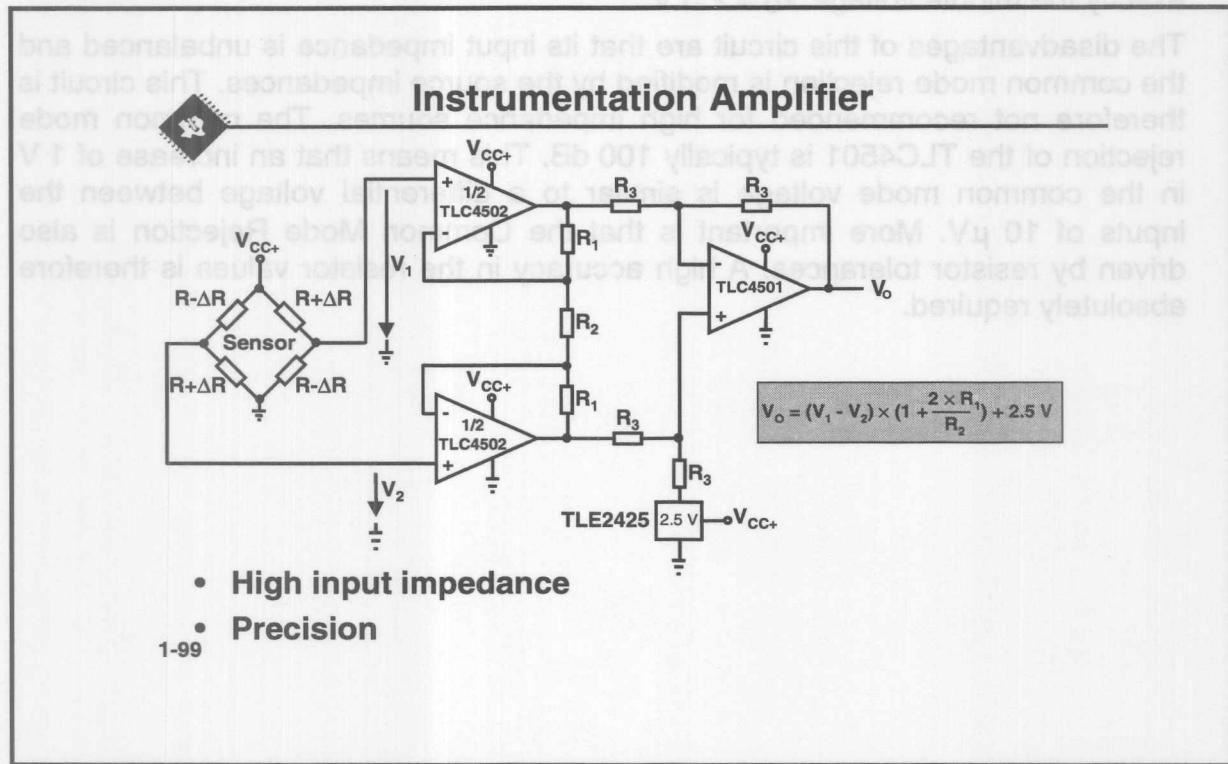


Instrumentation Amplifier

A very high input impedance can be achieved by using an instrumentation amplifier. Such an amplifier consists of three op amps. The differential amplifier discussed before can be found again with a gain of 1, because all resistors are the same. Two further op amps are connected in the front of this differential amplifier to provide now the very high input impedance which is only determined by the op amp input impedance. The source which is connected to the instrumentation amplifier is in this case only loaded by the high input impedance of the CMOS op amp TLC4501 which is typical  $10^{12}$ . The gain is adjusted by the resistor  $R_f$ . The output voltage can be calculated as follows:

$$V_O = (V_2 - V_1) \times \left(1 + \frac{2 \times R_f}{R_1}\right) + V_{ref}$$

Again, also in this circuit it is very important to select the resistor  $R_f$  with a high accuracy relative to each other to achieve high common mode rejection. This can be achieved with a resistor array network for  $R_f$ , where the relative accuracy is very good (value in the region of 10 kΩ). The absolute accuracy of the resistors  $R_1$  is not as important.



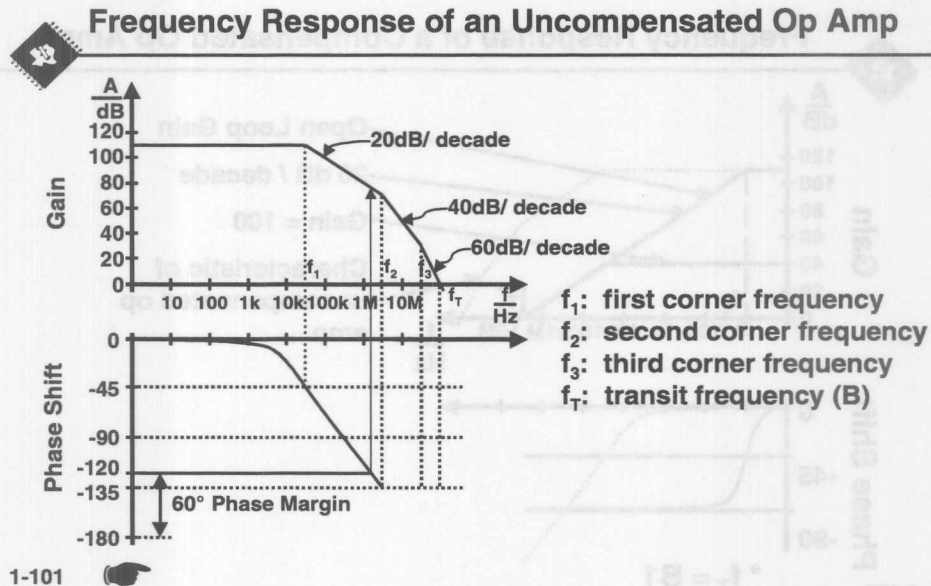
### Instrumentation Amplifier

A very high input impedance can be achieved by using an instrumentation amplifier. Such an amplifier consists of three op amps. The differential amplifier discussed before can be found again with a gain of 1, because all resistors are the same. Two further op amps are connected in the front of this differential amplifier to provide now the very high input impedance which is only determined by the op amp input impedance. The source which is connected to the instrumentation amplifier is in this case only loaded by the high input impedance of the CMOS op amp TLC4501 which is typical  $10^{12}$ . The gain is adjusted by the resistor  $R_2$ . The output voltage can be calculated as follows

$$V_0 = (V_2 - V_1) \times \left(1 + \frac{2 \times R_1}{R_2}\right) + V_{REF}.$$

Again, also in this circuit it is very important to select the resistors  $R_3$  with a high accuracy relative to each other to achieve high common mode rejection. This can be achieved with a resistor array network for  $R_3$ , where the relative accuracy is very good (value in the region of 10 kΩ). The absolute accuracy of the resistors  $R_3$  is not as important.

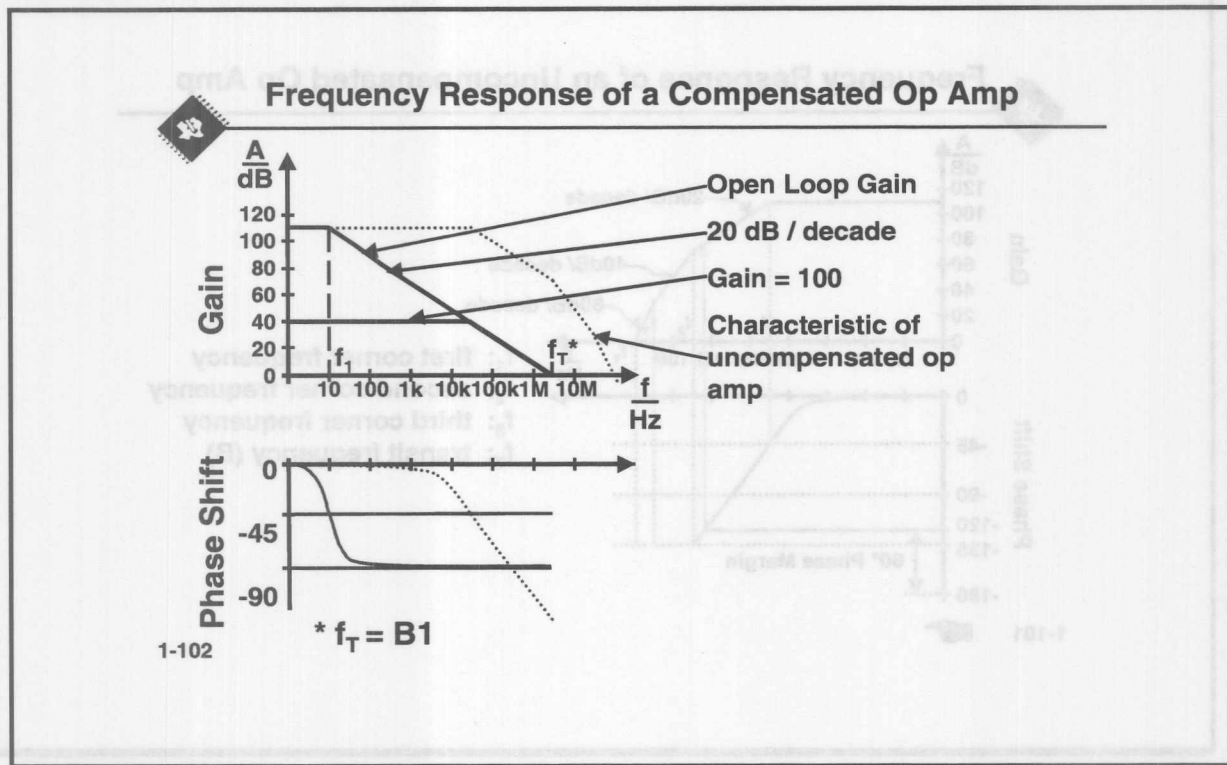
## AC-Considerations of Operational Amplifiers



### Frequency Response of an Uncompensated Op Amp

An operational amplifier behaves, because of internal stages and parasitic capacitances, as a low-pass filter of a higher order. The figure shows the typical frequency response. The differential gain and the phase shift between input and output are a function of the frequency. The gain is constant up to the first break frequency  $f_1$ . At this point the gain has decreased by 3 dB and the phase shift between input and output of the op amp has increased to  $-45^\circ$ . For frequencies above  $f_1$  the amplitude decreases with 20 dB per decade until the second break frequency  $f_2$ . If the frequencies  $f_1$  and  $f_2$  are far enough apart, the phase shift caused by the first low-pass filter is  $-90^\circ$ , the phase shift caused by the second low-pass filter is  $-45^\circ$ , which results into a phase shift of  $-135^\circ$  at frequency  $f_2$ . Beginning from  $f_2$ , the amplitude decreases with 40 dB per decade, till the edge frequency of the third low-pass filter is reached. The phase shift at  $f_3$  between input and output is now  $-180^\circ$ , under the assumption that the frequencies  $f_2$  and  $f_3$  are far enough apart. This is the point where the inverting and the noninverting input of the op amp swap their roles. The feedback which is fed to the inverting input, expected as a negative feedback, has now become positive and may influence the circuitry to oscillate. To avoid oscillation, a phase margin is required. If the gain  $|A_{VD}| > 1$ , the phase margin should be at least  $-60^\circ$ , which means that the phase shift between input and output is not higher than around -

120°. This results for the depicted frequency response into a minimum gain of 75 to 80 dB and a restricted bandwidth.



### Frequency Response of a Compensated Op Amp

An operational amplifier which has to be used universally must have a phase shift between input and output which is less than around 120° while having a closed loop gain greater or equal to 1. This can be achieved if the frequency response of the op amp over the usable frequency range is compensated so that the frequency response is similar to a first order low-pass filter. The undesired low-pass filter, which was discussed before, cannot be avoided and remains at the same frequency. However, the break frequency  $f_1$  can be decreased by adding a compensation capacitor inside the op amp that the gain  $A$  reaches the value 1 before the second low-pass filter causes a phase shift of -180° between input and output. Since the break frequency  $f_1$  has decreased, the available bandwidth is lower compared to a decompensated op amp. This is the reason that some high bandwidth op amps (e.g. the TLE2037) are not compensated. The picture shows an op amp which can be used universally since the phase shift between input and output is 90° at a closed loop gain of 1. It shows also the available bandwidth at a gain of 100 and at open loop gain. It is clear that the available bandwidth decreases with an increasing gain.

# Limited Slew Rate Distortion

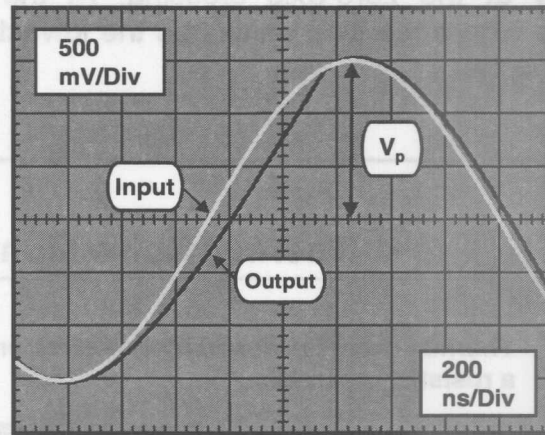
$$SR_{min} = 2 \times \pi \times f \times V_p$$

Example:

SR of 3.45 V/μs

output swing  $V_p$  of 1.5 V

$f_{max} = 366$  kHz



Result with  $f_{in} = 460$  kHz

1-103

## Distortion caused by limited Slew Rate

The basic bandwidth of an operational amplifier is specified as the unity-gain bandwidth. This unity-gain bandwidth is the range of frequencies within which the maximum output voltage swing is above a specified value. However, this bandwidth can only be used for **small signals** which are in the range of mV or μV. If large-signals in the range of **several volts** up to the supply voltage are considered, the slew rate is the determining factor of the maximum signal frequency. The measurement shows the input and output voltages of an op amp which operates as a voltage follower. The input voltage is a sine wave. The equation for the output voltage without distortion is:

$$v(t) = V_p \times \sin \omega t$$

The slope of this sine signal is:  $\frac{dv}{dt} = V_p \times \omega \cos \omega t$

The maximum slope occurs when  $\cos \omega t = 1$ , or at the zero-axis crossing of the sine signal. If the slew rate of the op amp is set to the maximum slope of the signal, the following equation is obtained:

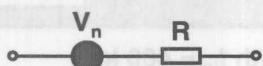
$$SR = \left. \frac{dv}{dt} \right|_{max} = V_p \times \omega$$

This equation gives the minimum required slew rate of the op amp for a desired output magnitude and signal frequency to get an output signal without distortion

in terms of Transient Intermodulation (TIM). The example shows the effect of slow rate, which is too slow. The maximum signal frequency in that example is 366 kHz with a given slew rate of 3.45 V/ $\mu$ s and a signal magnitude of 1.5 V. The measurement shows the result with a signal frequency of 460 kHz. It can be seen that the output of the op amp is not able to follow the input signal, especially at the zero-axis crossing. At the minimum and at the maximum amplitude where the sine wave has the lowest slope, the output is able to follow the input signal.

## Thermal Noise (Johnson Noise)

Thermal noise is caused by free electrons which move randomly in a resistive material.



$$V_n = \sqrt{4 \times k \times T \times \Delta f \times R}$$

where:  $k$  is Boltzmann's Constant ( $1.374 \times 10^{-3}$  J/ $^{\circ}$ K)  
 $T$  is the absolute temperature in degrees Kelvin  
 $\Delta f$  is the bandwidth in Hz  
 $R$  is the resistance in  $\Omega$

### Rule of thumb:

The noise contribution of a 1 k $\Omega$  resistor at 25 $^{\circ}$ C in a 1 Hz bandwidth will generate 4 nV rms noise.

1-104

## Thermal Noise (Johnson Noise)

Thermal Noise is generated when thermal energy causes free electrons to move randomly in a resistive material. Capacitances and inductances don't show this thermal noise except in the thermal noise of the parasitic resistances. The phenomenon of thermal noise was discovered by Schottky in 1928 and measured and evaluated by Johnson in the same year and it is therefore also referred to as Johnson noise. The rms thermal noise across an open-circuit resistor is given by:

$$V_n = \sqrt{4kT\Delta fR}$$

where  $k$  is the Boltzmann's constant,  $R$  the resistance,  $\Delta f$  the bandwidth over which the noise is measured and  $T$  is the absolute temperature in degree Kelvin.

The generated noise voltage up to high frequencies is independent of the frequency. Therefore the thermal noise is also referred to as white noise in

analogy with the spectrum of white light which has also a flat power distribution in the optical frequency range.

Therefore, the power in thermal noise is proportional to the square of  $V_n$ , which is independent of the frequency for a fixed bandwidth. The power between 20 Hz and 20 kHz is the same as the power between 10.020 kHz and 30 kHz.

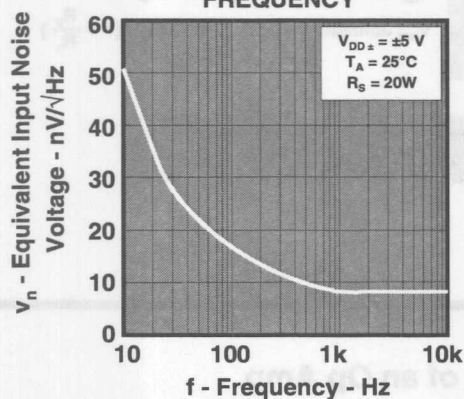
The noise contribution of a 1 k $\Omega$  resistor at 25°C in a 1 Hz bandwidth will generate 4 nV rms noise. With a bandwidth of 1 kHz, the thermal noise increases

to: 
$$4 \text{ nV} \times \frac{\sqrt{1000\text{Hz}}}{\sqrt{\text{Hz}}} = 126 \text{ nV}.$$



## Op Amp Noise (TLC2272)

### EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY



Typ. Noise Parameter @ 25°C  
(TLC2272):

$V_n$  (f = 10 Hz): 50 nV/√Hz

$V_n$  (f = 1 kHz): 9 nV/√Hz

$V_{NPP}$  (f = 0.1 Hz to 1 Hz): 1  $\mu$ V

$V_{NPP}$  (f = 0.1 Hz to 10 Hz): 1.4  $\mu$ V

$I_N$ : 0.6 fA/√Hz

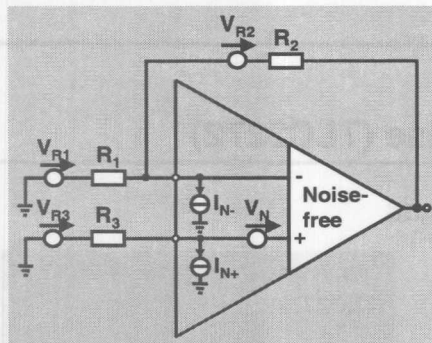
1-105

## Op Amp Noise (TLC2272)

An op amp shows different kinds of noise phenomena. These are the Schottky noise (current noise), thermal noise (voltage noise) and flicker noise. The Schottky noise is associated with the current flowing through a pn junction. Voltage noise is generated both by ohmic resistances in the op amp, and also by the effect of the current noise on the resistors in the op amp circuitry. An example of this is shown on the next page. This noise is for most of the frequency operating area white noise. This means that the noise level up to high frequencies is independent of the frequency and remains at the same amplitude (also referred to as "white noise". For the TLC2272 it can be seen that above 1 kHz the voltage noise stays at around 9 nV/√Hz. However, at lower frequencies in the region of 10 Hz up to some hundred Hz, the noise level is higher. This

increase is caused by the flicker noise, which is only dominant in the low-frequency area and is inversely proportional to the frequency. The flicker noise is therefore referred to as  $1/f$  noise and is also called „pink“ noise. This phenomena is visible in the shown noise diagram for the TLC2272.

## Calculating the Noise at the Output of an Op Amp



Noise of each source individually:

$$V_{N1}: \text{Op amp voltage noise: } V_N \times (1 + \frac{R_2}{R_1})$$

$$V_{N2}: \text{Op amp current noise } (I_{N-}): (I_{N-}) \times R_2$$

$$V_{N3}: \text{Op amp current noise } (I_{N+}): (I_{N+}) \times R_3 \times (1 + \frac{R_2}{R_1})$$

$$V_{N4}: \text{Johnson noise } R_1: \sqrt{4kT\Delta f R_1} \times (-\frac{R_2}{R_1})$$

$$V_{N5}: \text{Johnson noise } R_2: \sqrt{4kT\Delta f R_2}$$

$$V_{N6}: \text{Johnson noise } R_3: \sqrt{4kT\Delta f R_3} \times (1 + \frac{R_2}{R_1})$$

$$V_{NT} = \sqrt{(V_{N1})^2 + (V_{N2})^2 + (V_{N3})^2 + (V_{N4})^2 + (V_{N5})^2 + (V_{N6})^2}$$

1-106

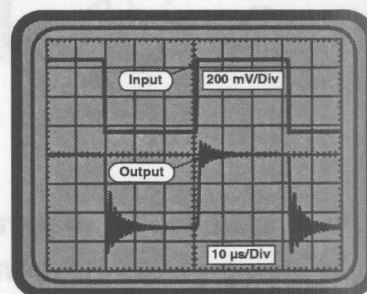
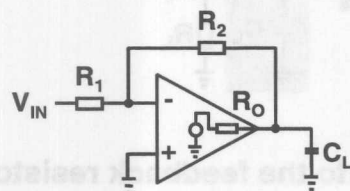
## Calculating the Noise at the Output of an Op Amp

The picture shows an example where the noise at the output of an op amp is calculated. The op amp circuit which is investigated can be considered as an inverting or non-inverting amplifier, but without having a signal source. Six different noise sources have to be taken into account in this example, which generate a noise voltage at the output of the op amp. These are the three op amp noise sources (voltage noise, current noise  $I_{N+}$ ,  $I_{N-}$ ) and the thermal noise of each resistor used. Each noise source has a specific transmission factor to the output of the op amp.

The op amp voltage noise is amplified with the factor  $(1 + R_2/R_1)$ , because this voltage is applied at the non-inverting input of the amplifier. The noise current  $I_{N+}$  flows through the resistor  $R_3$  and generates a voltage  $(I_{N+} \times R_3)$  at the non-inverting input. This voltage is also amplified with the factor  $(1 + R_2/R_1)$ . Therefore the output voltage caused by  $I_{N+}$  is:  $(I_{N+} \times R_3) \times (1 + R_2/R_1)$ . The noise current  $I_{N-}$  generates the voltage  $I_{N-} \times R_2$  which is transmitted with factor 1 to the output of the op amp. The thermal noise caused by  $R_1$  ( $\sqrt{4kT\Delta f R_1}$ ) is amplified with the factor  $-R_2/R_1$  (inverting amplifier). The thermal noise caused by  $R_3$

$(\sqrt{4kT\Delta fR_3})$  is amplified with the factor  $(1 + R_2/R_1)$  (non-inverting amplifier). The thermal noise caused by  $R_2$  ( $\sqrt{4kT\Delta fR_2}$ ) is applied directly at the output of the op amp. It is important to mention here that the resulting noise is not the arithmetic sum of all noise sources. The resulting noise at the output of the op amp is the root of the sum of their squares as shown in the picture above.

## Driving a Capacitive Load



\* Measurement with a TLC272 operating as a voltage-follower with a 220 pF capacitive load.

A capacitive load creates in combination with the output impedance  $R_O$  of the op amp a low-pass filter. A further phase shift in addition to the op amp's phase shift is caused and the phase margin is reduced.

1-107

## Driving a Capacitive Load

Problems in terms of stability are often caused either by bad bypassing or by a capacitive load which the op amp has to drive, whether or not this is desired. Even the trace capacitance of a printed circuit board, which may be in the range of 0.5 to 1 pF/cm may increase the settling times for amplifiers which are designed to handle capacitive loads of around 100 pF. The capacitive load at the output of the op amp creates a low pass filter with the output resistance  $R_O$ . The break frequency depends on  $R_O$  and  $C_L$  and can be calculated as follows:

$$f_c = \frac{1}{2\pi R_O C_L}$$

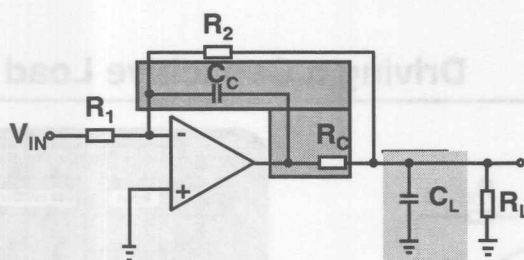
This low-pass filter causes a phase shift in addition to the op amp's phase shift. The phase shift is given by:

$$\varphi = -\arctan \omega R_O C_L$$

The phase margin is therefore reduced and at frequencies where the phase shift of the op amp and the low-pass filter is each  $90^\circ$ , the negative feedback

becomes a positive feedback. This results into oscillation at the output of the op amp which can also be seen in the measurement.

## Lead Compensation of Capacitive Load



The capacitor  $C_c$  in parallel to the feedback resistor causes a phase lead and can therefore compensate for the phase lag caused by the capacitive load  $C_L$ .

1-108

## Lead Compensation of Capacitive Load

A popular technique to reduce the oscillation caused by a capacitive load is the lead compensation of the capacitive load. The phase lag caused by the capacitive load  $C_L$  can be compensated for by a small capacitor  $C_c$  in parallel with the feedback resistor in order to provide a phase lead at the input of the op amp. It is possible to neutralise the phase lag which is caused by  $C_L$ . The required phase lead can be generated with  $C_c$ . The equation for a neutral compensation are:

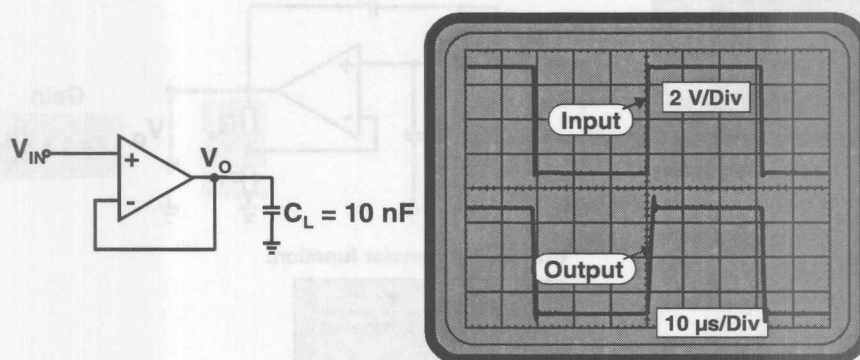
$$R_c = \frac{R_1 \times R_2}{R_1 + R_2} \times R_o$$

and

$$C_c = \left(1 + \frac{R_1 \times R_2}{R_1 + R_2}\right)^2 \times \frac{R_o \times R_2}{R_o + R_2} C_L$$

In most cases a small isolating resistor (30 – 100  $\Omega$ ) between the amplifier feedback and the capacitive load is sufficient in order to reduce the oscillation at the output of the op amp.

# TLE214x - Driving a Capacitive Load of 10000 pF



\* Measurement with a TLE2142 operating as a voltage-follower with a 10 nF capacitive load.

1-109

## TLE214x – Driving a Capacitive Load of 10000 pF

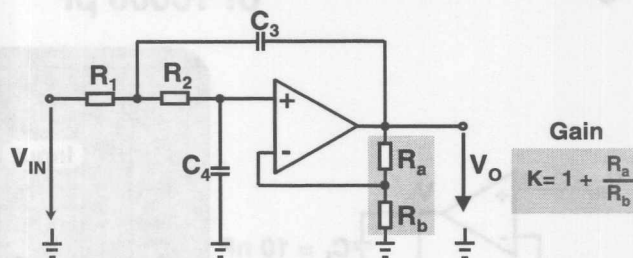
The TLE214x op amp family is especially designed to be able to drive a higher capacitive load. The devices are stable with capacitive loads up to 10 nF, although the 6-MHz bandwidth decreases to 1.8 MHz at this high loading level. Therefore, this family is suitable for direct buffering of longer cables.

## Sallen and Key Lowpass Filter

For  $R_1 = R_2 = R$  and  
 $C_3 = C_4 = C$

$$f_c = \frac{1}{2\pi RC}$$

$f_c$  : corner frequency



Normalized transfer function:

$$H(s) = \frac{K}{s^2 + 2Dsn + 1}$$

$$2D = \frac{1}{Q}$$

Butterworth filter 2nd-order:  $2D = \sqrt{2}$

1-110

## Sallen and Key Lowpass filter

Active filters are built up from op amps with resistive and capacitive components. Sallen and Key circuit technology, as shown in the picture, can be used to implement all types of filters. Active filters have many advantages over R-L-C filters especially at low frequencies where the elimination of large inductors improves filter performance while reducing costs. Other advantages are greater response accuracy and the ability to provide circuit gain. Designing active filters means choosing a filter shape that satisfies the requirements in terms of amplitude, phase and transient response. It is basically only possible to optimise one of these parameters while for the other a compromise has to be found. A Butterworth filter is often the best overall choice because it has the flattest passband and proceeds smoothly from the passband, without ripple, through the cut-off frequency  $f_c$  at  $-3$  dB into the stop band with a decrease in the amplitude of 40 dB/decade. The normalised equation for a 2<sup>nd</sup> order lowpass filter is:

$$H(s) = \frac{K}{s^2 + 2Dsn + 1} = \frac{K}{\left(\frac{s}{\omega_B}\right)^2 + 2D\frac{s}{\omega_B} + 1}, \text{ where } 2D = 1/Q.$$

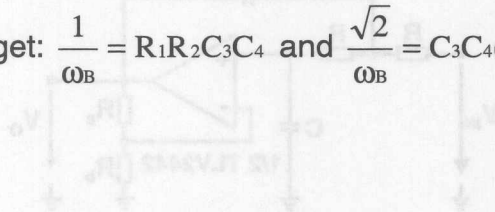
It is possible to select the center frequency, the damping  $D$  and its inverse  $Q$ . Damping, or  $Q$ , sets the peaking or drop of the response near the cutoff frequency. The normalised equation for a Butterworth 2<sup>nd</sup> order filter is:

$$H(s) = \frac{K}{\left(\frac{s}{\omega_B}\right)^2 + \sqrt{2} \frac{s}{\omega_B} + 1} \quad (1)$$

The transfer function of the Sallen and Key circuit results in:

$$H(s) = \frac{K}{s^2 R_1 R_2 C_3 C_4 + s[C_4(R_1 + R_2) + R_1 C_3(1 - K)] + 1} \quad (2)$$

From (1) and (2) we get:  $\frac{1}{\omega_B} = R_1 R_2 C_3 C_4$  and  $\frac{\sqrt{2}}{\omega_B} = C_3 C_4(R_1 + R_2) + R_1 C_3(1 - K)$ .



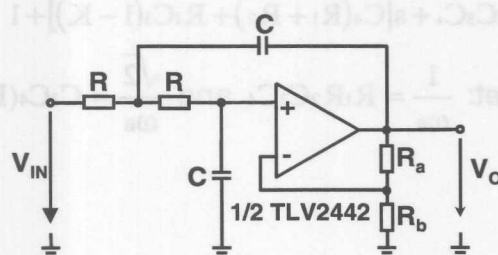
Filter for Telecom Application - Butterworth 2<sup>nd</sup> Order -

An example for a lowpass filter with a cutoff frequency of 4 kHz (telecom application) is considered with the condition:  $R_1 = R_2 = R$ ,  $C_3 = C_4 = C$ ,  $\omega_B = \omega_C$  and  $R = 5k\Omega$ . The cutoff frequency is simply:  $\omega_c = \frac{1}{2\pi RC}$ . The gain K results into:  $\sqrt{2}RC = 3RC - KRC$ , therefore  $K = 1.588$ . With  $R = 5k\Omega$ , C can now be calculated:  $C = \frac{1}{R\omega_c} = 7.95 nF$ .

The op amp used in active filters has to be chosen carefully, because the gain-bandwidth and the slew rate will limit the accuracy and highest frequency of operation for a given filter realization. As the filter gain-cut-off frequency product approaches the op amp gain-bandwidth product the accuracy of the cut-off frequency will be reduced. To limit these effects the closed loop gain of the op amp gain should be at least 10 times higher than the cut-off frequency of the filter. The slew rate limits the large signal bandwidth and can affect stability with increasing amplitude because of the additional phase shift introduced when the signal is close to the slew limit. The TLV2442 fits this application ideally.

### Filter for Telecom Application

#### - Butterworth 2nd Order -



$f_c = 4 \text{ kHz}$   
 $K = 1.586$   
 $R = 5 \text{ k}\Omega$   
 $C = 7.96 \text{ nF}$

1-111

#### Filter for Telecom Application - Butterworth 2<sup>nd</sup> Order -

An example for a lowpass filter with a cutoff frequency of 4 kHz (telecom application) is considered with the condition:  $R_1=R_2=R$ ,  $C_3=C_4=C$ ,  $\omega_B=\omega_C$  and

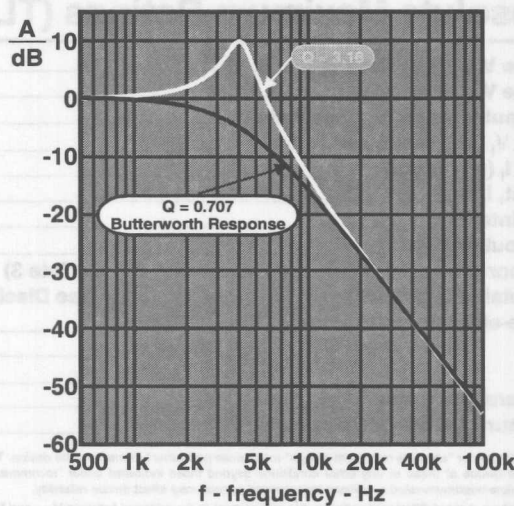
$R=5\text{k}\Omega$ . The cutoff frequency is simply:  $f_c = \frac{1}{2\pi RC}$ . The gain K results into:

$\sqrt{2}RC = 3RC - KRC$ , therefore  $K=1.586$ . With  $R=5\text{k}\Omega$ , C can now be calculated:

$$C = \frac{1}{R\omega_c} = 7.96 \text{ nF}.$$

The op amp used in active filters has to be chosen carefully, because the gain-bandwidth and the slew rate will limit the accuracy and highest frequency of operation for a given filter realisation. As the filter gain-cut-off frequency product approaches the op amp gain bandwidth product the accuracy of the cut-off frequency will be reduced. To limit these effects the closed loop gain of the op amp gain should be at least 10 times higher than the cut-off frequency of the filter. The slew rate limits the large signal bandwidth and can affect stability with increasing amplitude because of the additional phase shift introduced when the signal is close to the slew limit. The TLV2442 fits this application ideally

# Responses of 2nd-order filter



1-112

## Responses of 2<sup>nd</sup> order Filter

The graph shows the frequency response of the circuit which was shown on the page before. Two characteristics, the Butterworth frequency response ( $Q = 0.707$ ) and the a  $Q$  of 3.16, were measured. The Butterworth characteristic shows it has the flattest passband and proceeds smoothly from the passband, without ripple, through the cut-off frequency  $f_c$  at  $-3$  dB into the stop band with a decrease in the amplitude of 40 dB/decade.

## Device Ratings


**Absolute Maximum Ratings (TLC227x)**

|                                                                    |                                |
|--------------------------------------------------------------------|--------------------------------|
| Supply voltage $V_{DD+}$ (see Note 1)                              | 8 V                            |
| Supply voltage $V_{DD-}$ (see Note 1)                              | -8 V                           |
| Differential input voltage, $V_{ID}$ (see Note 2)                  | $\pm 16$ V                     |
| Input voltage, $V_I$ (any input, see Note 1)                       | $V_{DD-} - 0.3$ V to $V_{DD+}$ |
| Input current, $I_I$ (any input)                                   | $\pm 5$ mA                     |
| Output current, $I_O$                                              | $\pm 50$ mA                    |
| Total current into $V_{DD+}$                                       | $\pm 50$ mA                    |
| Total current out of $V_{DD-}$                                     | $\pm 50$ mA                    |
| Duration of short-circuit current at (or below) 25° C (see Note 3) | unlimited                      |
| Continuous total dissipation                                       | See Dissipation Rating Table   |
| Operating free-air temperature range, $T_A$ :                      |                                |
| C suffix                                                           | 0° C to 70° C                  |
| I suffix                                                           | -40° C to 85° C                |
| M suffix                                                           | -55° C to 125° C               |
| Storage temperature range                                          | -65° C to 150° C               |
| Lead temperature 1.6 mm from case for 10 seconds                   | 260° C                         |

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operation conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may effect device reliability.

Notes: 1. All voltage values, except differential voltages, are with respect to the midpoint between  $V_{DD+}$  and  $V_{DD-}$ .  
 2. Differential voltages are at  $IN+$  with respect to  $IN-$ . Excessive current will flow if input is brought below  $V_{DD-} - 0.3$  V.  
 3. The output may be shorted to either supply. Temperature and/or supply voltage must be limited to ensure that the maximum dissipation rating is not exceeded.

1-114

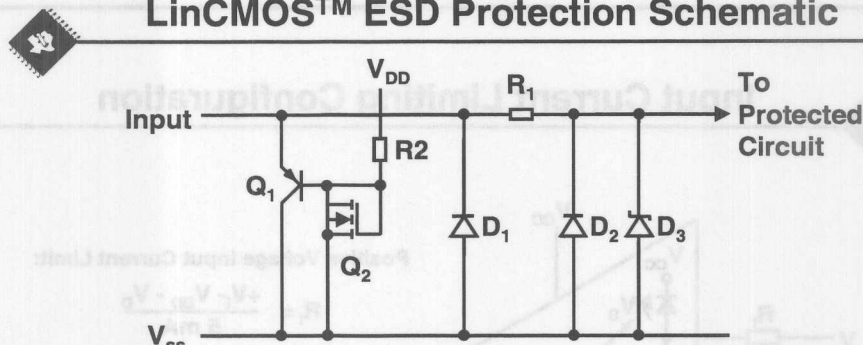
**Absolute Maximum Ratings (TLC227x)**

The absolute maximum ratings are the limit values for a specific device; if these are exceeded, permanent damage to the device may be caused. The picture above shows the Absolute Maximum Ratings as an example for the Advanced LinCMOS™ operational amplifier TLC2272.

CMOS devices are limited in their supply voltage and will not operate with supply voltages greater than 16 V. This can be seen in the example with the TLC2272 which has a maximum supply voltage  $V_{DD+}$  of 8 V and  $V_{DD-}$  of -8 V with respect to the midpoint between  $V_{DD+}$  and  $V_{DD-}$ .

An important value which often causes problems, is the input voltage of an op amp. For most of the devices, the input voltage shall not exceed the supply voltages. With the TLC2272 the input voltage must not be more than 0.3V more negative than  $V_{DD-}$  and not higher than  $V_{DD+}$ . This has to be considered especially when the supply voltage of the op amp is turned off and an input voltage is still applied. If this hasn't been taken into account, an excessive current will flow! Such excessive current can be avoided if the input current is limited by using an external current limiting resistor.

### LinCMOS™ ESD Protection Schematic



All input and output pins on LinCMOS™ and Advance LinCMOS™ have an ESD protection to withstand:

- 2000 V discharged from a 100 pF capacitor through a 1500  $\Omega$  resistor (**Human Body Model**)
- 200 V discharged from a 100 pF capacitor with no current limiting resistor (**Charged Device Model**)

1-115

### Input Protection Circuit Operation

Texas Instruments patented protection circuitry allows for both positive- and negative-going ESD transients. These transients are characterised by extremely fast rise times and usually low energies, and can occur both if the device has all pins open and if it is installed in a circuit.

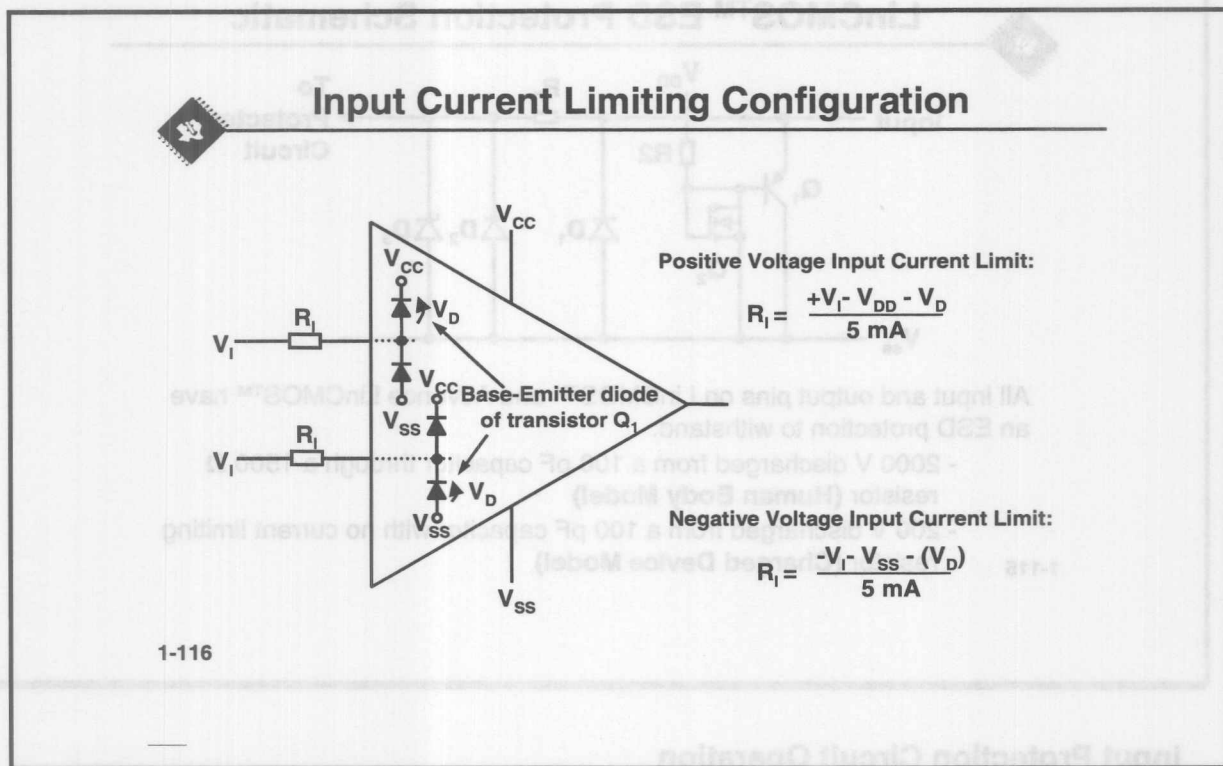
#### Positive ESD transients

Initial positively charged energy is shunted through  $Q_1$  to  $V_{SS}$ .  $Q_1$  will turn on when the voltage at the input rises above the voltage on the  $V_{DD}$  pin by a value equal to the  $V_{BE}$  of  $Q_1$ . Additional energy is dissipated in  $R_2$  when  $Q_1$   $h_{FE}$  limits and saturates. The base current now increases with input current. This current through  $R_2$  will force the voltage at the gate of  $Q_2$ , which is a n-channel enhancement MOS transistor, to exceed its threshold voltage ( $V_T \sim 22$  to  $26$  V) and turn on. The input current through  $Q_1$  is now shunted through  $Q_2$  to  $V_{SS}$ . If the voltage on the input pin continues to rise, the breakdown voltage of the Zener diode  $D_3$  is exceeded and all remaining energy is dissipated in  $R_1$  and  $D_3$ . The breakdown voltage of  $D_3$  is designed to be 24 to 27 V, which is well below the gate oxide voltage of the circuit to be protected.

#### Negative ESD transients

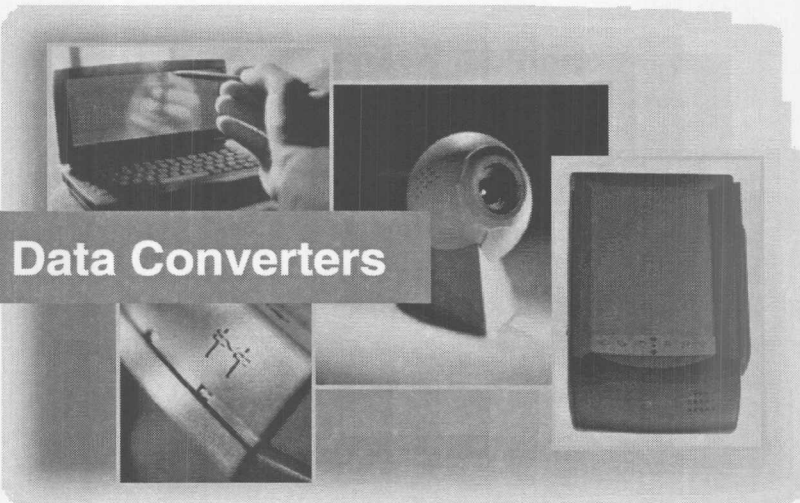
The negatively charged ESD transients will be shunted directly through  $D_1$ . Additional energy will be dissipated in  $R_1$  and  $D_2$  as  $D_2$  becomes forward biased.

The voltage seen by the protected circuit is -0.3 V to -1.0 V (the forward voltage of  $D_1$  and  $D_2$ ).



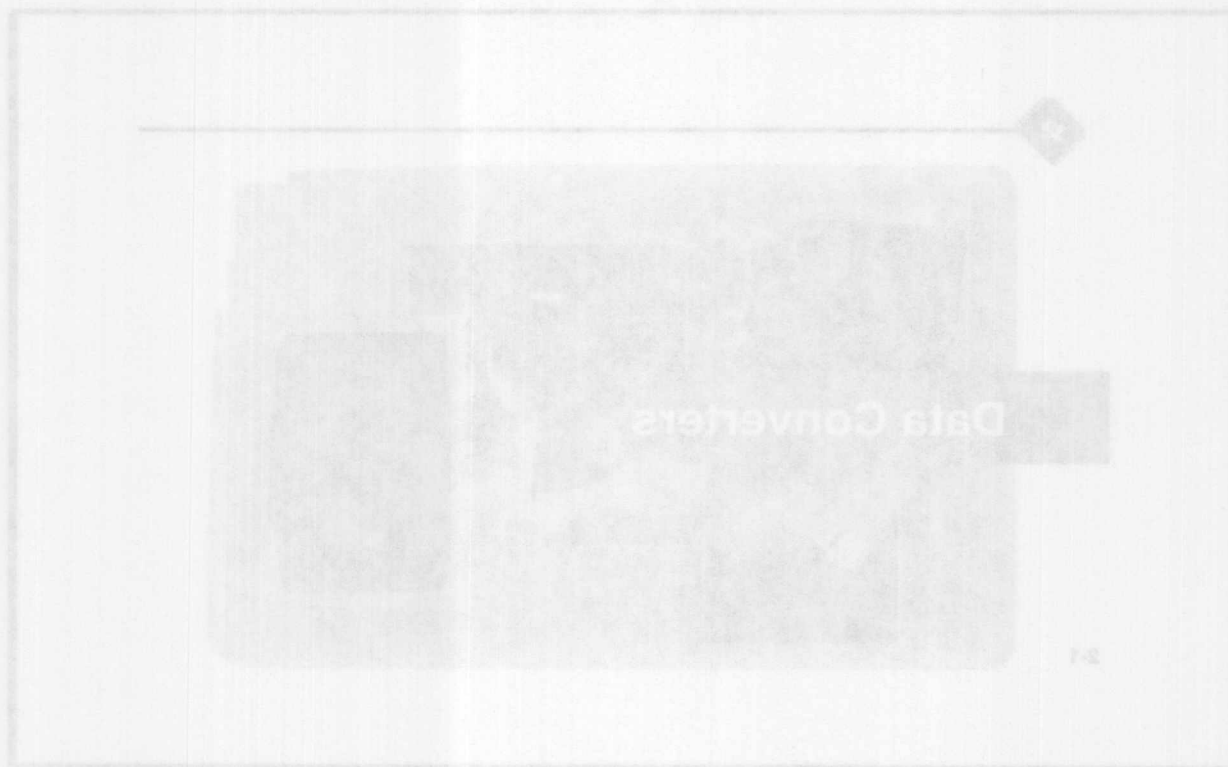
### Input Current Limiting Configuration

LinCMOS™ operational amplifiers are being used in circuit environments that have input voltages which may exceed the recommended common-mode input voltage range. This, as an example, may be caused by using Rail-to-Rail operational amplifiers where output swing reaches the positive or negative supply voltage. The input voltages can exceed  $V_{ICR}$  and not damage the device only if the inputs are current limited. The picture above shows the equivalent protection by using a clamping diode to  $V_{CC}$  and to  $V_{SS}$ . The clamping diode in this case to  $V_{CC}$  is provided by the base-emitter-diode of transistor  $Q_1$  of the protection circuit as discussed before. The recommended current limit shown on most product data sheets is  $\pm 5 \text{ mA}$ .



## **Data Converters**

2-1



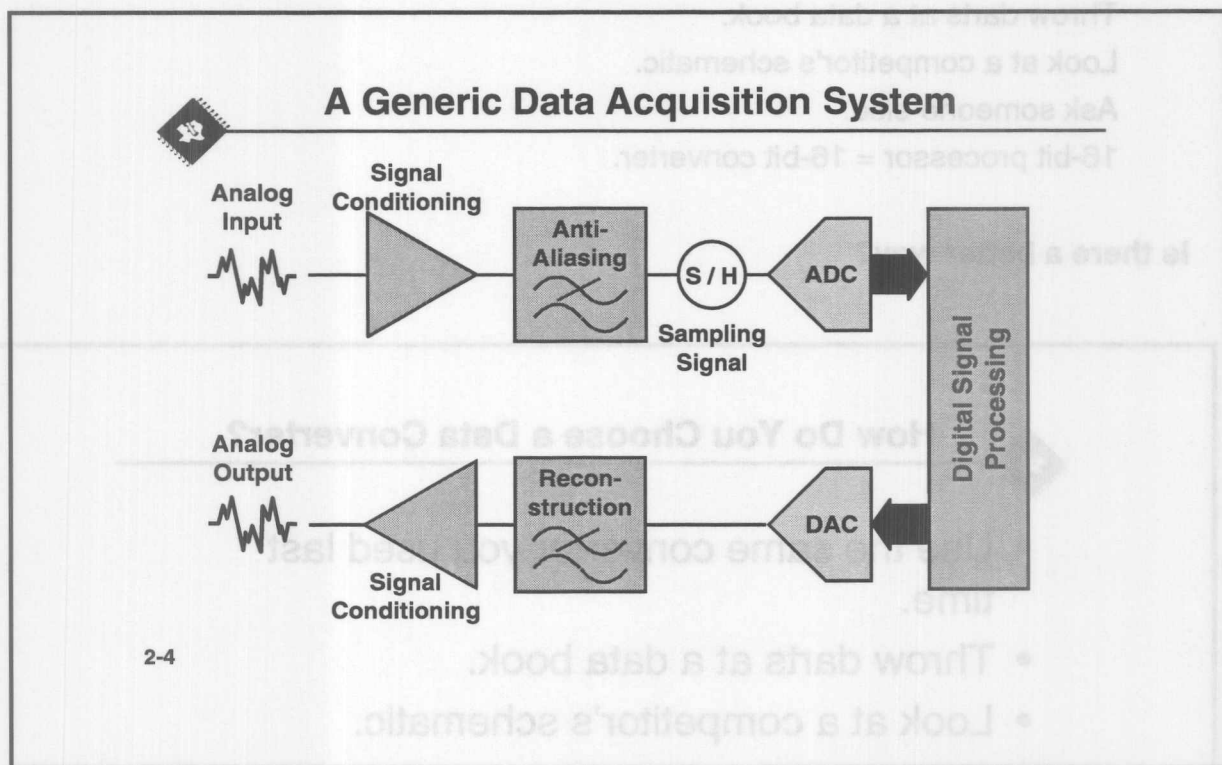
## Table of Contents

|                                                |           |
|------------------------------------------------|-----------|
| <b>Data Converter Overview</b>                 | <b>5</b>  |
| What Is A Data Acquisition System? .....       | 5         |
| Sampling Theory Overview .....                 | 8         |
| <b>DC Specifications</b>                       | <b>16</b> |
| <b>Dynamic (AC) Specifications</b>             | <b>22</b> |
| <b>A/D Converter Architectures</b>             | <b>28</b> |
| Analog to Digital Conversion Techniques .....  | 28        |
| Flash/Pipeline Converters .....                | 41        |
| Sigma-Delta Conversion Technology .....        | 53        |
| <b>D/A Converters</b>                          | <b>59</b> |
| Resistor String DACs .....                     | 59        |
| Current Steering DAC .....                     | 60        |
| Multiplying DACs .....                         | 61        |
| Programmable Gain Amplifier .....              | 63        |
| Precision Programmable Window Comparator ..... | 64        |
| Low Power DAC Families .....                   | 65        |
| <b>Analog Interface Circuits for DSP</b>       | <b>67</b> |
| Analog Interface for DSP .....                 | 67        |
| Audio Converters .....                         | 76        |
| <b>Data Converter Application Reports</b>      | <b>83</b> |

## Table of Contents

|    |                                          |
|----|------------------------------------------|
| 5  | Data Converter Overview                  |
| 8  | What is a Data Acquisition System?       |
| 8  | Sampling Theory Overview                 |
| 10 | DC Specifications                        |
| 22 | Dynamic (AC) Specifications              |
| 28 | ADC Converter Architectures              |
| 28 | Analog to Digital Conversion Techniques  |
| 41 | Flash/Pipeline Converters                |
| 63 | Sigma-Delta Conversion Technology        |
| 69 | D/A Converters                           |
| 69 | Resistor String DACs                     |
| 69 | Current Steering DAC                     |
| 69 | Multiplying DACs                         |
| 69 | Programmable Gain Amplifier              |
| 69 | Precision Programmable Window Comparator |
| 69 | Low Power DAC Families                   |
| 69 | Analog Interface Circuits for DSP        |
| 69 | Analog Interface for DSP                 |
| 78 | Audio Converters                         |
| 83 | Data Converter Application Reports       |

## Data Converter Overview



### What Is A Data Acquisition System?

For a computer or other digital equipment to process analog signals, these signals must first be converted from the analog domain to the digital domain. This process is called quantization. Quantization may be defined as the conversion of an input function, which may have values in a continuous range to an output that has only discrete values.

Data conversion uses the quantization process for transforming analog electrical signals into digital information for storage, display, processing, data transmission, or control. A data conversion system performs this task and comprises sensors, transducers, signal conditioning, anti-aliasing filters, sample-and-hold circuits, analog multiplexers and analog-to-digital converters (ADCs). Recovery of a digital signal into analog form is sometimes required. Digital-to-analog converters (DACs) and filters perform this function. The output amplifier provides the necessary drive the application requires.

How do you Choose a Data Converter?

Use the same converter you used last time.

Throw darts at a data book.

Look at a competitor's schematic.

Ask someone else.

16-bit processor = 16-bit converter.

**Is there a better way?**

### How Do You Choose a Data Converter?

- Use the same converter you used last time.
- Throw darts at a data book.
- Look at a competitor's schematic.
- Ask someone else.
- 16-bit processor = 16-bit converter

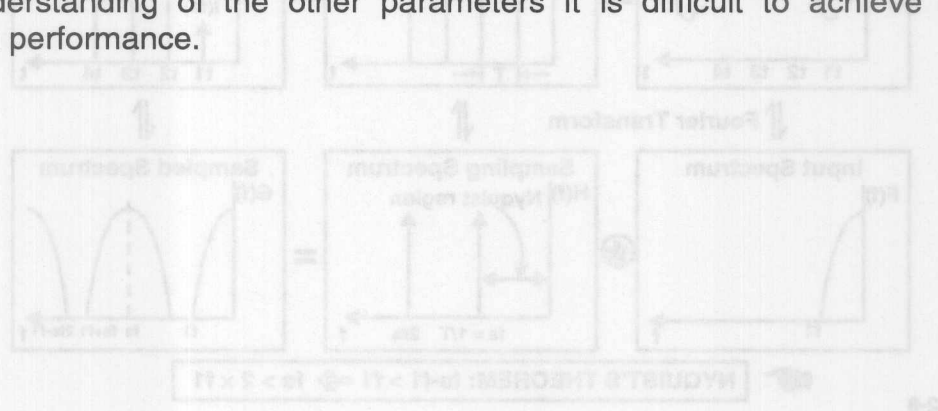
**Is there a better way?**

2-5

Many methods seem to be used in selecting data converters. Some of the methods described above would seem less than optimum. The objective should be to select the right converter for the application. Selecting the right converter be cost effective and provide the performance needed to implement the system solution.

Selecting the right converter begins with the system definition. A description overall system performance and a description of the signal to be converted are the first steps. The signal bandwidth will determine the converter speed. Signal information content will help to determine converter resolution. The system processor interface will determine the converter data interface. This results in an initial specification for a data converter. The converter requirements can be further defined by a more detailed evaluation of system requirements.

The next part of this section describes the basics of sampling theory and sources of error. The next parts describe DC and AC performance of converters. An understanding of the sources of error, AC and DC performance are necessary in order to refine the initial data converter requirements of speed and resolution. Often converters are selected on speed and resolution alone, however without an understanding of the other parameters it is difficult to achieve optimum system performance.



## Sampling Theory Overview

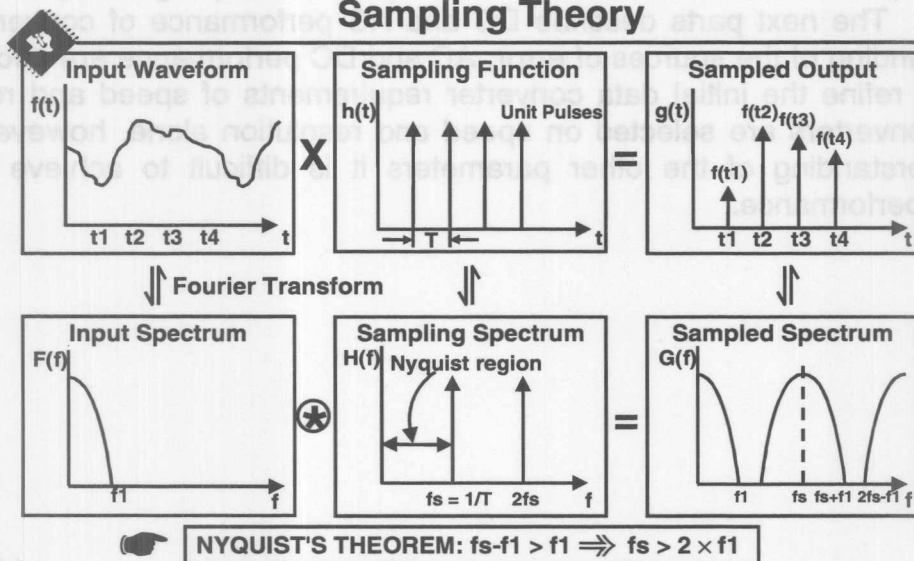
In order to produce a discrete digital representation of a continuously varying analog signal, it is necessary to take samples of the signal at regular intervals and convert them from analog into digital form. In an ideal situation the sampling function is a train of impulses, each of which is infinitesimally narrow and has unit area. The frequency of these pulses is the sampling rate ( $f_s$ ). The input signal can also be idealized by considering it to be truly band limited, containing no components in its spectrum above a certain frequency.

The ideal sampling condition, represented in both the frequency and time domains, is shown in the figure above. The effect of sampling in the time domain is to produce amplitude modulated train of impulses representing the value of the input signal at the instant of sampling. In the frequency domain the spectrum of the pulse train is a series of discrete frequencies at multiples of the sampling rate. Sampling convolves the spectrum of the input signal with that of the pulse train to produce the combined spectrum shown, with sidebands around each discrete frequency produced by the amplitude modulation. In effect some of the higher frequencies are "folded back" so that they produce interference at lower ones. This interference causes distortion, which is called aliasing. Aliases cannot be removed by subsequent processing.

If we assume that the input signal is band limited to a frequency  $f$  and is sampled at frequency  $f_s$  it is clear from the figure that the overlap (and hence aliasing) will not occur if

$$f_s > 2 \times f$$

## Sampling Theory



2-8

## Sampling Theory Overview

In order to produce a discrete digital representation of a continuously varying analog signal, it is necessary to take samples of the signal at regular intervals and convert them from analog into digital form. In an ideal situation the sampling function is a train of impulses, each of which is infinitesimally narrow and has unit area. The frequency of these pulses is the sampling rate ( $f_s$ ). The input signal can also be idealized by considering it to be truly band limited, containing no components in its spectrum above a certain frequency.

The ideal sampling condition, represented in both the frequency and time domains, is shown in the figure above. The effect of sampling in the time domain is to produce amplitude modulated train of impulses representing the value of the input signal at the instant of sampling. In the frequency domain the spectrum of the pulse train is a series of discrete frequencies at multiples of the sampling rate. Sampling convolves the spectrum of the input signal with that of the pulse train to produce the combined spectrum shown, with sidebands around each discrete frequency produced by the amplitude modulation. In effect some of the higher frequencies are "folded back" so that they produce interference at lower ones. This interference causes distortion, which is called aliasing. Aliases cannot be removed by subsequent processing.

If we assume that the input signal is band limited to a frequency  $f_1$  and is sampled at frequency  $f_s$  it is clear from the figure that the overlap (and hence aliasing) will not occur if

$$f_1 < f_s - f_1$$

This could also be expressed by:  $2f_1 < f_s$

Therefore, if sampling is done at a frequency at least twice as great as the maximum frequency of the input signal, no aliasing will occur and all the signal information can be extracted. This is Nyquist's Sampling Theorem, which provides a basic criterion for the selection of the sampling rate required by the converter to process an input signal of a given bandwidth.

In real sampling, however, the width of each sample is finite and this gives rise to a modulation error of  $(\sin x) / x$ . This is explained later.

Real world signals are generally not band limited. To avoid errors due to aliasing an anti-aliasing filter is normally used. This filter band limits the signal and minimizes any errors due to aliasing. Anti-aliasing filters can be either external or internal to the data converter.

When designing a system it is necessary to know the input signal characteristics in order to select a sampling rate and filters, if necessary, for minimum conversion errors.

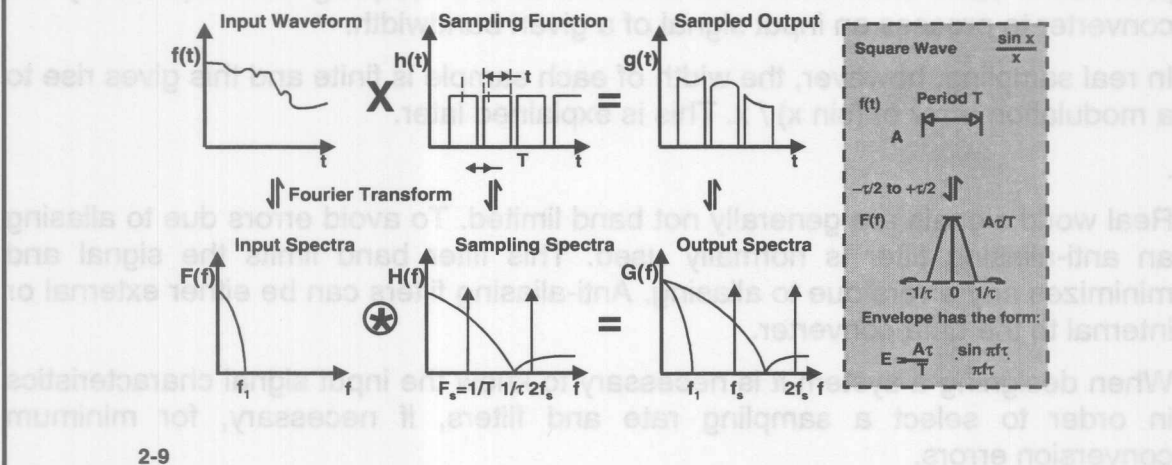
Real Sampling Analog to Digital Conversion

Sampling analog input signals with a unit impulse is an ideal case, which can only be approximated in practice. As shown in the above figure, a real sampling pulse will have a finite width  $\tau$ , but this should still be much shorter than the sampling interval  $T$ . The effect of a sampling pulse  $\tau$  of finite width is to multiply the input signal by a  $(\sin x)/x$  function in the frequency domain, as shown above, and attenuate the higher frequencies. The narrower the sampling pulse  $\tau$  the lower this attenuation will be.

For practical sample and hold (S/H) devices and analog to digital converters that contain an S/H function the aperture over which the incoming signal is sampled gives the effective sampling pulse width. This aperture is the transition time from sample to hold and the value held is the average input over this transition. In this situation the sampling pulse width is the uncertainty or jitter in the sampling instant caused by noise on the digital hold signal within the device. For analog to digital converters, usually of older design, that does not include a S/H function the aperture or sampling pulse width is equal to the conversion time.



## Real Sampling - Analog to Digital Conversion



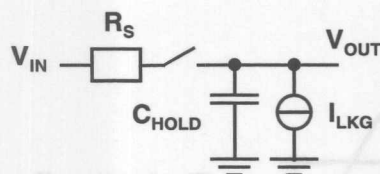
2-9

### Real Sampling Analog to Digital Conversion

Sampling analog input signals with a unit impulse is an ideal case, which can only be approximated in practice. As shown in the above figure, a real sampling pulse will have a finite width  $\tau$ , but this should still be much shorter than the sampling interval  $T$ . The effect of a sampling pulse  $\tau$  of finite width is to multiply the input signal by a  $(\sin x)/x$  function in the frequency domain, as shown above, and attenuate the higher frequencies. The narrower the sampling pulse  $\tau$  the lower this attenuation will be.

For practical sample and hold (S/H) devices and analog to digital converters that contain an S/H function the aperture over which the incoming signal is sampled gives the effective sampling pulse width. This aperture is the transition time from sample to hold and the value held is the average input over this transition. In this situation the sampling pulse width is the uncertainty or jitter in the sampling instant caused by noise on the digital hold signal within the device. For analog to digital converters, usually of older design, that does not include a S/H function the aperture or sampling pulse width is equal to the conversion time.

## Sample and Hold Considerations

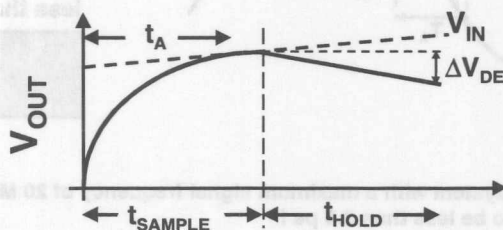


Full Scale Input Acquisition Time:

$$t_A = R_S * C_{HOLD} * \ln(2^n)$$

Drift Error:

$$\Delta V_{DE} = t_{HOLD} * I_{LKG} / C_{HOLD}$$



2-10

## Sample and Hold Considerations

### Acquisition Time

During the sampling phase, period  $t_{SAMPLE}$ , of a sample and hold circuit's operation it acquires and tracks the input signal to within a specified error band.

The Acquisition time,  $t_A$ , required depends on the impedance driving the sample and hold and the capacitor value within the sample and hold. The worst case value for the acquisition time when the input voltage goes from a minimum input to a maximum input, that is the input range of the ADC that the sample and hold is driving.

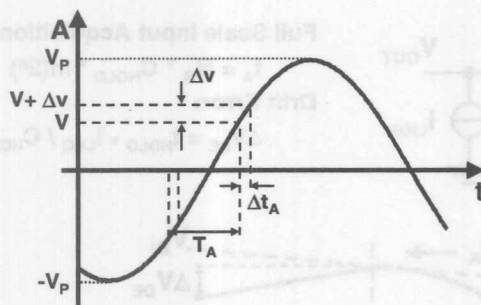
### Voltage Drift

Once the signal has been held, its output will start to droop due to the leakage of the capacitor, open circuit leakage of the analogue switch and impedance of the following stage.

Assuming a constant leakage current of  $I_{LKG}$  over the hold period the held signal will have dropped by:

$$V_{Droop} = t_{HOLD} * I_{LKG} / C_{HOLD}$$

## Aperture-Jitter (Sampling Uncertainty)



The Aperture Error is less than 1 LSB, if:

$$\Delta t_A < \frac{1}{2^n \times \pi \times f_{\max}}$$

In a 12-bit system with a maximum signal frequency of 20 MHz, the Aperture-Jitter has to be less than 3.8 ps !

2-11

## Aperture Jitter (Sampling Uncertainty)

A parameter, which may decrease the SNR of the system, is caused by the sampling uncertainty, or the Aperture-Jitter. If the aperture time varies by the time  $\Delta t_A$ , an error is caused which is equal to the change  $\Delta v$  in the voltage. This results into a degradation of the SNR of an ADC. To calculate the maximum time  $\Delta t_A$  which results into an error less than 1 LSB, a sine wave with the maximum frequency  $f_{\max}$  as an input signal is considered. This can be expressed as:

$$v(t) = V_P \times \sin \omega t.$$

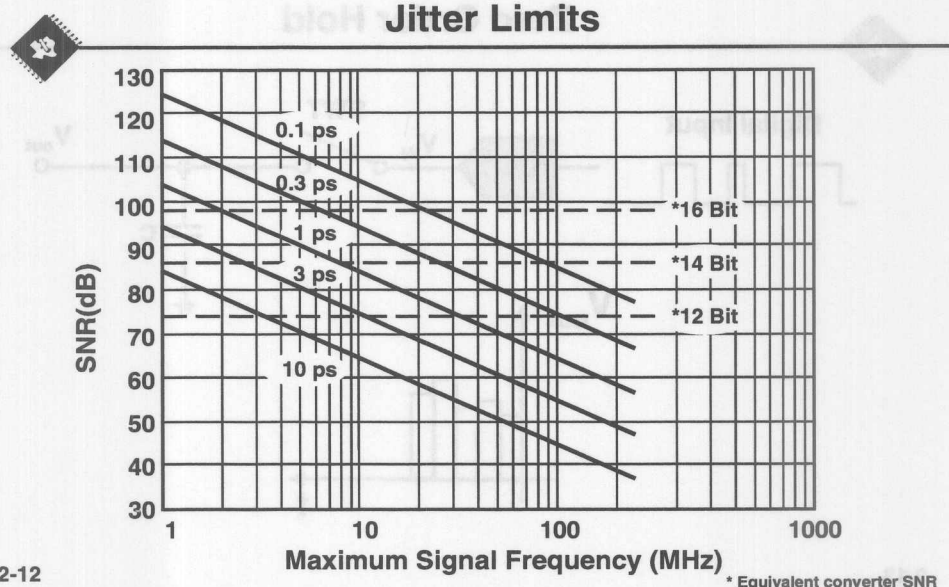
The slope of the sine signal is:

$$\frac{dv}{dt} = V_P \times \omega \times \cos \omega t.$$

The maximum slope occurs when  $\cos \omega t = 1$ , or at the zero-crossing point. This results in:  $\Delta t_A = \frac{\Delta v}{V_P \times \omega}$ . In order to limit the error in the change of the voltage to

less than 1 LSB (1 LSB can be expressed as  $\frac{2V_P}{2^n}$ ),  $\Delta t_A$  results in:

$$\Delta t_A < \frac{1}{(2^n) \times \pi \times f_{\max}}$$



2-12

### Jitter Limits

The degradation of the SNR, caused by the phase jitter, is a function of the frequency and the maximum phase jitter  $t_j$ . As described before, the slew rate of a sine wave can be expressed by:

$$\frac{dv}{dt} = V_P \times \omega \times \cos \omega t,$$

and the maximum slew rate of a sine wave is at the zero-crossing point.

$$\left. \frac{dv}{dt} \right|_{\max} = V_P \times \omega.$$

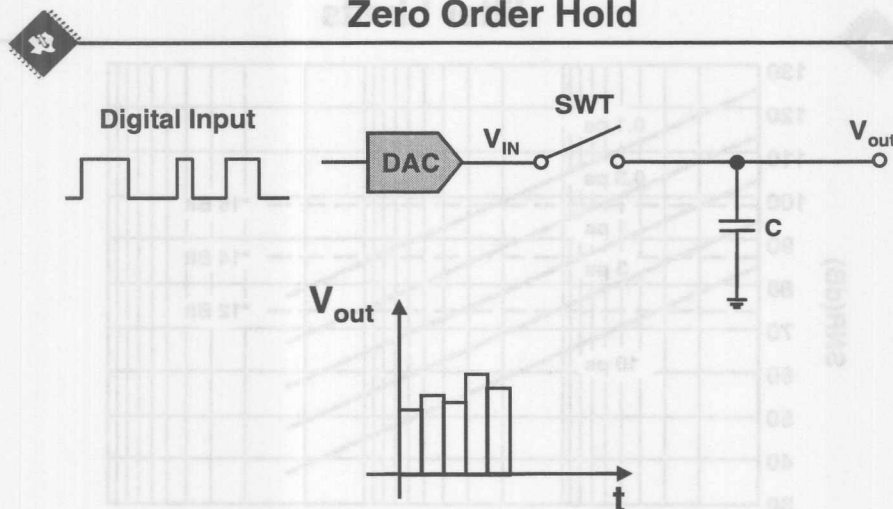
The rms value is then  $\frac{dv}{dt}_{\text{RMS}} = \frac{V_P \times \omega}{\sqrt{2}}$ , therefore  $\Delta V_{\text{rms}} = dv_{\text{rms}} \times dt$  (with

$dt = t_j$ ). The SNR is given by:  $\text{SNR} = \frac{V_P}{\sqrt{2} \Delta V_{\text{rms}}}$ , expressed in dB:

$$\text{SNR}_{(\text{dB})} = 20 \times \log \frac{1}{2 \times \pi \times f \times t_j}$$

For instance, with a jitter of 3 ps and with a maximum signal frequency of 10 MHz, the SNR is about 74 dB.

## Zero Order Hold



2-13

## Zero Order Hold

A switch and a capacitor can represent the simplest form of a zero order hold. The switch is closed for a short time and places a coded voltage on the hold capacitor and repeats the process for every switch closure.

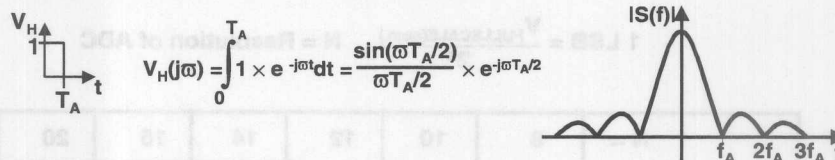
The sample and hold function produces the output voltage envelope shown in the insert as more samples are taken.

Most DAC architectures replicate this sample and hold function to produce the envelope waveform and reduce transients associated with code changes (glitches). The output voltage of the DAC is  $\sin x/x$  weighted, which is shown on the next page.

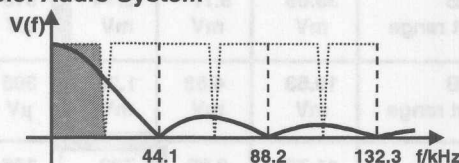
## DAC Sampling Effects

### - sin x / x Modulation -

'Zero Order Hold' and its transfer function



Example: Audio System



2-14

## DAC Sampling Effects - sinx/x Modulation

The concept of an impulse is a useful one to simplify the analysis of sampling. However, it is a theoretical idea, which can be approached but never fully reached in practice. Instead of the ideal very short output pulse, the sample and hold stage produces at the output a pulse with a length which in some cases is up to about the sampling frequency. D/A converters are a good example for this, where the analog output is maintained over the period where the next analog voltage is reproduced. The result of sampling with a finite pulse shows that the original signal is weighted with a  $(\sin(x))/x$  function, where  $x$  in this case is  $\pi f/f_s$ .

$$x = \omega \times \frac{T_A}{2} = 2 \times \pi \times f \times \frac{T_A}{2} = \pi \times f \times \frac{1}{f_s} = \pi \times \frac{f}{f_s}$$

This effect is also known as  $(\sin(x))/x$  distortion. The error resulting from this can be controlled with a filter which compensates for the  $(\sin(x))/x$  distortion. This can be implemented as a digital filter, in a DSP, or using conventional analog techniques. The  $(\sin(x))/x$  is much worse on DACs than on ADCs. Therefore, a correction is performed many times in D/A converters.

# DC Specifications

## How Large is an LSB ?

$$1 \text{ LSB} = \frac{V_{\text{FULLSCALE(nom.)}}}{2^N} \quad N = \text{Resolution of ADC}$$

| N =                        | 8           | 10         | 12         | 14        | 16         | 20         |
|----------------------------|-------------|------------|------------|-----------|------------|------------|
| 1 LSB<br>± 5 V input range | 39.06<br>mV | 9.77<br>mV | 2.44<br>mV | 610<br>μV | 153<br>μV  | 9.53<br>μV |
| 1 LSB<br>+ 5 V input range | 19.53<br>mV | 4.88<br>mV | 1.22<br>mV | 305<br>μV | 76.3<br>μV | 4.77<br>μV |
| 1 LSB<br>+ 3 V input range | 11.72<br>mV | 2.93<br>mV | 732<br>μV  | 183<br>μV | 45.8<br>μV | 2.86<br>μV |

2-16

## How Large is a LSB ?

A code of an ADC represents a specific voltage magnitude, which is given by:

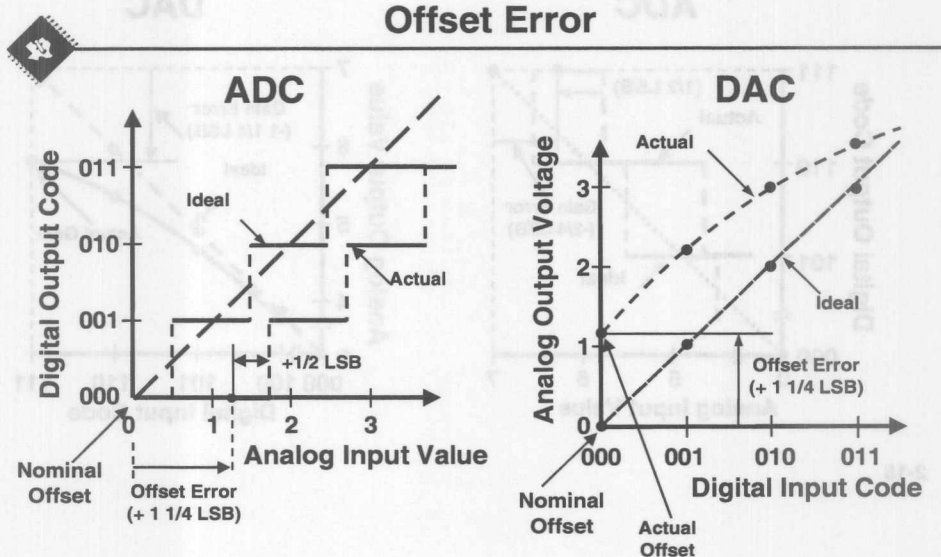
$$1 \text{ LSB} = \frac{V_{\text{FS(nom.)}}}{2^N},$$

Where N is the resolution of the ADC. The figure shows the magnitude of a LSB for different resolutions and different analog input voltage ranges. It's obvious that the LSB is getting very small if the ADC provides a high resolution or the analog input voltage range is small. The figure shows LSB values smaller than 1 mV. Therefore, it is a challenge to keep the error (offset, drift, noise), which is caused by the signal conditioning stage below an LSB of the ADC.

Practical Full-Scale Range (VFS) is the total range of analog values that correspond to the ideal transfer line.

$$1 \text{ LSB} = \frac{V_{\text{FS}}}{2^N - 1},$$

Nominal Full-Scale Range (VFS(nom)) is the total range in analog values that can be coded with uniform accuracy by the total number of steps with this number rounded to the next higher power of 2.



2-17

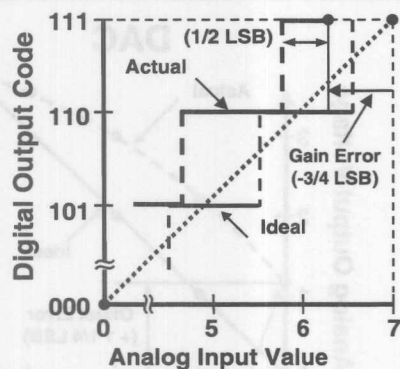
### Offset Error

The offset error is defined as the difference between the nominal and actual offset points. For an A/D converter, the offset point is the mid step value when the digital output is zero and for a DAC it is the output value when the digital input is zero. This error affects all codes by the same amount and can usually be compensated by a trimming process. If trimming is not possible, this error is referred to as the zero-scale error.

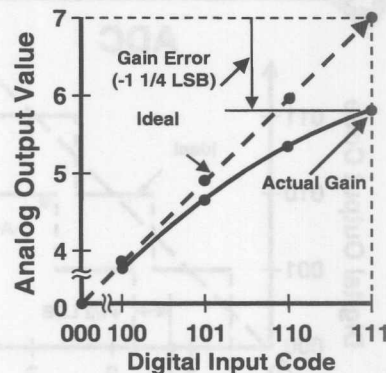
## Gain Error



### ADC



### DAC



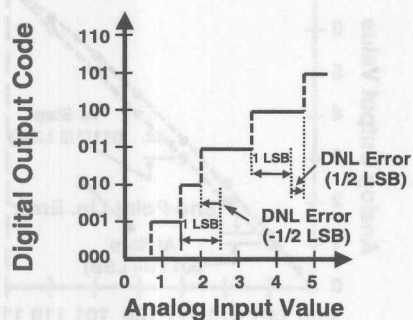
2-18

## Gain Error

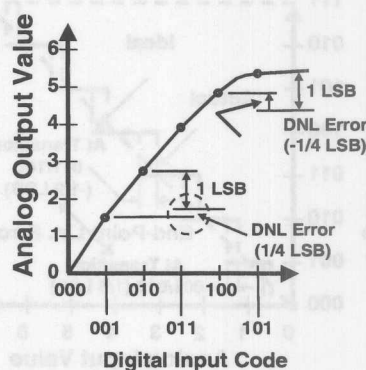
The gain error as shown in the picture is defined as the difference between the nominal and actual gain points on the transfer function after the offset error has been corrected to zero. For an ADC, the gain point is the midstep value when the digital output is full scale, and for a DAC it is the step value when the digital input is full scale. This error represents a difference in the slope of the actual and ideal transfer functions and as such corresponds to the same percentage error in each step. This error can also usually be adjusted to zero by trimming.

## Differential Nonlinearity (DNL) Error

### ADC



### DAC

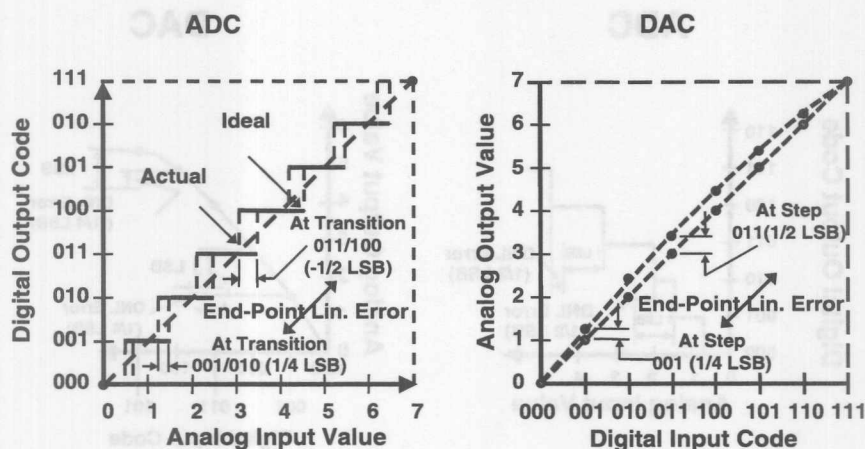


2-19

## Differential Nonlinearity (DNL) Error

The differential nonlinearity error shown in the figure above (sometimes seen as simply differential linearity) is the difference between an actual step width (for an ADC) or step height (for a DAC) and the ideal value of 1 LSB. Therefore if the step width or height is exactly 1 LSB, then the differential nonlinearity error is zero. If the DNL exceeds 1 LSB, there is a possibility that the converter can become nonmonotonic. This means that the magnitude of the output gets smaller for an increase in the magnitude of the input. In an ADC there is also a possibility that there can be missing codes i.e., one or more of the possible  $2^n$  binary codes are never output.

## Integral Nonlinearity (INL) Error



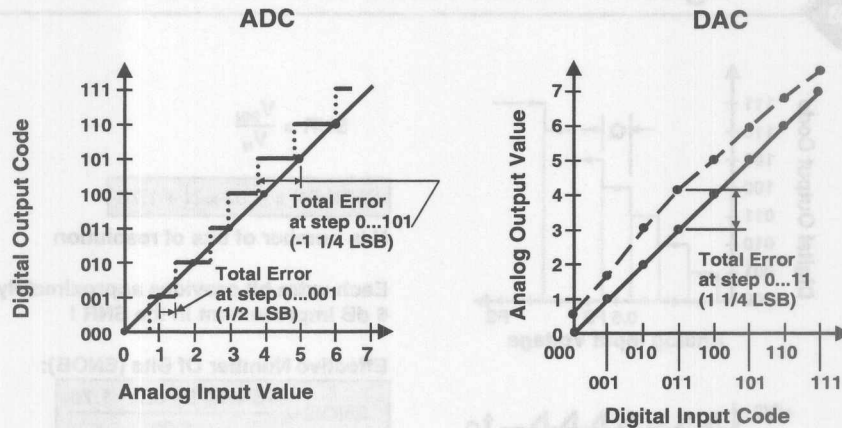
2-20

### Integral Nonlinearity (INL) Error

The integral nonlinearity error is shown in the figure above. It is sometimes seen as simply deviation of the values on the actual transfer function from a straight line. This straight line can be either a best straight line which is drawn so as to minimize these deviations or it can be a line drawn between the end points of the transfer function once the gain and offset errors have been nullified. The second method is called end-point linearity and is the usual definition adopted since it can be verified more directly.

For an ADC the deviations are measured at the transitions from one step to the next, and for the DAC they are measured at each step. The name integral nonlinearity derives from the fact that the summation of the differential nonlinearities from the bottom up to a particular step, determines the value of the integral nonlinearity at that step.

## Total Unadjusted Error



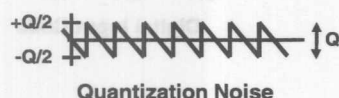
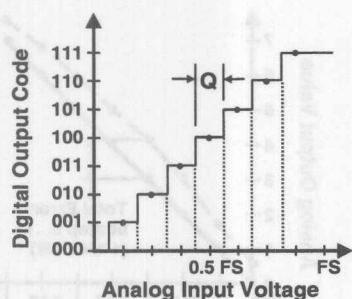
2-21

### Absolute Accuracy (Total) Error

The absolute accuracy or total error of an ADC as shown in the picture is the maximum value of the difference between analog value and the ideal midstep value. It includes offset, gain, and integral linearity errors and also the quantization error in the case of an ADC.

# Dynamic (AC) Specifications

## Signal to Noise Ratio of Data Converter



$$SNR = \frac{V_{SIN}}{V_N}$$

$$SNR(dB) = 6.02 \times N + 1.76$$

N is number of bits of resolution

Each extra bit provides approximately 6 dB improvement in the SNR !

Effective Number Of Bits (ENOB):

$$ENOB = \frac{(SNR + D)(dB) - 1.76}{6.02}$$

2-23

## Signal to Noise Ratio of Data Converter

The Signal to Noise Ratio (SNR also often referred to as S/R) is a very important parameter for an A/D converter. The SNR is the ratio of the rms (root mean square) value of the input signal to the rms value of the quantization noise. The input signal is typically a sine wave with a maximum amplitude  $V_{peak}$ . The rms value can be calculated as follows:

$$V_{SIN(RMS)} = \frac{V_{PEAK}}{\sqrt{2}} = \frac{V_{FSR}}{2 \times \sqrt{2}}$$

The quantization noise voltage, which is also shown in the picture, is similar to a sawtooth voltage waveform. The rms value of a sawtooth waveform is:  $V_N = \frac{V_P}{\sqrt{3}}$ ,

where  $V_P$  is  $Q/2$ . This results into  $V_N = \frac{Q}{2 \times \sqrt{3}} = \frac{Q}{\sqrt{12}} = \frac{V_{FSR}}{2^n \sqrt{12}}$ . Therefore, the SNR can be derived.

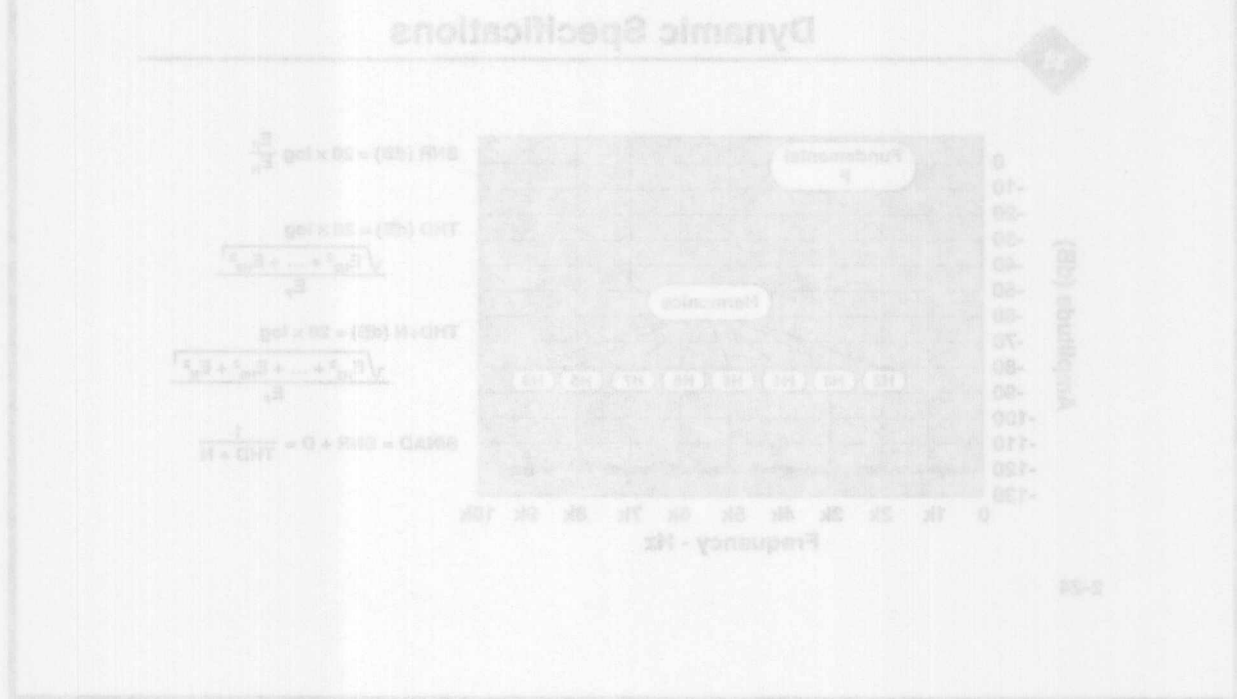
$$SNR = \frac{V_{FSR}}{2\sqrt{2}} \times \frac{2^n \sqrt{12}}{V_{FSR}} = 2^n \sqrt{1.5}.$$

$$SNR(dB) = 20 \times \log 2^n + 20 \times \log \sqrt{1.5} = n \times 20 \times \log 2 + 20 \times \log \sqrt{1.5}$$

This can be written as:

$$SNR(dB) = 6.02 \times n + 1.76 \quad (1)$$

The theoretical SNR of a 12-Bit ADC is approximately 74 dB.



## Dynamic Specifications

### SNR

For a full-scale sine wave input, the theoretical SNR for an N bit converter is given by:  $SNR = 6.02N + 1.76$  dB as already derived before. The normal way of measuring the SNR for a converter is to digitize a full-scale sine wave and then perform an FFT on the output. The rms power of the fundamental is then compared to the noise floor by inserting a notch filter at the input frequency and the harmonics so that the output is purely due to the effects of noise. The ratio of the two is taken to give a direct measurement of the SNR.

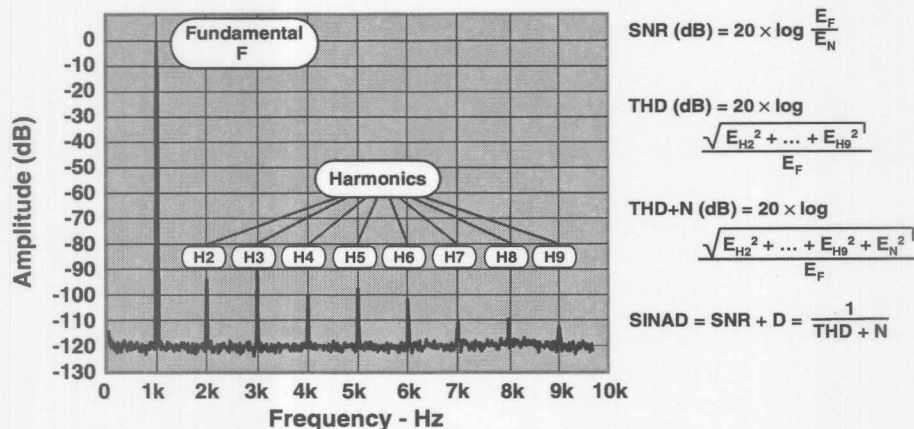
### THD

As in SNR testing, the normal way of measuring the distortion for a converter is to digitize a full-scale sine wave input and then perform an FFT on the output. The rms power of the fundamental is then compared to the sum of the harmonics by inserting a notch filter at the input frequency and the harmonics so that the output is purely due to the effects of harmonics. The ratio of the sum of the harmonic amplitudes to the fundamental gives a direct measurement of distortion. The number of harmonics, which are used for the THD calculation, may vary depending on the particular application.

### THD + N

The distortion plus noise (THD + N) is the ratio of the sum of the harmonic distortion and noise to the rms power of the input signal. The distortion and noise are measured separately and then added together to form the ratio. The noise voltage relates to the measured bandwidth.

## Dynamic Specifications



2-24

## Dynamic Specifications

### SNR

For a full-scale sinewave input, the theoretical SNR for an N bit converter is given by:  $\text{SNR} = 6.02N + 1.76 \text{ dB}$  as already derived before. The normal way of measuring the SNR for a converter is to digitize a full-scale sinewave and then perform an FFT on the output. The rms power of the fundamental is then compared to the noise floor by inserting a notch filter at the input frequency and the harmonics so that the output is purely due to the effects of noise. The ratio of the two is taken to give a direct measurement of the SNR.

### THD

As in SNR testing, the normal way of measuring the distortion for a converter is to digitize a full-scale sinewave input and then perform an FFT on the output. The rms power of the fundamental is then compared to the sum of the harmonics by inserting a notch filter at the input frequency and the harmonics so that the output is purely due to the effects of harmonics. The ratio of the sum of the harmonic amplitudes to the fundamental gives a direct measurement of distortion. The number of harmonics, which are used for the THD calculation, may vary depending on the particular application.

### THD + N

The distortion plus noise (THD + N) is the ratio of the sum of the harmonic distortion and noise to the rms power of the input signal. The distortion and noise are measured separately and then added together to form the ratio. The noise voltage relates to the measured bandwidth.

## SINAD

The signal to distortion plus noise (SINAD) is the ratio of the input signal to the sum of the harmonic distortion and noise. The distortion and noise are measured separately and then added together to form the ratio. The SINAD is the reciprocal to the THD + N. The SINAD and THD+N are a good indication of the overall dynamic performance of the ADC, because all components of noise and distortion are included.

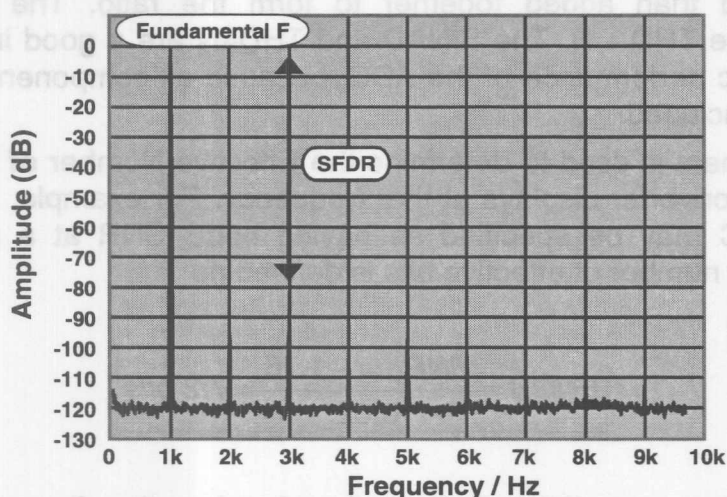
This measurement is used to determine the **Effective Number of Bits (ENOB)** of accuracy the converter displays at that frequency. For example, a nominal 8 bit resolution ADC may be specified as having 45dB SNR at a particular input frequency. The number of effective bits is defined as

$$ENOB = \frac{SNR_{REAL} - 1.76}{6.02} = 7.2 \text{ bits}$$

The actual performance of the device is therefore less than its nominal resolution at this frequency.



## Spurious Free Dynamic Range (SFDR)



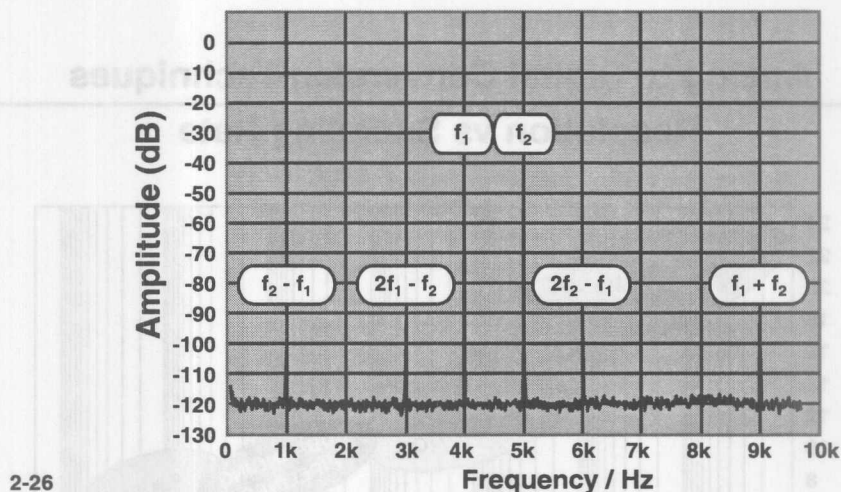
2-25

### Spurious-Free Dynamic Range

The Spurious-Free Dynamic Range (SFDR) is also a very important dynamic specification for wide dynamic range and high frequency applications. The SFDR is the difference in dB between the maximum signal component and the largest distortion component as shown in the picture. The SFDR becomes an issue when the spectral purity of a converter is important. This is the case for A/D converters in noisy receiver environments where the converter must digitize a small-amplitude signal.

The SFDR of the 10-bit 20 Msps A/D converter TLC876 is typically 64 dB at 20 Msps with a 3.58 MHz input signal. The SFDR of the 8-bit 40 Msps A/D converter TLC5540 is typically 46 dB at 40 Msps with a 3 MHz input signal.

## Intermodulation Distortion, IMD



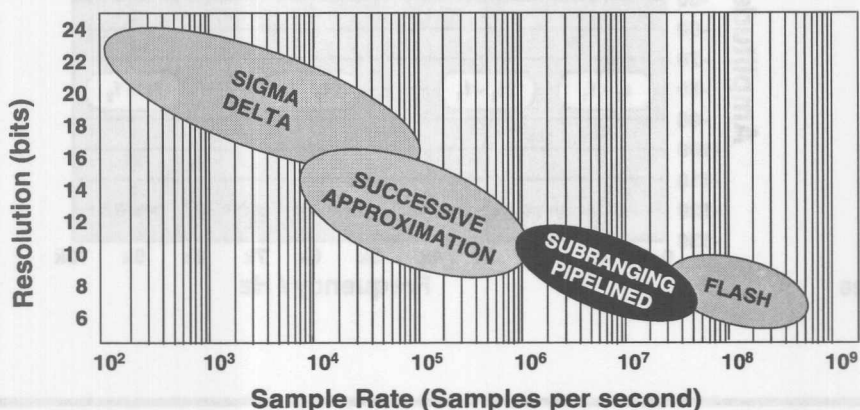
### Intermodulation Distortion IMD

Intermodulation distortion is a measurement of how much one frequency modulates another frequency within a system. Two frequencies are added together and applied to the system. The output harmonic products are measured and the value is also a measure of linearity. The more linear the system is, the lower the intermodulation products become. The second order terms are:  $f_1 + f_2$  and  $f_2 - f_1$ . Third order terms are:  $2f_1 + f_2$ ,  $2f_1 - f_2$ ,  $f_1 + 2f_2$  and  $f_1 - 2f_2$ . Especially when the distortion frequencies are close to the original frequencies, it will be very difficult to filter these out. Also in RF applications, the IMD products can mask out the information of very small-amplitude signals.

## A/D Converter Architectures



### Analog to Digital Conversion Techniques Resolution vs Sampling Rate



2-28

### Analog to Digital Conversion Techniques

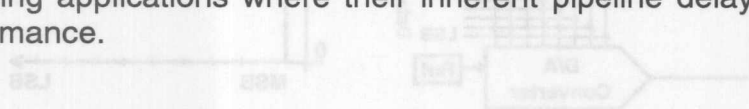
The analog to digital converter (ADC) is a vital component in many of today's digital signal processing systems. The architecture used to implement the ADC is determined by the combination of sample rate and resolution for which the converter is specified. The picture shows four of the most popular conversion methods.

The successive approximation register (SAR) method has been used extensively throughout the last two decades to produce a wide range of ADCs with individual resolutions ranging from 8 to 16 bits. For a particular IC process, sample rates of these converters are inversely proportional to the resolution. This is because the conversion method requires one clock cycle to produce each bit of the output result. This limits the maximum practical sample rate which SAR type ADCs can achieve. However, successive approximation architectures do offer parallel data output.

The sigma delta method has grown in popularity in recent years, particularly for sample rates below 100 ksp/s. They are used extensively for the conversion of audio signals. This technique lends itself well to oversampling followed by decimation and digital low pass filtering. It also produces the highest resolution ADC's currently available.

The flash conversion method has previously been favored for achieving sample rates in excess of 15 MSPS. However, the flash method requires  $2^n - 1$  comparators to implement an n-bit converter. This means that 255 comparators are needed for an 8-bit ADC. Flash converters therefore occupy a relatively large area of silicon, require a lot of power, have a high input capacitance and are expensive.

Semi-flash and, more generally, subranging architectures offer a good compromise between lower power/cost and the high speed of the flash approach. Recently pipelined architectures have been gaining in popularity because they offer an excellent combination of high sample rates, relatively small IC area and moderate cost. They are particularly suitable for continuous sampling applications where their inherent pipeline delay will not affect system performance.



The successive approximation ADC requires  $N$  sequential comparisons.

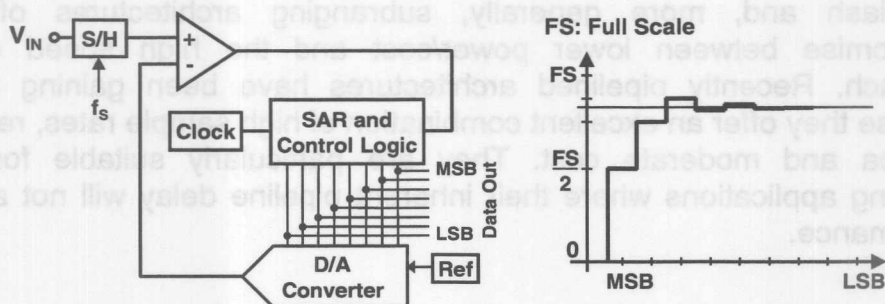
2-29

## Successive Approximation ADC

Successive approximation is a common technology for A/D converters. A conversion time from 100  $\mu$ s to below 1  $\mu$ s and a resolution up to around 18 bits is possible and make this type of ADC still the most popular type of converter.

Successive comparison of an unknown analog input voltage with binary weighted values of a reference give this method its name of "successive approximation." A converter of  $N$ -bit resolution takes " $N$ " steps to achieve a digital output. The conversion technique is the following. One input of the comparator, shown in the block diagram, is driven by an unknown input signal,  $V_{in}$ , while the output of the DAC drives the other. The successive-approximation register (SAR) provides the input to the DAC. When the DAC has its MSB set to logic level 1 (with all other bits zero) by the successive-approximation register (SAR), it will produce a voltage output of  $1/2$  the reference (analog input full-scale range). The comparator then determines if the DAC output is above or below the unknown input signal. If, as shown, the input signal  $V_{in}$  is above the DAC output value, the MSB is retained in the successive-approximation register while the next weight of  $1/4$  the reference is compared. This process continues until all bits are tested and the nearest approximation to the input signal is obtained. The result is then passed to the output register. While the successive-approximation converter process continues, the input signal must be held constant using a sample-and-hold circuit in front of the comparator. Alternatively, the signal should, as a rule of thumb, vary a maximum of  $1/2$  LSB during conversion. This puts a slow-rate or full-scale frequency limitation on the signals the converter can handle.

## Successive Approximation ADC



The successive approximation ADC requires N sequential comparisons.

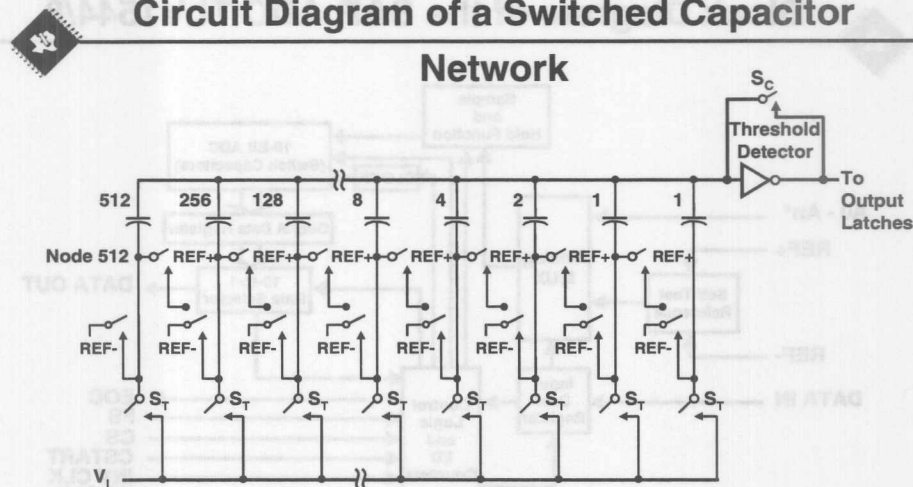
2-30

### Successive Approximation ADC

Successive approximation is a common technology for A/D converters. A conversion time from 100  $\mu$ s to below 1  $\mu$ s and a resolution up to around 16 bits is possible and make this type of ADC still the most popular type of converter.

Successive comparison of an unknown analog input voltage with binary weighted values of a reference give this method its name of "successive approximation". A converter of N-bit resolution takes "N" steps to achieve a digital output. The conversion technique is the following. One input of the comparator, shown in the block diagram, is driven by an unknown input signal,  $V_{IN}$ , while the output of the DAC drives the other. The successive-approximation register (SAR) provides the input to the DAC. When the DAC has its MSB set to logic level 1 (with all other bits zero) by the successive-approximation register (SAR), it will produce a voltage output of 1/2 the reference (analog input full-scale range). The comparator then determines if the DAC output is above or below the unknown input signal. If, as shown, the input signal  $V_{IN}$  is above the DAC output value, the MSB is retained in the successive-approximation register while the next weight of 1/4 the reference is compared. This process continues until all bits are tested and the nearest approximation to the input signal is obtained. The result is then passed to the output register. While the successive-approximation converter process continues, the input signal must be held constant using a sample-and-hold circuit in front of the comparator. Alternatively, the signal should, as a rule of thumb, vary a maximum of 1/2 LSB during conversion. This puts a slew-rate or full-scale frequency limitation on the signals the converter can handle.

### Circuit Diagram of a Switched Capacitor Network

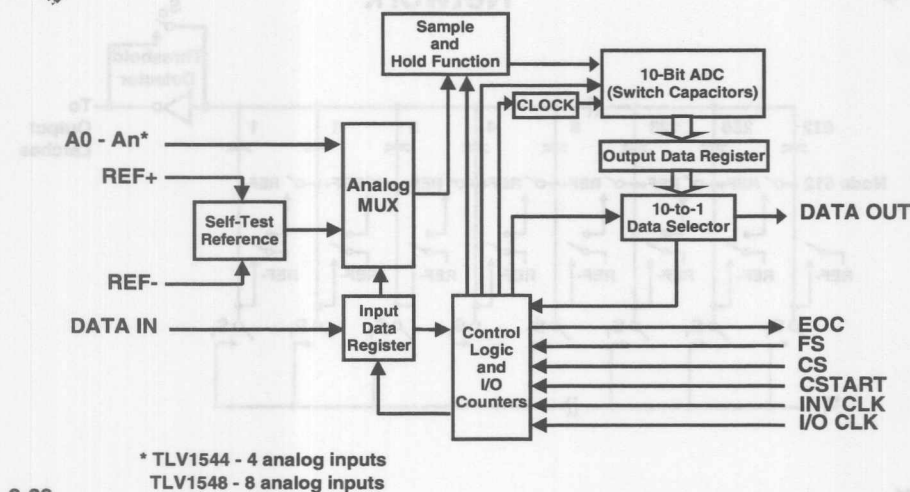


2-31

### Circuit Diagram of a Switched Capacitor Network

The CMOS threshold detector in the successive-approximation conversion system determines the value of each bit by examining the charge on a series of binary-weighted capacitors (see picture). In the first phase of the conversion process, the analog input is sampled by closing the  $S_C$  switch and all  $S_T$  switches simultaneously. This action charges all of the capacitors to the input voltage. In the next phase of the conversion process, all  $S_T$  and  $S_C$  switches are opened and the threshold detector begins identifying bits by identifying the charge (voltage) on each capacitor relative to the reference ( $REF-$ ) voltage. In the switching sequence, ten capacitors are examined separately until all ten bits are identified and then the charge-convert sequence is repeated. In the first step of the conversion phase, the threshold detector looks at the first capacitor (weight = 512). Node 512 of this capacitor is switched to the  $REF+$  voltage, and the equivalent nodes of all the other capacitors on the ladder are switched to  $REF-$ . If the voltage at the summing node is greater than the trip point of the threshold detector (approximately one-half  $V_{CC}$ ), a bit 0 is placed in the output register and the 512-weight capacitor is switched to  $REF-$ . If the voltage at the summing node is less than the trip point of the threshold detector, a bit 1 is placed in the register and the 512-weight capacitor remains connected to  $REF+$  through the remainder of the successive-approximation process. The process is repeated for the 256-weight capacitor, the 128-weight capacitor, and so forth down the line until all bits are counted. With each step of the successive-approximation process, the initial charge is redistributed among the capacitors. The conversion process relies on charge redistribution to count and weigh the bits from MSB to LSB.

# Block Diagram of the SAR ADC TLV1544/8

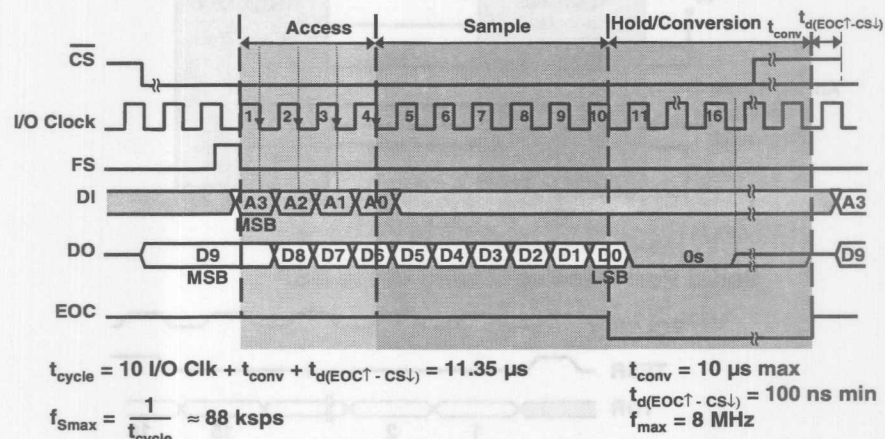


2-32

## Block Diagram of the SAR ADC TLV1544/8

The picture shows the block diagram of the TLV1544/8 which is typical for a successive approximation ADC (SAR ADC). The ADC has an analog multiplexer on chip, where the analog input channel is selected. Further programmable features like self-test reference, programmable conversion rate, power-down state and the conversion speed can be chosen. These different choices have to be written into the Input Data Register. The analog input signal is sampled and held, and the converted signal is written into the Output Data Register where it can be read out via the 10-to-1 Data Selector and the Data Out pin of the device. The selection of the desired mode of the ADC needs specific timing, which is shown on the next page.

### Maximum Sampling Rate of the TLV1544/8



2-33

### Maximum Sampling Rate of the TLV1544/8

A frequently asked question is how to calculate the maximum sampling frequency of an A/D converter. The figure shows the timing diagram of the 10-bit serial A/D converter TLV1544/8. The first four I/O CLK cycles load the input data register with the 4-bit input data on DATA IN that selects the desired analog channel. The next six clock cycles provide the control timing for sampling the analog input. The sampled analog input is held after the first I/O CLK sequence of ten clocks. The tenth clock edge also takes EOC low and begins the conversion. The conversion time depends on the selected mode. If the fast conversion is selected, the maximum conversion time will be 10  $\mu\text{s}$  (40  $\mu\text{s}$  in the slow conversion mode). Therefore, the maximum sampling frequency can be calculated as follows:

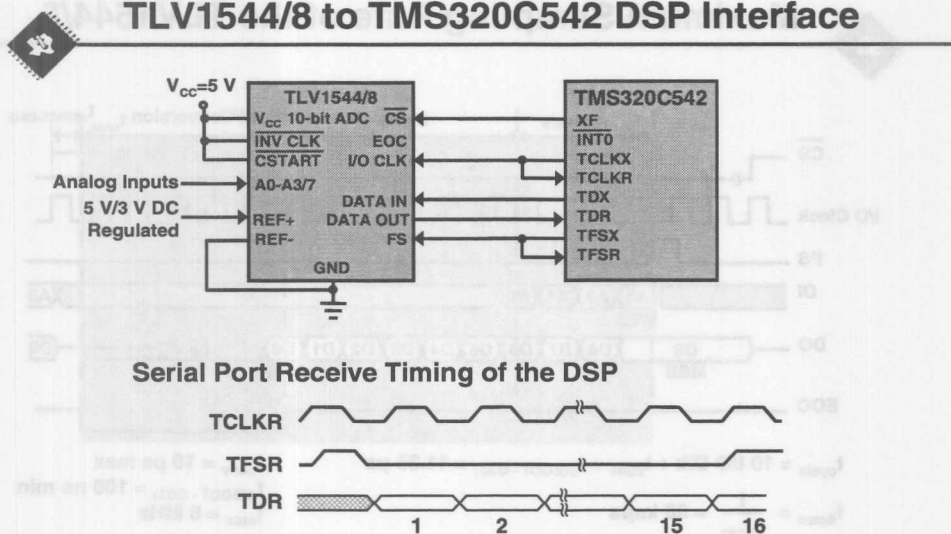
$$f_s = \frac{1}{t_{\text{cycle}}}$$

The cycle time of a complete conversion is given by:

$$t_{\text{cycle}} = 10 \text{ I/O Clk} + t_{\text{conv}} + t_{d(\text{EOC}\uparrow - \text{CS}\downarrow)}$$

The minimum delay time, EOC  $\uparrow$  to CS low is 100 ns. With a maximum I/O CLK frequency of 8 MHz, the maximum sampling frequency results in around 88 ksp/s. However, at this high sampling frequency the driving source resistance has to be taken into account.

## TLV1544/8 to TMS320C542 DSP Interface



2-34

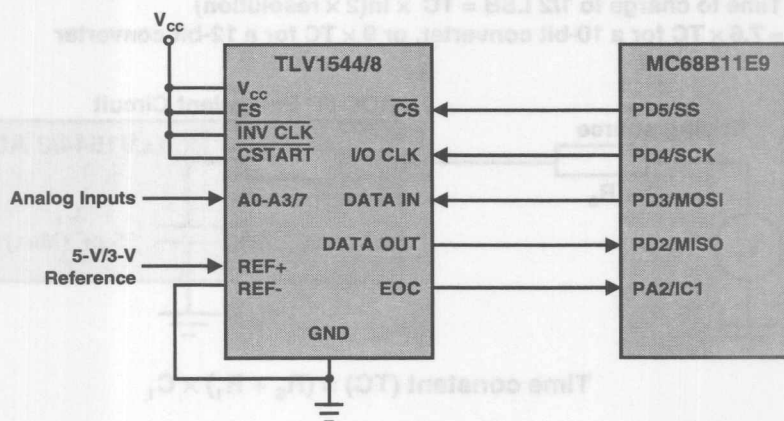
### Interfacing the TLV1544/8 to the TMS320C542 DSP

The circuit diagram shows the configuration that can be used to interface the A/D converter TLV1544/8 to the fixed point DSP TMS320C542.

The timing diagram of the TLV1544/8 was already shown before in combination with the maximum sampling rate of this converter. The I/O Clock signal is in this interface generated by the DSP and oscillates continuously. When CS is brought low by using the XF output of the DSP and a Frame Sync (FS) signal is received on the FS pin, the TLV1544/8 starts simultaneously to receive the next operation mode byte (DATA IN) and to send the last converted value (DATA OUT). Once the first four input bits have been received, any more data to the input is ignored.

Conversion complete is determined using a software routine and a DSP internal timer. This configuration is described in an application report. The EOC signal can be used with an inverter connected to an interrupt.

## Interfacing the 10-bit ADC TLV1544/8 to a SPI



2-35

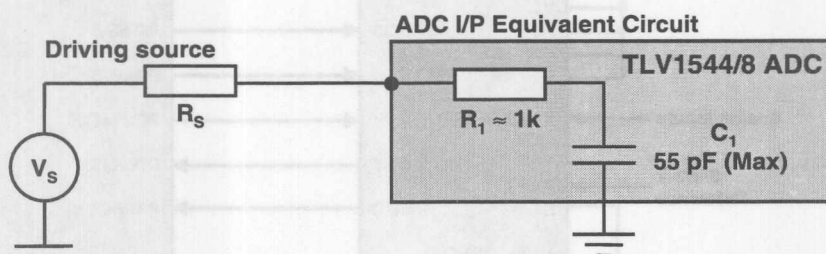
### Interfacing the TLV1544/8 to a SPI

A very efficient way to interface an ADC to a Microcontroller is to use the SPI (Serial Peripheral Interface). Microcontrollers which include the SPI interface are for instance the TMS370C10 and the MC68HC11.

A SPI consists of an 8-bit serial shift register, which is initially loaded by software with the mode-control data to be sent to the ADC input. The SPI transfer is then initiated by software. This automatically starts the output of serial data from the MOSI (Master Out Slave In) pin of the microcontroller. At the same time data from the previous conversion result is received at the MISO (Master In Slave Out) pin of the microcontroller. This data is shifted into the other end of the serial shift register. On completion of an 8-bit SPI transfer the new content of the shift register is automatically loaded into a serial input buffer ready to be read by the next software instruction in the routine.

## Driving the Input of a Switched Capacitor ADC

- Driving source needs to charge  $C_1$  to within 1/2 LSB during sampling time
- Time to charge to 1/2 LSB =  $TC \times \ln(2 \times \text{resolution})$
- $\approx 7.6 \times TC$  for a 10-bit converter, or  $9 \times TC$  for a 12-bit converter



$$\text{Time constant (TC)} = (R_s + R_1) \times C_1$$

2-37

## Driving the Input of a Switched Capacitor ADC

Switched capacitor ADCs offer an inherent sample-and-hold function at their input. This avoids the need to provide an external sample-and-hold but care should be taken to ensure that sufficient time is allowed during the sampling phase of the conversion process. For correct operation of the ADC, the capacitor must be charged to the required accuracy of 1/2 LSB or more during the sampling phase of the ADC. The voltage  $V_C$  on capacitor  $C_1$  is given by:

$$V_C = V_s(1 - e^{-t/TC})$$

where  $TC$  is the time constant  $C_1(R_s + R_1)$ . Therefore, we get:

$$e^{-t/TC} = (1 - \frac{V_C}{V_s}), \text{ and } -t/TC = \ln(1 - \frac{V_C}{V_s})$$

Hence for a full-scale change in input voltage, the time to settle to 1/2 LSB for a converter with resolution  $N$  ( $N=2^n$ ) is:

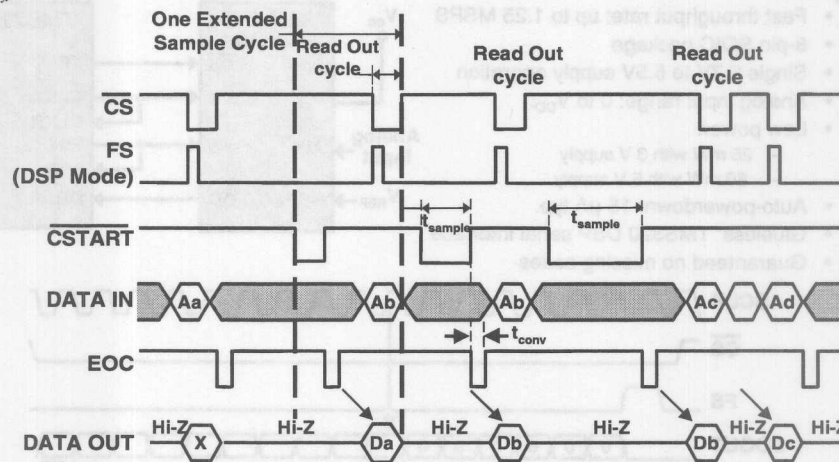
$$t = -TC \times \ln(1 - \frac{V_s - \frac{1}{2} \text{LSB}}{V_s}) = -TC \times \ln(\frac{\text{LSB}}{2V_s}) = TC \times \ln(\frac{2V_s}{\text{LSB}}) = TC \times \ln(\frac{2 \times N \times \text{LSB}}{\text{LSB}})$$

$$t = TC \times \ln(2 \times N)$$

This therefore sets a maximum limit on the source impedance when driving into a capacitive ladder ADC. The maximum I/O CLK frequency for the TLV1544/8 is 8 MHz (this results with 6 I/O CLK cycles into 0.75  $\mu$ s sampling time). To achieve this high sampling frequency, the source resistance has to be smaller than 800  $\Omega$ .



## TLV1544/8 Extended Sampling Operation



2-38

### Extended Sampling Operation of the TLV1544/8

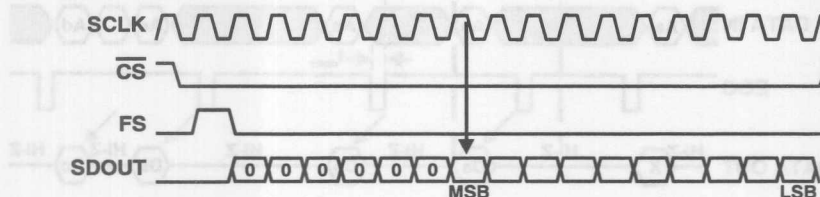
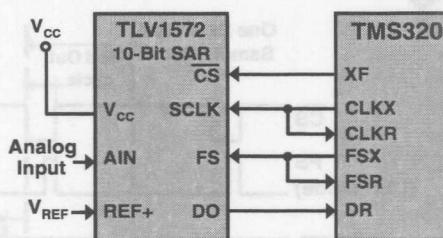
The extended sampling mode of operation programs the acquisition time ( $t_{ACQ}$ ) of the sample-and-hold circuit. This allows the analog inputs of the device to be directly interfaced to a wide range of input source impedances. Power consumption for the extended sampling mode depends on the duration of the sampling period chosen.

The CSTART signal controls the sampling period and starts the conversion. The falling edge of CSTART initiates the sampling period of a preset channel. The low time of CSTART controls the acquisition time of the input sample-and-hold circuit. The sample is held on the rising edge of CSTART. Asserting CSTART causes the converter to perform a new sample of the signal on the selected valid MUX channel (one of eight) and discard the current conversion result ready for output. Sampling continues as long as CSTART is active (negative). The rising edge of CSTART ends the sampling cycle. The conversion cycle starts two internal system clocks after the rising edge of CSTART. Immunity to digital noise is improved since the extended sampling mode acquires the input signal when the digital circuitry is shut down.

Once the conversion is complete, the processor can initiate a normal I/O cycle to read the conversion result and select the input channel for the next conversion.

## Interfacing the TLV1572 to the TMS320 DSP

- Fast throughput rate: up to 1.25 MSPS
- 8-pin SOIC package
- Single 2.7V to 5.5V supply operation
- Analog input range: 0 to  $V_{DD}$ .
- Low power:
  - 25 mW with 3 V supply
  - 50 mW with 5 V supply
- Auto-powerdown: 15  $\mu$ A typ.
- Glueless TMS320 DSP serial interface
- Guaranteed no missing codes



2-36

## Interfacing the TLV1572 to the TMS320 DSP

The TLV1572 is a 10-bit, 1.25 Msps successive approximation analog-to-digital converter, which has one analog input channel (AIN), a chip-select (CS), serial clock (SCLK) and a serial data output. An additional input called frame sync (FS) initiates the data transfer when using a DSP and connects to the DSP serial port FSX pin. A high level on the CS pin disables the device, puts it in a power down mode and switches DATA OUT to high impedance. When taken low, CS enables the device inputs, but no data is transferred until the falling edge of FSX is received from the DSP to FS. After the falling edge of DSP FSX, the TLV1572 starts shifting the data out on the DO line. After six null bits, the 10 bit A/D conversion data becomes available.

## Selection Guide: Successive Approximation ADCs

**Successive Approximation ADC's**

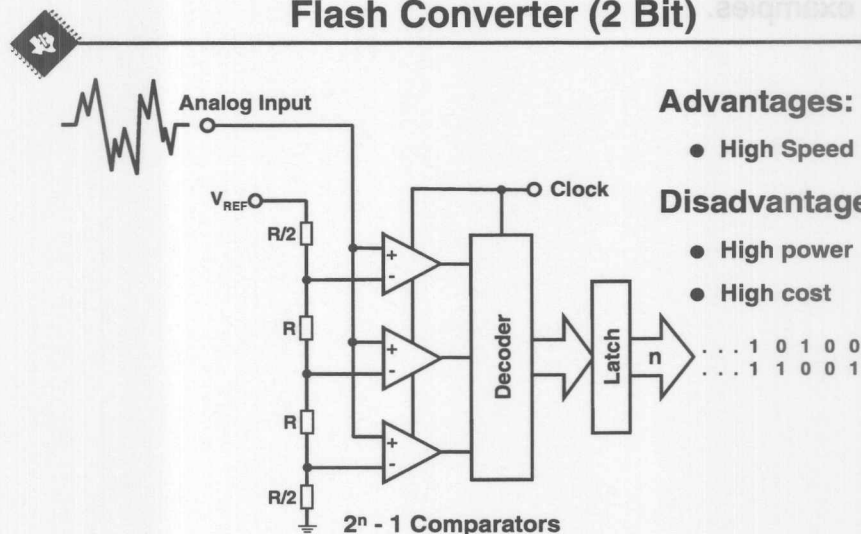
| Part Number                                | Linearity [LSB] | Conversion Time [us] | Sampling Rate [kSPS] | Number of Inputs | Power Supply [V] | Parallel or Serial Output | Internal Clock | Powerdown | Power Consumption [mW] |
|--------------------------------------------|-----------------|----------------------|----------------------|------------------|------------------|---------------------------|----------------|-----------|------------------------|
| <b>10-bit Analog-to-Digital Converters</b> |                 |                      |                      |                  |                  |                           |                |           |                        |
| <b>TLC1540</b>                             | ±0.5            | 21                   | 32                   | 11               | 5                | S                         |                |           | 12                     |
| <b>TLC1541</b>                             | ±1.0            | 21                   | 32                   | 11               | 5                | S                         |                |           | 12                     |
| <b>TLC1542</b>                             | ±1.0            | 21                   | 38                   | 11               | 5                | S                         | Y              |           | 12                     |
| <b>TLC1543</b>                             | ±1.0            | 21                   | 38                   | 11               | 5                | S                         | Y              |           | 12                     |
| <b>TLC1549</b>                             | ±1.0            | 21                   | 38                   | 1                | 5                | S                         | Y              |           | 12                     |
| <b>TLV1543</b>                             | ±1.0            | 21                   | 38                   | 11               | 3.3              | S                         | Y              |           | 12                     |
| <b>TLV1544</b>                             | ±1.0            | 10                   | 66                   | 4                | 3-5              | S                         | Y              | Y         | 3                      |
| <b>TLV1548</b>                             | ±1.0            | 10                   | 66                   | 8                | 3-5              | S                         | Y              | Y         | 3                      |
| <b>TLV1549</b>                             | ±1.0            | 21                   | 38                   | 1                | 3.3              | S                         | Y              |           | 8                      |
| <b>TLC1550</b>                             | ±0.5            | 6                    | 164                  | 1                | 5                | P                         | Y              |           | 40                     |
| <b>TLC1551</b>                             | ±1.0            | 6                    | 164                  | 1                | 5                | P                         | Y              |           | 40                     |
| <b>TLV1570</b>                             | ±0.5            | 0.8                  | 1250                 | 8                | 2.7-3.6          | S                         |                | Y         | 21                     |
| <b>TLV1572</b>                             | ±0.5            | 0.8                  | 1250                 | 1                | 3-5              | S                         |                | Y         | 20                     |
| <b>12-bit Analog-to-Digital Converters</b> |                 |                      |                      |                  |                  |                           |                |           |                        |
| <b>TLC2543</b>                             | ±1.0            | 10                   | 66                   | 11               | 5                | S                         | Y              | Y         | 12.5                   |
| <b>TLV2543</b>                             | ±1.0            | 10                   | 66                   | 11               | 3.3              | S                         | Y              | Y         | 12.5                   |

## Successive Approximation ADC's

| Part Number                               | Linearity<br>[LSB] | Conversion<br>Time [us] | Sampling<br>Rate [kSPS] | Number of<br>Inputs | Power Supply<br>[V] | Parallel or<br>Serial Output | Internal Clock | Powerdown | Power<br>Consumption<br>[mW] |
|-------------------------------------------|--------------------|-------------------------|-------------------------|---------------------|---------------------|------------------------------|----------------|-----------|------------------------------|
| <b>Serial Output ADCs</b>                 |                    |                         |                         |                     |                     |                              |                |           |                              |
| <b>8-bit Analog-to-Digital Converters</b> |                    |                         |                         |                     |                     |                              |                |           |                              |
| TLC0831                                   | ±1.0               | 13.3                    | 28                      | 1                   | 5                   | S                            |                |           | 12.5                         |
| TLC0832                                   | ±1.0               | 13.3                    | 28                      | 2                   | 5                   | S                            |                |           | 26                           |
| TLC0834                                   | ±1.0               | 13.3                    | 28                      | 4                   | 5                   | S                            |                |           | 12.5                         |
| TLC0838                                   | ±1.0               | 13.3                    | 22                      | 8                   | 5                   | S                            |                |           | 12.5                         |
| TLC540                                    | ±0.5               | 9                       | 75                      | 11                  | 5                   | S                            |                |           | 12                           |
| TLC541                                    | ±0.5               | 17                      | 40                      | 11                  | 5                   | S                            |                |           | 12                           |
| TLC542                                    | ±0.5               | 20                      | 25                      | 11                  | 5                   | S                            | Y              |           | 10                           |
| TLC545                                    | ±0.5               | 9                       | 76                      | 19                  | 5                   | S                            |                |           | 12                           |
| TLC546                                    | ±0.5               | 17                      | 40                      | 19                  | 5                   | S                            |                |           | 12                           |
| TLC548                                    | ±0.5               | 17                      | 45.5                    | 1                   | 5                   | S                            | Y              |           | 12                           |
| TLC549                                    | ±0.5               | 17                      | 40                      | 1                   | 5                   | S                            | Y              |           | 12                           |
| TLV0831                                   | ±1.0               | 13.3                    | 28                      | 1                   | 5                   | S                            |                |           | 2.5                          |
| TLV0832                                   | ±1.0               | 13.3                    | 28                      | 2                   | 5                   | S                            |                |           | 8.25                         |
| TLV0834                                   | ±1.0               | 13.3                    | 28                      | 4                   | 5                   | S                            |                |           | 2.5                          |
| TLV0838                                   | ±1.0               | 13.3                    | 22                      | 8                   | 5                   | S                            |                |           | 2.5                          |

## Flash/Pipeline Converters

## Flash Converter (2 Bit)



2-42

## Flash Converter (2 Bit)

The flash analog to digital converter provides the fastest conversion method today. This is achieved by a simultaneous comparison of the analog input signal with  $2^n - 1$  reference voltages. These reference voltages are generated with a voltage divider, which is built by a resistor chain. Each reference voltage is connected to the inverting input of a comparator. Again, for an  $n$ -bit resolution,  $2^n - 1$  comparators are required with threshold voltages varying by 1 LSB. The analog input signal is connected to the noninverting input of every comparator. The output is low for every comparator where the analog input signal is smaller than the reference voltage. The output is high for every comparator where the analog input signal is higher than the reference voltage. The decoded digital output data, which is  $n$  bits wide, is written into a latch.

As previously mentioned, flash converters have been favored for achieving high sample rates. However, the flash method requires  $2^n - 1$  comparators to implement an  $n$ -bit converter. This means that 255 comparators are needed for an 8-bit ADC and 4095 comparators for a 12 bit flash converter. Flash converters therefore occupy a relatively large area of silicon, require a lot of power, have a high input capacitance and are expensive.

A technology, which reduces the number of comparators, is the semi-flash converter. The semi-flash concept is first to digitize the upper 4 bits, which are fairly insensitive to noise. The converted 4 bits are then input to a 4 bit DAC, and subtracted from the original analog input, to create a residue voltage. This

residue is then digitized to provide the lower 4 bits of information. For an 8-bit converter, this architecture can be implemented with 31 comparators, (an 8x reduction from the flash ADC). This yields improvements in cost, power and input capacitance. The semi-flash architecture is a popular choice for 8 bit, 20 MSPS ADCs. The TLC0820, TLC5510, TLC5733 and TLC5540 from Texas Instruments are all good examples.

## Advantages:

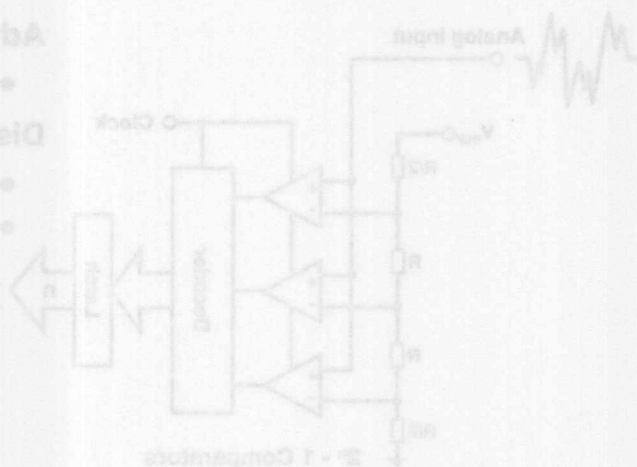
- High Speed

## Disadvantages:

- High Power

- High Cost

10100  
11001



2-42

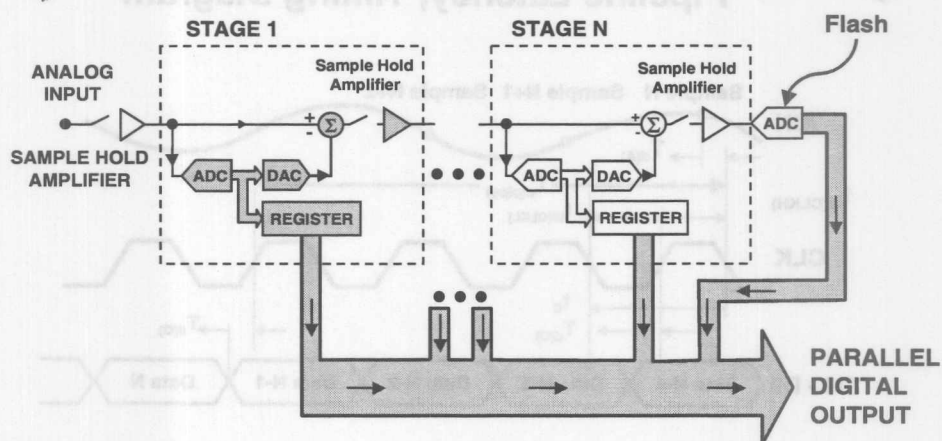
## Flash Converter (2 Bit)

The flash analog to digital converter provides the fastest conversion method today. This is achieved by a simultaneous comparison of the analog input signal with  $2^{n-1}$  reference voltages. These reference voltages are generated with a voltage divider, which is built by a resistor chain. Each reference voltage is connected to the inverting input of a comparator. Again, for an  $n$ -bit resolution,  $2^{n-1}$  comparators are required with threshold voltages varying by 1 LSB. The analog input signal is connected to the noninverting input of every comparator. The output is low for every comparator where the analog input signal is smaller than the reference voltage. The output is high for every comparator where the analog input signal is higher than the reference voltage. The decoded digital output data, which is  $n$  bits wide, is written into a latch.

As previously mentioned, flash converters have been favored for achieving high sample rates. However, the flash method requires  $2^{n-1}$  comparators to implement an  $n$ -bit converter. This means that 255 comparators are needed for an 8-bit ADC and 4095 comparators for a 12 bit flash converter. Flash converters therefore occupy a relatively large area of silicon, require a lot of power, have a high input capacitance and are expensive.

A technology, which reduces the number of comparators, is the semi-flash converter. The semi-flash concept is first to digitize the upper 4 bits, which are fairly insensitive to noise. The converted 4 bits are then input to a 4 bit DAC, and subtracted from the original analog input, to create a residue voltage. This

## N Stage Pipelined ADC Architecture



2-43

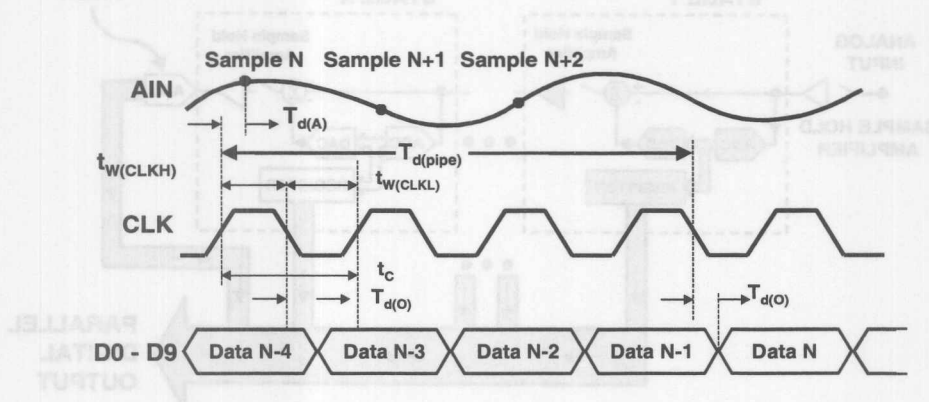
### N Stage Pipelined ADC Architecture

Higher sample rates than successive approximation techniques can be achieved cost effectively by using the pipelined architecture. The functional block diagram of this conversion method is shown in the picture. It consists of a number of individual  $n$ -bit resolution (typically  $n = 2$  or  $4$ ) converter stages which are cascaded to form the complete converter. Each stage comprises of an  $n$ -bit ADC, an  $n$ -bit DAC, a sample/hold amplifier and a data register. The sample/hold should be  $N$  bits accurate where  $N$  is the resolution of the overall ADC. For a semi-flash (or 2 step) architecture, this is usually done in 2 stages. For an 8 bit ADC, the upper 4 bits are converted then the lower 4 bits.

The ADC operates as follows. The analog input signal is sampled and held. The first stage produces the first  $n$  MSBs of the overall ADC conversion result. This  $n$ -bit result is then reconverted back into analog form via the  $n$ -bit DAC and is subtracted from the held input signal level. The result of this subtraction is then sampled and held. The next stage then repeats the process performed by the previous stage and this in turn is repeated for subsequent stages. The instant that the result of the subtraction of stage 1 is successfully held, the preceding sample/hold amplifier acquires the next sample of the input signal. This allows the individual  $n$ -bit conversions to occur serially in time. Thus the throughput rate of the overall ADC is increased significantly. In addition, the chip area is significantly reduced from that which would be needed with a full Flash architecture. The pipeline or semi-flash will produce an output for each clock once the pipeline is filled. The number of clocks to fill the pipeline is referred to as latency. For the TI 8 bit semi-flash ADCs, the latency is 2.5 clock periods.

## TLC876, 10-bit and 20 Msps ADC

### Pipeline Latency, Timing Diagram



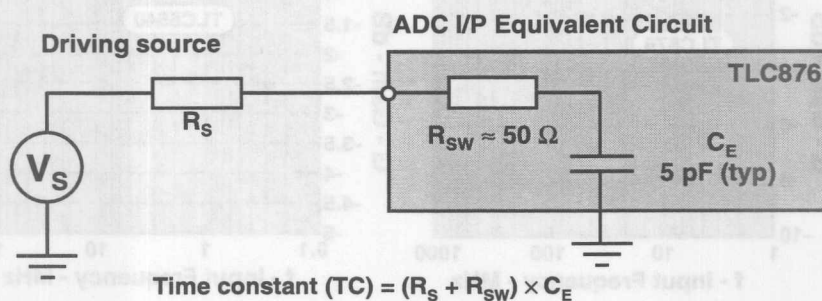
2-44

### TLC876 Pipeline Latency – Timing Diagram

The principle of a pipeline ADC has been explained. The TLC876 uses a multistage pipelined architecture. This pipelined multistage architecture achieves a high sample rate with low power consumption. However, such architecture causes a pipeline latency, which is the number of clock cycles between the conversion initiation on an input sample and the corresponding output data. Once the data pipeline is full, new valid output data are provided every clock cycle. The picture shows a pipeline latency of 3.5 clock cycles for the TLC876.

## Driving the Analog Input of the TLC876

- In the worst case, the source is driving a low input impedance
- Charge or discharge to 1/2 LSB in the sample period of 1/2 of a clock cycle
- $R_s \leq \frac{1}{2 f_{(CLK)} \times C_E \times \ln(2048)} - R_{sw} \leq 278 \Omega$  (for  $C_E = 5 \text{ pF}$ )



2-45

## Driving the Analog Input of the TLC876

The picture shows an equivalent input circuit of the TLC876 sample-and-hold amplifier. The total equivalent capacitance,  $C_E$ , is typically less than 5 pF and the input source must be able to charge or discharge this capacitance to 10-bit accuracy in the sample period of one half of a clock cycle. When the switch S1 closes, the input source must charge or discharge the capacitor  $C_E$  from the voltage already stored on  $C_E$  (the previously captured sample) to the new voltage. In the worst case, a full-scale voltage step on the input, the input source must provide the charging current through the switch resistance  $R_{sw}$  (50  $\Omega$ ) of S1 and quickly settle (within 1/2 CLK period), and, therefore, the source is driving a low input impedance. However, when the source voltage equals the value previously stored on  $C_E$ , the hold capacitor requires no input current to maintain the charge and the equivalent input impedance is extremely high.

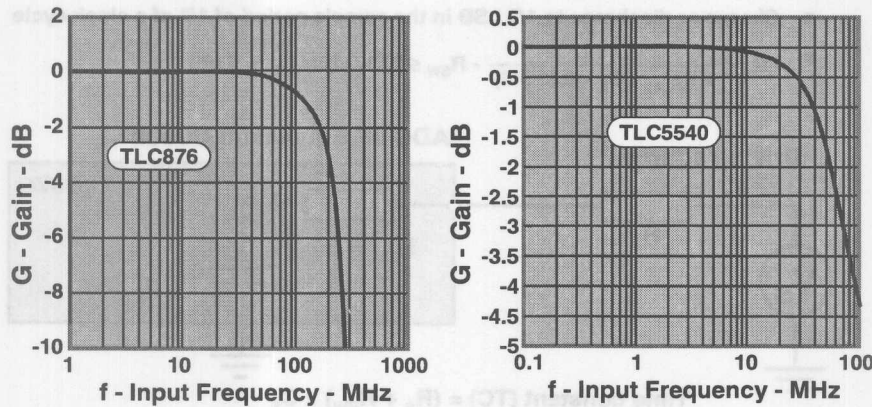
Adding series resistance between the output of the source and the AIN terminal reduces the drive requirements placed on the source. To maintain the frequency performance outlined in the specifications, the resistor should be limited to 200  $\Omega$  minus the source resistance or less. The maximum source resistance,  $R_s$ , for 10-bit, 1/2 LSB accuracy can be calculated by using the equation, already derived:

$$t = TC \times \ln(2 \times n) = TC \times \ln(2 \times \text{Resolution})$$

Therefore,  $R_s$  is given by:

$$R_s \leq \frac{1}{2 f_{(CLK)} \times C_E \times \ln(2048)} - R_{sw}$$

### Analog Input Bandwidth of the TLC876 (10-bit, 20 Msps), TLC5540 (8-bit 40 Msps)



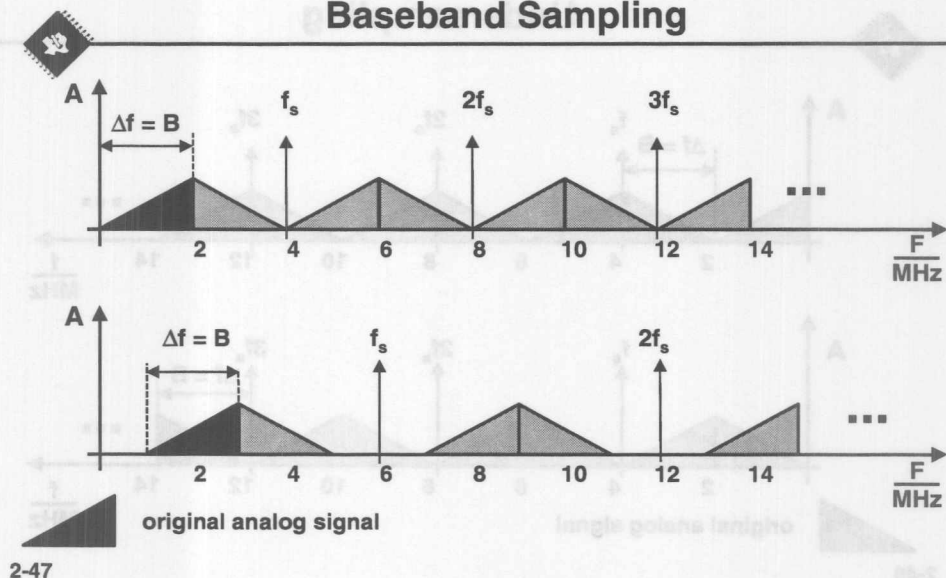
2-46

### Analog Input Bandwidth of the TLC876, TLC5540

TLC876 (10-bit, 20 Msps), TLC5540 (8-bit 40 Msps)

As already discussed the analog input bandwidth of an A/D converter is very important for undersampling applications. An example is shown for the TLC876, a 10-bit, 20 Msps A/D converter. The typical analog input bandwidth of this device is 200 MHz, which makes the device well suited for undersampling applications. A further example is shown for the 40 Msps ADC TLC5540, which has a typical analog input bandwidth of 75 MHz.

## Baseband Sampling



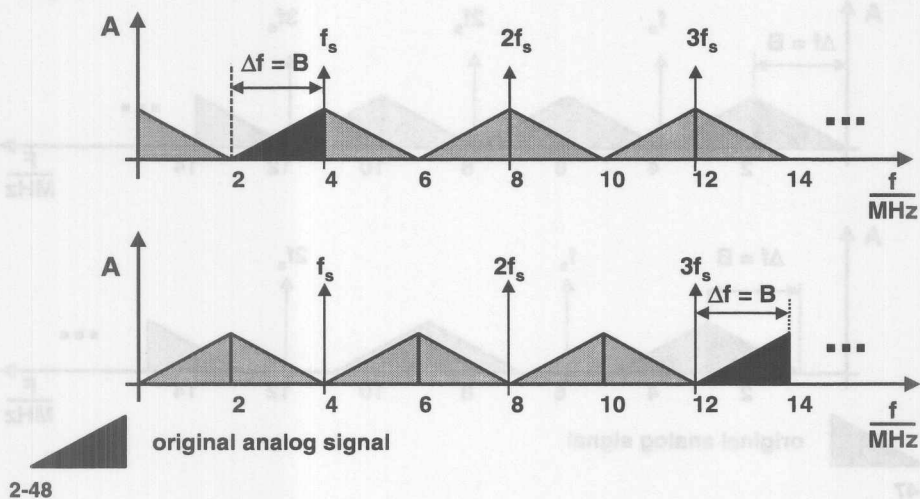
2-47

### Baseband Sampling

Baseband sampling is the type of conversion commonly used. In baseband sampling the actual frequency of the signal to convert does not exceed  $f_s/2$ . Nyquist's criteria states that the bandwidth (not the actual frequency) of the signal being converted should not exceed  $f_s/2$  in order for the information to be preserved. When the actual frequency of the signal to be converted exceeds  $f_s/2$  but the bandwidth does not exceed  $f_s/2$  then this is called undersampling (or Super-Nyquist).

example of this is an analog signal with a bandwidth of 10 MHz. Without using undersampling the minimum sampling frequency is 20 MHz. If undersampling is used, the minimum sampling frequency in this example is only 20 kHz. Another advantage especially in high frequency systems is that the number of analog components, like downmixers, can be reduced. A further big advantage is that the applied speed to the ADC and system can be reduced.

## Undersampling

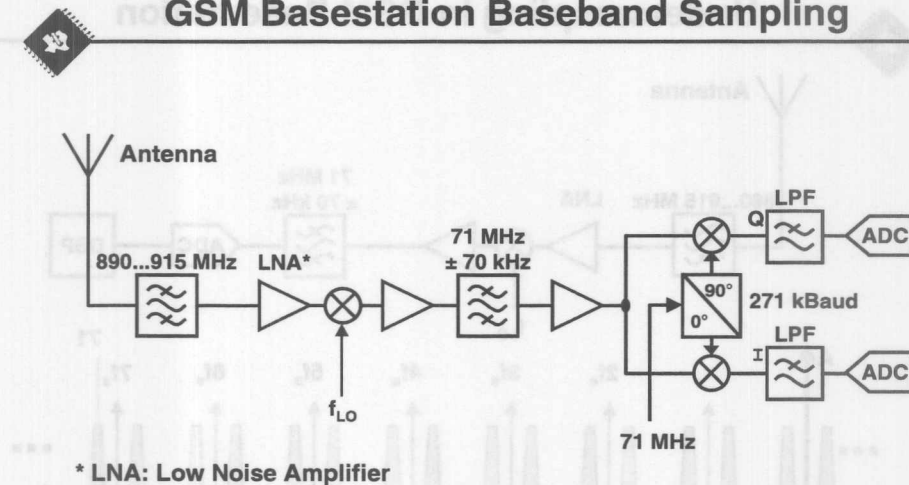


### Undersampling

Undersampling is quite often not well understood. In most cases it is assumed that the analog input signal in front of an ADC has to be limited to less than one half of the sampling frequency of the converter. However, the ADC can convert the analog signal into the right digital signal, if only the bandwidth of the analog signal is limited. This means that a signal in the frequency area above the sampling frequency of the ADC can be converted, if the bandwidth is limited. An example of this is an analog signal with a bandwidth of 100 kHz, which is centered at 10 MHz. Without using undersampling the minimum sampling frequency is 20 MHz. If undersampling is used, the minimum sampling frequency in this example is only 20 kHz. Another advantage especially in high frequency systems is that the number of analog components, like downmixers, can be reduced.

A further big advantage is that the applied speed to the ADC and system can be reduced.

## GSM Basestation Baseband Sampling

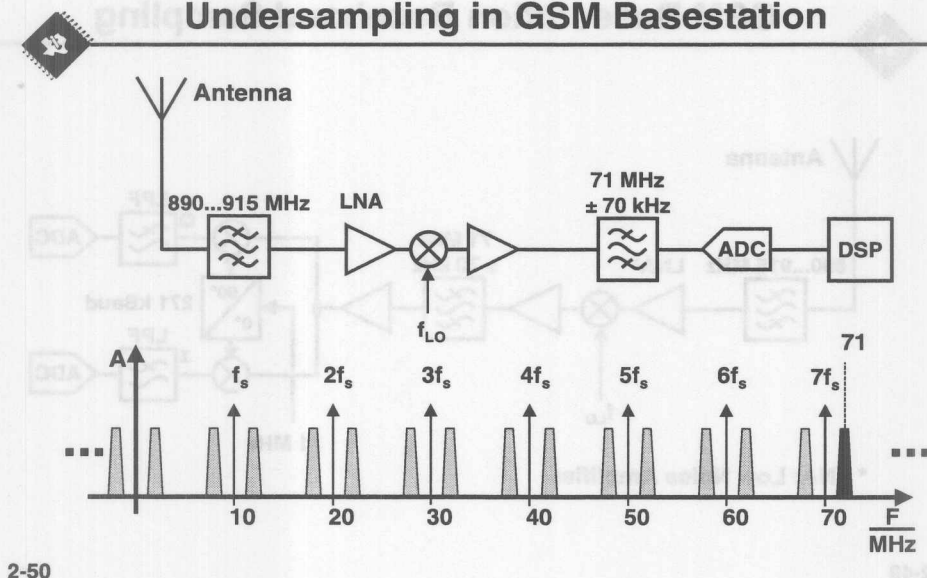


2-49

### GSM Basestation Baseband Sampling

The picture shows a conventional GSM basestation baseband sampling system. The frequency of interest is in the range of 890 to 915 MHz. This range is filtered with a bandpass filter and amplified by a LNA (Low Noise Amplifier). The amplified frequency is mixed down to the IF frequency of 71 MHz  $\pm$  70 kHz. The IF signal is then applied to a quadrature demodulator where the I and Q components are separated. The baseband I(t) and Q(t) signals are then applied to the inputs of A/D converters. The digitized data is further handled by a DSP.

## Undersampling in GSM Basestation



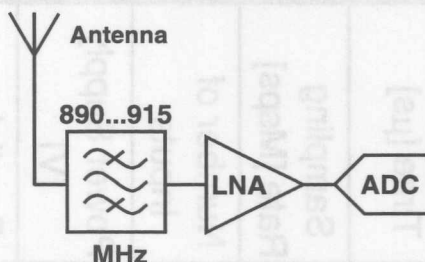
2-50

## Undersampling in GSM Basestation

Today, the intention is to do more and more of the signal processing in the digital domain by using a DSP. Therefore, the ADC moves more and more in the direction of the antenna. The advantage in this example is that the analog I/Q demodulation can be performed digitally. Instead of converting the IF signal using a conventional I and Q demodulator, the IF 71 MHz IF signal is digitized. The band of interest is in this case around 140 kHz. By using undersampling technology, it is not necessary to sample at 140 MHz. The ADC can be operated at a sampling frequency of 10 or 20 Msps. The ADC actually functions as a mixer and aliases the signal down.

## Theoretical Undersampling in GSM

### Basestation



The conversion from analog to digital immediately after the bandpass filter would require an ADC with an analog input bandwidth of more than 900 MHz...

2-51

### Theoretical Undersampling in GSM Basestation

The intention in undersampling applications is to bring the A/D converter as near as possible to the RF antenna of the system. However, this is actually still a problem because of the high analog input bandwidth in combination with the required resolution of the A/D converter. In GSM systems an analog input bandwidth of more than 900 MHz would be required. These bandwidth and resolution requirements are beyond the limits of current technology.

## Selection Guide: Flash/Pipeline ADCs

**Flash/Pipeline ADC's**

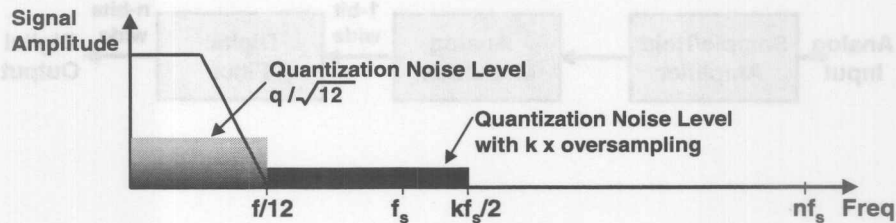
| Part Number                                | Linearity<br>[LSB] | Conversion<br>Time [ $\mu$ s] | Sampling<br>Rate [Msps] | Number of<br>Inputs | Power Supply<br>[V] | Parallel or<br>Serial Output | Internal Clock | Powerdown | Power<br>Consumption<br>[mW] |
|--------------------------------------------|--------------------|-------------------------------|-------------------------|---------------------|---------------------|------------------------------|----------------|-----------|------------------------------|
| <b>Video and High Speed ADCs</b>           |                    |                               |                         |                     |                     |                              |                |           |                              |
| <b>6-bit Analog-to-Digital Converters</b>  |                    |                               |                         |                     |                     |                              |                |           |                              |
| <b>TL5501</b>                              | $\pm 0.5$          | 0.050                         | 20                      | 1                   | 5                   | P                            |                |           | 300                          |
| <b>8-bit Analog-to-Digital Converters</b>  |                    |                               |                         |                     |                     |                              |                |           |                              |
| <b>TLC5510</b>                             | $\pm 0.75$         | 0.050                         | 20                      | 1                   | 5                   | P                            | Y              |           | 90                           |
| <b>TLC5510A</b>                            | $\pm 0.75$         | 0.050                         | 20                      | 1                   | 5                   | P                            | Y              |           | 90                           |
| <b>TLV5510</b>                             | $\pm 1.0$          | ?                             | 10                      | 1                   | 3                   | P                            | ?              | ?         | 60                           |
| <b>TLC5540</b>                             | $\pm 0.75$         | 0.025                         | 40                      | 1                   | 5                   | P                            | Y              |           | 150                          |
| <b>TLC5733A</b>                            | $\pm 0.75$         | 0.050                         | 20                      | 3                   | 5                   | P                            | Y              |           | 375                          |
| <b>10-bit Analog-to-Digital Converters</b> |                    |                               |                         |                     |                     |                              |                |           |                              |
| <b>TLC876</b>                              | $\pm 0.5$          | 0.050                         | 20                      | 1                   | 5                   | P                            | Y              | Y         | 110                          |

## Sigma-Delta Conversion Technology

 The Benefits of Oversampling

## Advantages:

- Reduced noise in band of interest
- Reduced filter requirements



2-54

## The Benefits of Oversampling

An ADC which is sampling an input signal at the Nyquist rate (twice the maximum input bandwidth) will produce a quantization noise, or error, of  $\frac{q}{\sqrt{12}}$  (where  $q$  is the width of one step of the converter) within the signal band of  $f_s/2$ . This is illustrated in the figure. Comparing this quantization noise with the amplitude of a sinewave input we find that the theoretical signal to noise ratio (SNR) is given by the expression

$$\text{Theoretical SNR} = 6.02 \times n + 1.76 \text{ dB}$$

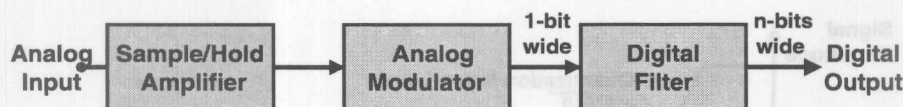
where  $n$  is the resolution of the ADC.

For example, the SNR of a 12 bit ADC has a theoretical upper limit of 74 dB. Using the same equation we find that the theoretical SNR of a 1-bit ADC, sampling at the Nyquist rate,  $f_s$  ( $2 \times$  maximum input frequency of interest) is as high as 7.78 dB!

If we now increase the sampling rate from  $f_s$  to some multiple,  $kf_s$ , we find that the same total amount of quantization noise is spread over a wider bandwidth,  $kf_s/2$  as shown in the figure above. This has the effect of reducing the amount of noise in the signal band of interest. The quantization noise, which now appears outside of the signal band, can be filtered out. This has the overall effect of increasing the resultant SNR in the band of interest. The benefits of oversampling are used to produce excellent performance in sigma-delta converters.



## $\Sigma \Delta$ Converters - Functional Block Diagram



2-55

### Sigma-Delta Converters – Functional Block Diagram

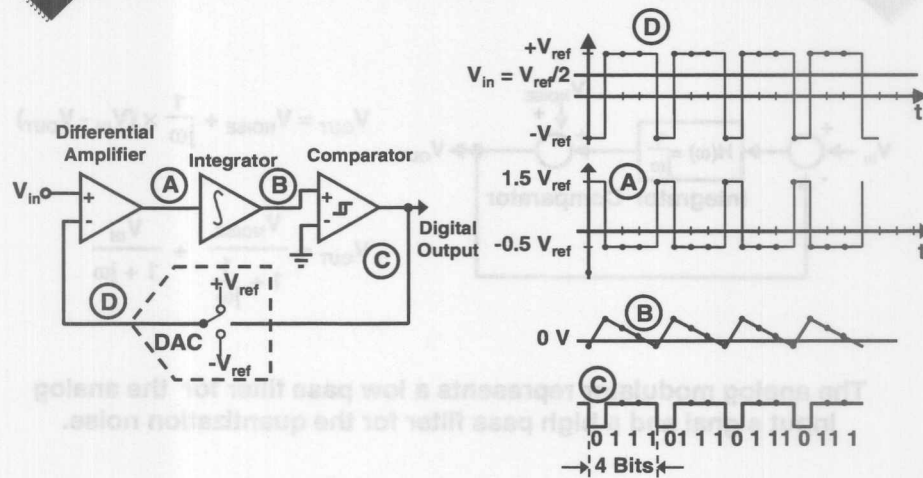
The simplified structure of a Sigma-Delta ADC is shown in the figure above and comprises an analog modulator and a digital filter. The analog modulator, running at a high sampling rate, converts the input signal at its output to a 1-bit pulse density modulated bit stream. The digital filter takes this bit stream and simultaneously removes out of band noise and reduces the bit rate while increasing the output word width.

To increase resolution the analog modulator not only oversamples the input signal but also shapes the quantization noise so it appears in the unwanted band to be removed by the digital filter.

The one bit quantization in the analog modulator provides low differential non-linearity and hence no missing codes in the output. The high input sampling rate means only a non-critical anti-aliasing filter is required and a sample and hold is not required.

The resolution of a Sigma-Delta converter is determined from its output signal to noise ratio.

# 1st Order Analog Modulator



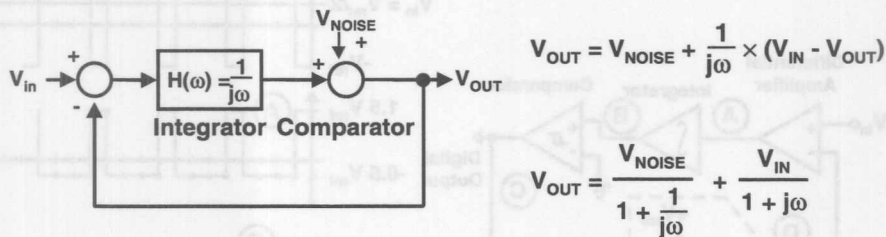
2-56

## 1st Order Modulator

The analog modulator performs the actual analog to digital conversion process. In its simplest form this consists of a differential amplifier, single integrator, comparator and 1-bit DAC connected in a closed loop configuration as shown in the figure above which illustrates a 1st Order modulator. The analog modulator converts the analog input signal into a 1-bit wide serial digital output.

The analog input voltage should not exceed the limits of  $+V_{ref}$  and  $-V_{ref}$ . An example of the modulator operation is given for an analog input voltage of  $V_{in} = +V_{ref}/2$  and where the starting conditions are: output voltage of the integrator  $V_B < 0$  (therefore the output of the comparator is 0), DAC output  $V_D = -V_{ref}$ . Therefore, the voltage at the output of the differential amplifier is:  $V_A = V_{in} - V_D = 1.5V_{ref}$ . In this situation, the integrator integrates up and as soon as the output voltage of the integrator exceeds  $0V$ , the output of the comparator switches to 1. Therefore, the DAC output switches from  $-V_{ref}$  to  $+V_{ref}$  and the output of the differential amplifier becomes:  $V_A = V_{in} - V_D = -0.5V_{ref}$ . The integrator-input voltage is therefore negative and the integrator now integrates down.

## Noise Shaping



The analog modulator represents a low pass filter for the analog input signal and a high pass filter for the quantization noise.

2-57

## Noise Shaping

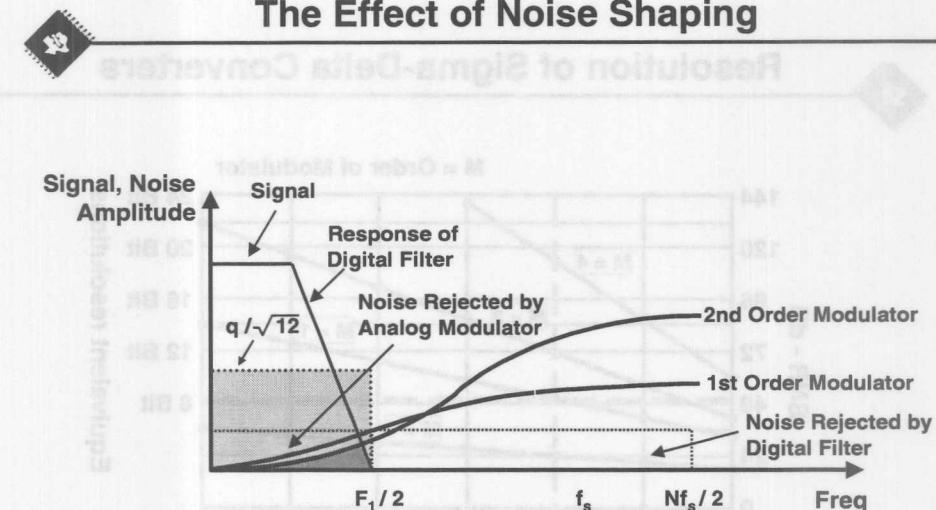
The modulator also shapes the quantization noise within the signal frequency band. This has the effect of pushing a significant percentage of the quantization noise out of the band of interest where it can be filtered by the digital filter. This effect can be derived mathematically. As visible in the picture of the analog modulator loop, the comparator is simplified to a quantization noise source. Therefore, the response of the analog modulator can be written as:

$$V_{OUT} = V_{NOISE} + \frac{1}{j\omega} \times (V_{IN} - V_{OUT}), \text{ or}$$

$$V_{OUT} = \frac{V_{NOISE}}{1 + \frac{1}{j\omega}} + \frac{V_{IN}}{1 + j\omega}$$

The analog modulator represents a low pass filter for the analog input signal and a high pass filter for the quantization noise.

## The Effect of Noise Shaping



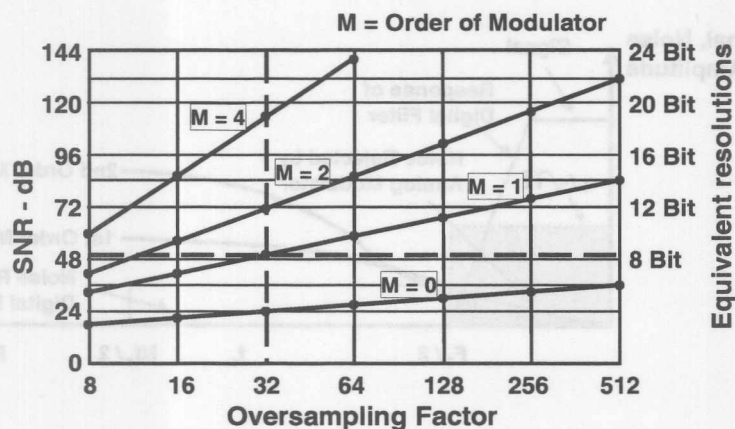
2-58

## The Effect of Noise Shaping

The number of integrators, which are included, determines the order of the modulator. The higher the order of the modulator the greater the amount of quantization noise which is pushed out of band. Higher order analog modulators enable increased resolution converters offering enhanced signal to noise ratios to be produced, without the need to increase the oversampling rate. The effect of noise shaping produced by 1st and 2nd order modulators can be seen in the figure above.

The idea of increasing the order of the modulator to a high number sufficient to achieve any desired resolution and SNR is an attractive one. Unfortunately there is rarely gain without some pain. Higher order modulators tend to be more difficult to stabilize. Most sigma-delta converters tend to use modulators, which are 5th order or less.

## Resolution of Sigma-Delta Converters



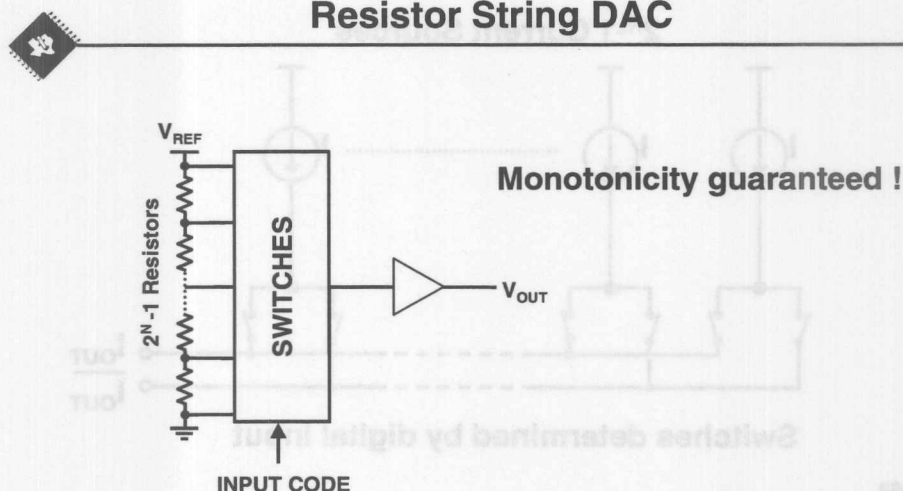
2-59

### Resolution of Sigma-Delta Converters

The graphic shows the performance of a Sigma-Delta converter in terms of resolution depending on the oversampling factor and the order of the modulator. As an example, a Sigma-Delta converter with a first order modulator is considered. The SNR is about 50 dB, which equivalent to an ADC with a resolution of 8 bit. A move from the first order modulator to a second order modulator increases the SNR to about 70 dB, which is then equivalent to approximately 11 to 12 bits of resolution. In addition, the higher the oversampling the higher the resolution.

## D/A Converters

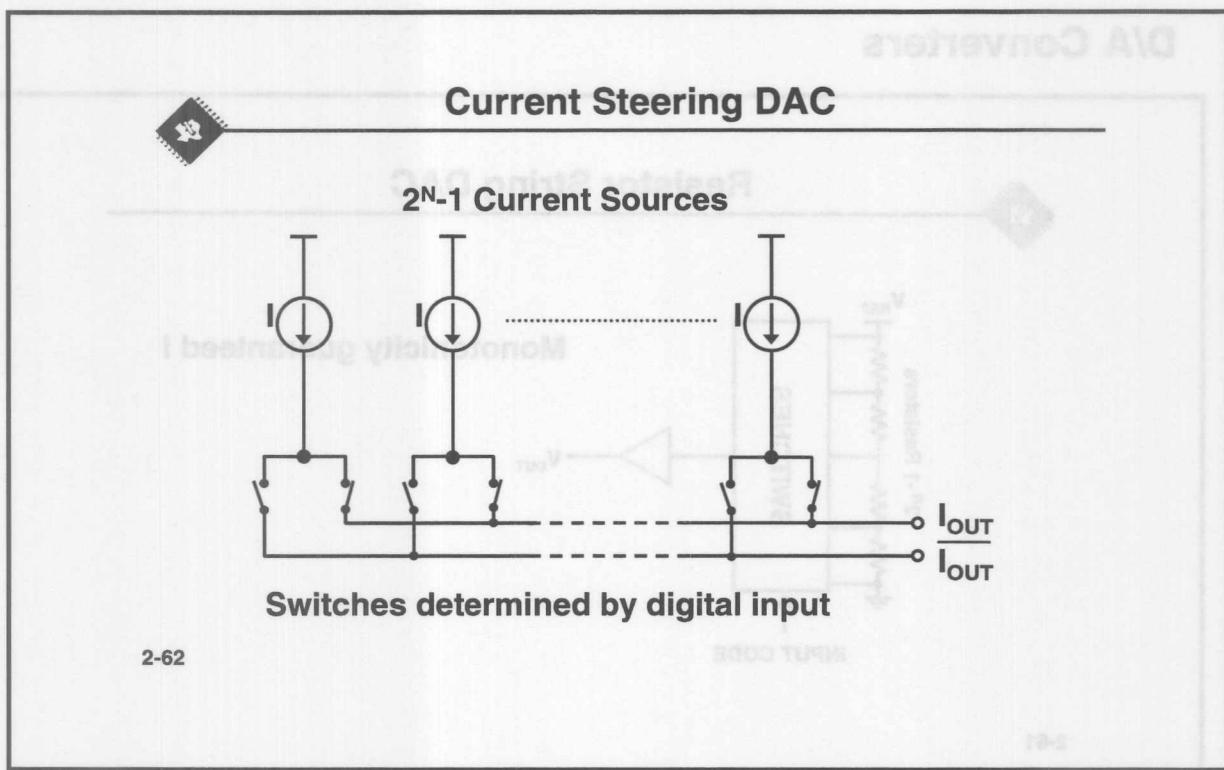
### Resistor String DAC



2-61

### Resistor String DACs

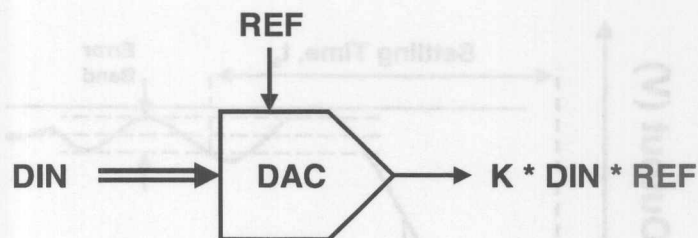
In a Resistor String architecture, the reference voltage is divided into  $2^N - 1$  parts, each exactly one LSB high. A network of switches selects the output voltage from the resistor string, depending on the digital input code. To avoid errors due to a load current, a buffer is required on the DAC output. This buffer is usually part of the DAC. The big advantages of this architecture are, that the transfer function is always monotonic and that the design is relatively simple. The disadvantages are, that  $2^N - 1$  matching resistors are required, which limit the achievable resolution and that this architecture needs an amplifier (buffer), which limits the achievable speed.



### Current Steering DAC

A Current Steering DAC is based on switched current sources. It has two current outputs, with one providing the complementary current of the other. The sum of the output currents is always constant. An array of switches, which is controlled by the digital input, directs the current of the sources to one of the two output rails. Like the resistor string architecture, current steering also guarantees monotonicity. And it allows much higher speeds, than designs with voltage outputs.

## Multiplying DACs



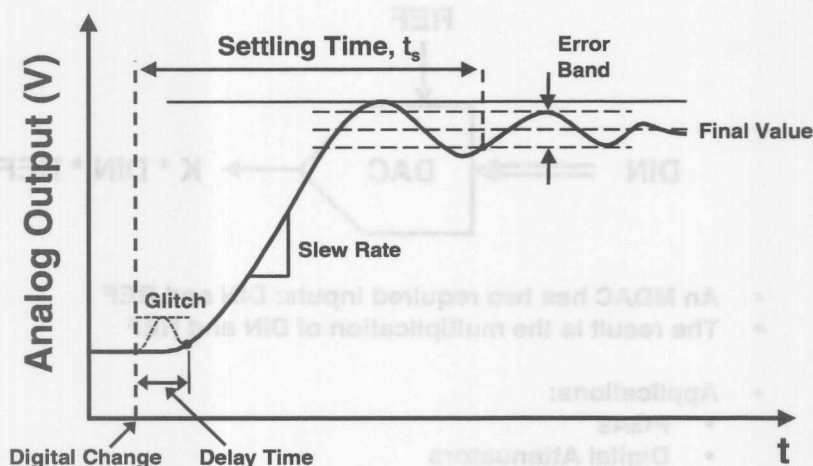
- An MDAC has two required inputs: DIN and REF
- The result is the multiplication of DIN and REF
- Applications:
  - PGAs
  - Digital Attenuators

2-63

## Multiplying DACs

Besides the input for the digital data, a multiplying DAC always has a dedicated input for the reference. Unlike non-multiplying DACs, which allow only a narrow band for the reference, MDACs are intended to handle signals over a specified voltage and frequency range on the reference input. The output of the MDAC is equal to the multiplication of the signal on the reference input and the input code. Depending on the reference voltage range and the input code range, the MDAC operates in specific quadrants. If both the reference and the digital input can have negative and positive values, then the MDAC operates in all four quadrants.

### Settling time of a DAC

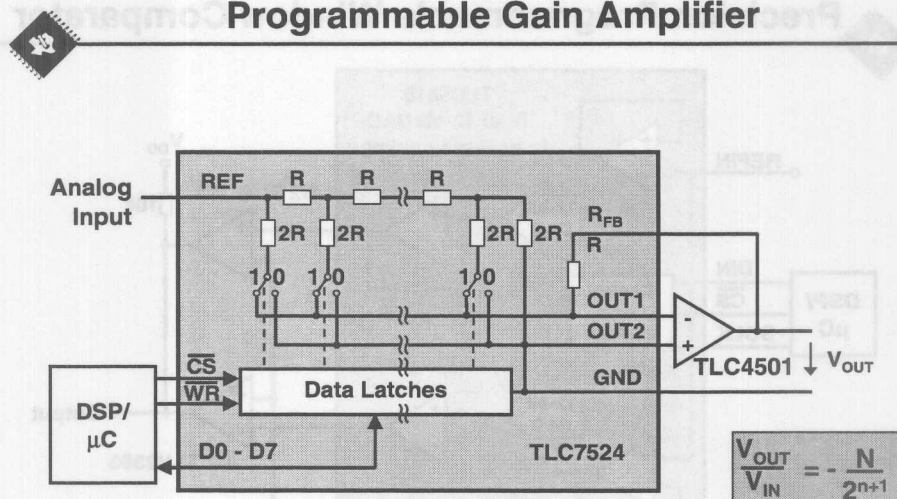


2-64

### Settling Time of a D/A Converter

The settling time of a D/A-converter is the time between the switching of the digital inputs of the converter and the time when the output reaches its final value and remains within a specified error band. The settling time is a very important parameter, because this must be faster than the signal frequency in order to be able to reconstruct the waveform. The picture shows also a possible glitch in the waveform of a DAC. This glitch is an undesirable transient in the analog output occurring following a code change at the digital input. If a current output DAC is used with an external amplifier, then a ferrite bead can be used to minimize the glitch by minimizing the switching current.

## Programmable Gain Amplifier



2-65

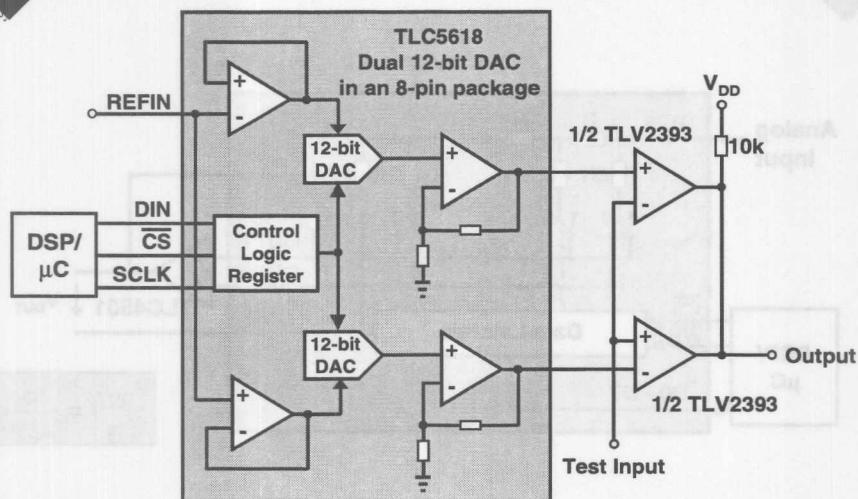
## Programmable Gain Amplifier

A D/A-converter can be used to build up a Programmable Gain Amplifier (PGA). The advantages are that multiple gain levels with high accuracy can be selected via software. The DAC can be seen as a programmable resistance. The picture shows the configuration of a PGA by using the 8 bit DAC TLC7524. The internal resistor  $R_{FB}$  is used as a feedback resistor for the external op amp. The analog input voltage is applied to the REF input of the DAC. The input impedance  $R_I$  of a DAC in R-2R technology is always  $2R$ . The feedback resistor  $R_{FB}$  of the TLC7524 is  $R$  ( $R_I = 2R_{FB}$ ) and therefore the transfer function results into:

$$\frac{V_{out}}{V_{in}} = -\frac{N \times R_{FB}}{2^n \times R_I} = -\frac{N}{2^{n+1}}$$

$N$  in this equation is the decimal input code of the DAC and  $n$  is the resolution of the DAC.

## Precision Programmable Window Comparator



2-66

## Precision Programmable Window Comparator

The figure shows a precision programmable window comparator, which uses a 12-bit dual D/A-converter TLC5618, and a dual open collector comparator TLV2393. The threshold voltages of the comparators are programmed via the D/A-converter. 1 LSB of the TLC5618 corresponds to 1 mV with a reference voltage of 2.048 V and a gain of 2. The input offset voltage of the comparator in this case limits the accuracy of the system.

**Low Power DAC Families**
**TI's New Low Power DAC Family**
**New TLC/TLV56xx 10-Bit Family**

| Device   | No. of DACs | Settling Time      | Clock Rate | Power Dissipation | Internal Voltage Ref. | Serial/Parallel Interface |
|----------|-------------|--------------------|------------|-------------------|-----------------------|---------------------------|
| TLC5615  | 1           | 12.5 $\mu$ s       | 14 MHz     | 1.15 mW           | No                    | serial                    |
| TLC5617A | 2           | 12.5 / 2.5 $\mu$ s | 20 MHz     | 3 / 8 mW          | No                    | serial                    |
| TLV5604  | 4           | 12/3 $\mu$ s       | 20 MHz     | 3 / 8 mW          | No                    | serial                    |
| TLV5637* | 2           | 3 / 1 $\mu$ s      | 20 MHz     | TBD / TBD mW      | Yes                   | serial                    |

**New TLC/TLV56xx 12-Bit Family**

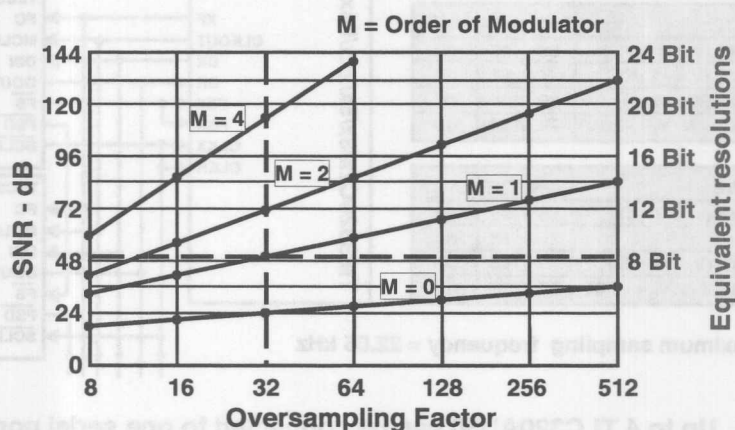
| Device   | No. of DACs | Settling Time      | Clock Rate | Power Dissipation | Internal Voltage Ref. | Serial/Parallel Interface |
|----------|-------------|--------------------|------------|-------------------|-----------------------|---------------------------|
| TLV5616  | 1           | 8.2 / 2.5 $\mu$ s  | 20 MHz     | 0.6 / 1.7 mW      | No                    | serial                    |
| TLV5613  | 1           | 3 / 1 $\mu$ s      | ---        | 1.2 / 4.2 mW      | No                    | parallel                  |
| TLV5619  | 1           | 1 $\mu$ s          | ---        | 4.2 mW            | No                    | parallel                  |
| TLC5618A | 2           | 12.5 / 2.5 $\mu$ s | 20 MHz     | 3 / 8 mW          | No                    | serial                    |
| TLV5614  | 4           | 12/ 3 $\mu$ s      | 20 MHz     | 3 / 8 mW          | No                    | serial                    |
| TLV5636* | 1           | 3 / 1 $\mu$ s      | 20 MHz     | TBD / TBD mW      | Yes                   | serial                    |
| TLV5638* | 2           | 3 / 1 $\mu$ s      | 20 MHz     | TBD / TBD mW      | Yes                   | serial                    |
| TLV5633* | 1           | 3 / 1 $\mu$ s      | ---        | 10 / 20 mW        | Yes                   | 8+4 bit parallel          |
| TLV5639* | 1           | 3 / 1 $\mu$ s      | ---        | 10 / 20 mW        | Yes                   | 12 bit parallel           |

**2-67**
**\* Product Preview Only**

## Selection Guide: D/A Converters

| Video and High Speed DACs          |      |   |   |   |     |       |       |      |      |
|------------------------------------|------|---|---|---|-----|-------|-------|------|------|
| 8-bit Digital-to-Analog Converters |      |   |   |   |     |       |       |      |      |
| TLC5602                            | ±0.2 | P | V | 1 | EXT | 30ns  | 5     | 20   | 125  |
| TL5632                             | ±0.5 | P | V | 3 | INT | 15ns  | 5     | 60   | 450  |
| Video and High Speed DACs          |      |   |   |   |     |       |       |      |      |
| 8-bit Digital-to-Analog Converters |      |   |   |   |     |       |       |      |      |
| TLC5620                            | ±1.0 | S | V | 4 | EXT | 10μs  | 5     | 0.1  | 10   |
| TLC5628                            | ±1.0 | S | V | 8 | EXT | 10μs  | 5     | 0.1  | 20   |
| TLC7225                            | ±1.0 | P | V | 4 | INT | 5μs   | 5-15  | 0.05 | 60   |
| TLC7226                            | ±1.0 | P | V | 4 | EXT | 5μs   | 5-15  | 0.05 | 60   |
| TLC7524                            | ±0.5 | P | I | 1 | EXT | 0.1μs | 5-15  | 10   | 5    |
| TLC7528                            | ±0.5 | P | I | 2 | EXT | 0.1μs | 5-15  | 10   | 5    |
| TLC7628                            | ±0.5 | P | I | 2 | EXT | 0.1μs | 10-15 | 10   | 20   |
| TLV5620                            | ±1.0 | S | V | 4 | EXT | 10μs  | 3     | 0.1  | 6.6  |
| TLV5621                            | ±1.0 | S | V | 4 | EXT | 10μs  | 3     | 0.1  | 4.5  |
| TLV5628                            | ±1.0 | S | V | 8 | EXT | 10μs  | 3     | 0.1  | 13.2 |

## Resolution of Sigma-Delta Converters



2-59

## Analog Interface Circuits for DSP

### Analog Interface for DSP

Digital signal processing (DSP) techniques are today being used in a whole range of industrial and consumer products. The advantages of accuracy and repeatability of digital approaches are being utilized in functions ranging from multi-tap filters in communications systems through to precision motor control.

A fundamental requirement which remains necessary, in order to exploit DSP methods, is the conversion of signals from analog into digital and digital into analog form, and the rapid transfer of these conversion results in and out of the DSP. It is important that bottlenecks are avoided in the flow of data between the real world and the computational heart of the DSP. The Analog Interface Circuit (AIC) is a class of mixed-signal products which includes the necessary analog circuit blocks and an optimized interconnection scheme to facilitate the rapid and efficient transfer of information between the analog and digital domains.

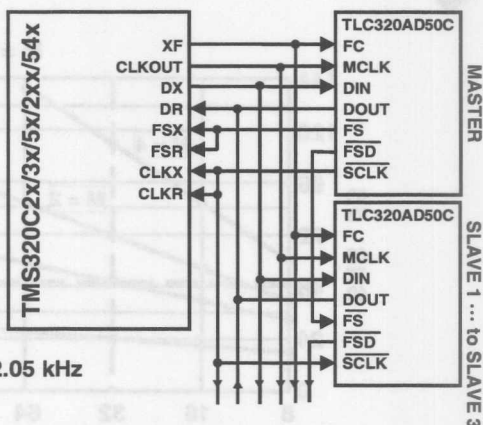
Texas Instruments offers today a growing family of analog interface circuit products. These consist always of A/D and D/A converters generally in sigma-delta technology. The sampling frequency of these circuits is in the range of in voice- and audio applications. The next page gives an overview of the today's available components.

# DSP Interface with 16-Bit AIC TLC320AD50

| ADC                      | MIN | TYP | UNIT |
|--------------------------|-----|-----|------|
| SNR ( $V_i = -1$ dB)     | 85  | 89  | dB   |
| DNR ( $V_i = -1$ dB)     |     | 88  | dB   |
| THD ( $V_i = -3$ dB)     | 80  | 85  | dB   |
| THD + N ( $V_i = -3$ dB) | 78  | 82  | dB   |

| DAC                      | MIN | TYP | UNIT |
|--------------------------|-----|-----|------|
| SNR ( $V_o = 0$ dB)      | 85  | 89  | dB   |
| DNR                      |     | 88  | dB   |
| THD ( $V_o = -3$ dB)     | 76  | 80  | dB   |
| THD + N ( $V_o = -3$ dB) | 75  | 79  | dB   |

maximum sampling frequency = 22.05 kHz



Up to 4 TLC320AD50 can be connected to one serial port !

2-70

## TLC320AD50

The TLC320AD50 is the latest analog interface circuit. The chip consists of sigma-delta A/D and D/A converters with a maximum sampling frequency of 22.05 kHz. The typical performance of the TLC320AD50 is listed in the picture.

In many applications it is important to connect more than one component to a DSP. By using the TLC320AD50 it is possible to connect up to 4 devices on one serial port of a DSP. In this case, one TLC320AD50 operates as the Master which generates the synchronization signal for the digital signal processor (DSP) and the slaves. The slave receives the synchronization signal from the master device. This configuration is shown in the picture. This master-slave technique makes a stereo or multi-channel application easy.

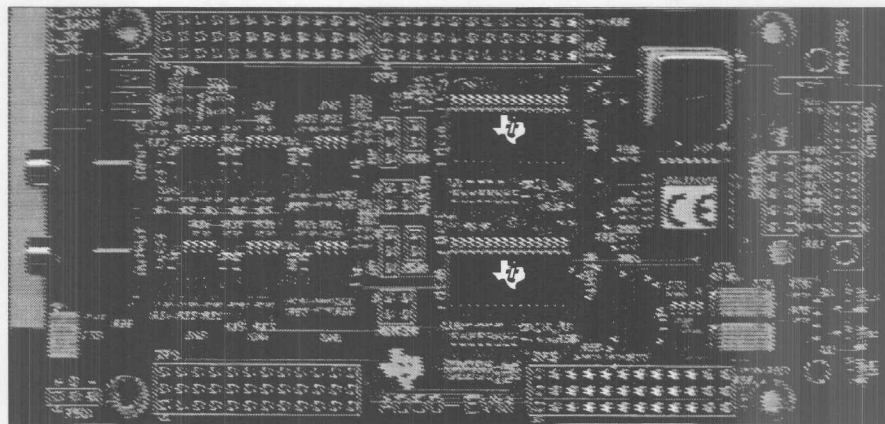
*SNR = Signal to Noise Ratio*

*DNR = Dynamic Range*

*THD = Total Harmonic Distortion*

*THD+N = Total Harmonic Distortion plus Noise*

## TLC320AD50 Evaluation Board



2-71

### TLC320AD50 Evaluation Board (AD50-EVM)

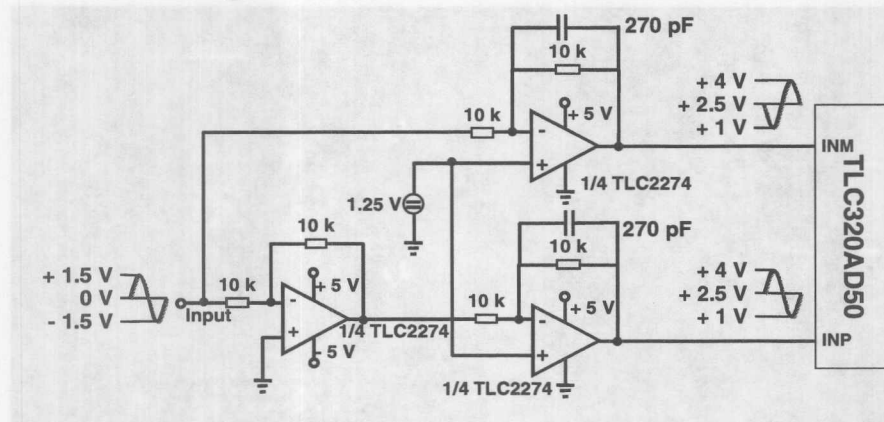
The AD50-EVM has two AD50 devices for stereo operation. Two AD50-EVMs can be configured as a four-channel system using a single serial interface.

The objective was to design a development board (the AD50-EVM) which would allow prospective users of the AD50 to determine its capabilities with a minimum of effort. The AD50-EVM can be directly connected to the low cost TMS320C54x DSP Starter Kit (DSK+), or to any other system with a compatible synchronous serial interface. Directly compatible DSP devices include TMS320C2x, C2xx, C3x, C5x, C54x and C6xxx.

A demonstration program is provided for the DSK+ development system, which allows the board to be used as a sine-wave generator, or to output samples read in from the ADC onto the DAC. In this echo mode, signal-processing functions such as filtering can easily be included. The AD50-EVM board was also interfaced to a TMS320C25 development board, which was used to transfer analog data to a personal computer running real-time FFT spectrum analysis software. This system was used to prepare the ADC and DAC FFT spectrograms shown in this seminar.

## TLC320AD50 Input Stage Design

### - Single Ended to Differential Converter -



2-72

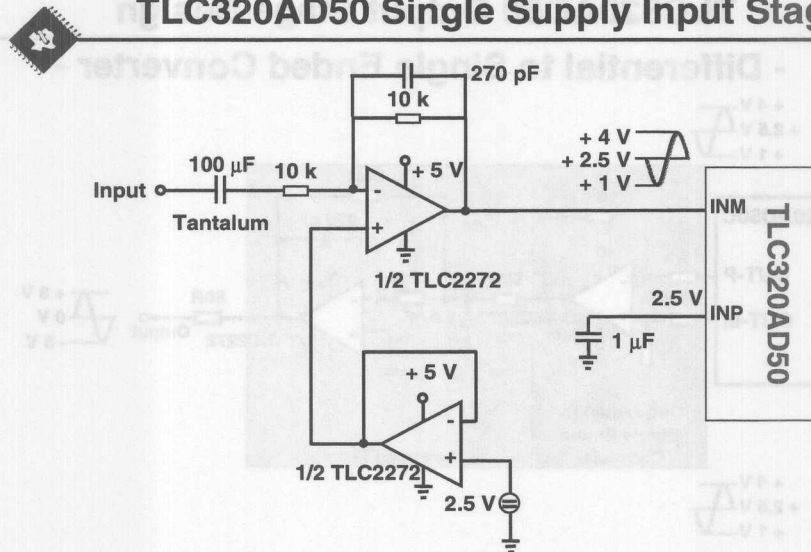
## TLC320AD50 Input Stage Design, Single Ended to Differential Converter

The A/D converter of the TLC320AD50 features a differential input structure. Therefore, a single ended input signal should always be converted to a differential input signal prior to being used by the TLC320AD50 to achieve the best possible performance. The differential inputs are biased at 2.5 V. A maximum code is generated with a 3 V<sub>PP</sub> signal on both differential inputs. The circuit diagram shows such a single ended to differential converter, where the first op amp inverts the incoming signal to provide a differential signal. The second op amp performs the necessary level shifting. The noninverting inputs of these op amps are biased with 1.25 V, which results in an output voltage range from 1 V up to 4 V with an input voltage range from -1.5 V to 1.5 V. The first op amp needs a bipolar voltage supply because of the bipolar input voltage range; the second needs only a single supply.

The bias voltage of 1.25 V is derived with a resistive divider on the AD50-EVM.

To obtain the same gain for both differential channels it is recommended a resistor network array be used to achieve a very high accuracy in each of the resistors.

### TLC320AD50 Single Supply Input Stage



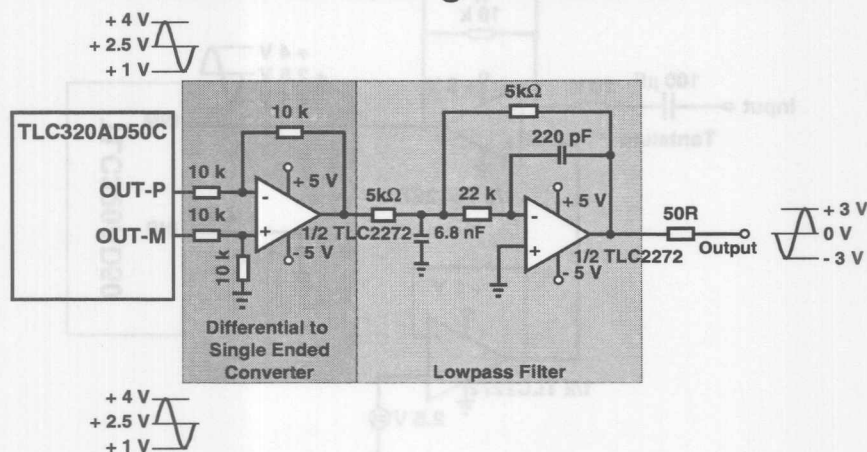
2-73

### TLC320AD50 Single Supply Input Stage

In this example of an input stage design, only a single supply is required. The input signal is ac coupled by the 100  $\mu\text{F}$  coupling capacitor and is level shifted to 2.5 V by half the op amp. The other half of the op amp provides a buffered 2.5 V supply. However, beside the advantages of a simple circuit and only a single supply, this proposal has also some disadvantages. The input must be ac coupled in order to allow the required level shifting. Furthermore, the TLC320AD50 has differential inputs, which are designed to provide immunity from noise and interference. To take advantage of this feature it is necessary to ensure that any noise at the reference point appears equally on both differential inputs. In this circuit, the INP input sees the noise directly whilst the INM input sees the noise amplified by 2. In addition to this, this input stage can only produce 50% of the differential voltage needed for maximum input. This effectively reduces the signal to noise ratio and dynamic range by 6 dB.

## TLC320AD50 Output Stage Design

### - Differential to Single Ended Converter -

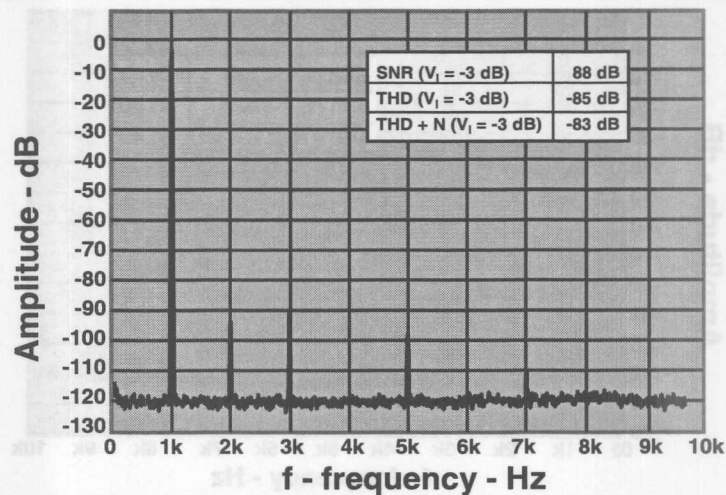


2-74

### TLC320AD50 Output Stage Design, Differential to Single Ended Converter

- The D/A converter of the TLC320AD50 uses a pair of differential voltage outputs.
- The output needs to convert the differential signals to a single ended output, and to attenuate noise outside the pass-band. This filter is not a conventional reconstruction filter, since the AD50 has an integral low-pass reconstruction filter. This filter is a 12 kHz second order low-pass filter designed for use at 20 ksp/s and will be less effective at lower sampling rates. Since this filter only removes out of band noise it will be unnecessary in many applications.

# AD50-EVM ADC Distortion Measurement

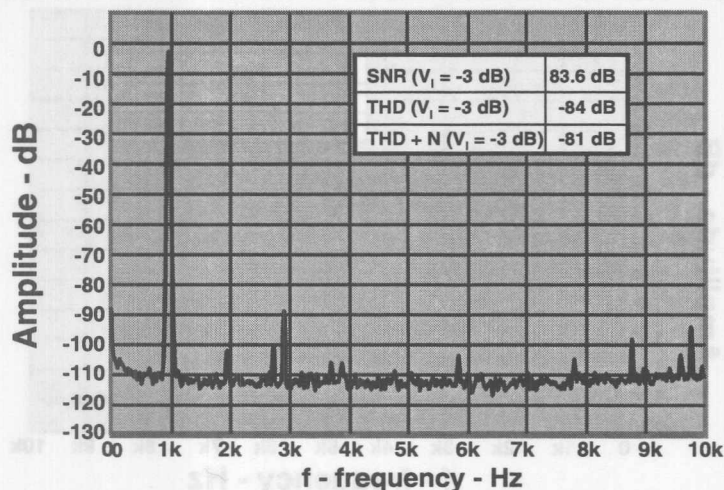


Input signal: 1 kHz, -3 dB --- FFT: 20ksps, 4096 freq bins, 5 averages

## AD50-EVM ADC Distortion Measurement

To evaluate the performance of the ADC channel of the AD50-EVM, FFT measurements were performed. The input signal was a 1 kHz sinewave at -3 dB relative to maximum input. An audio analyzer (UPD, Rohde & Schwarz) was used to produce the test signal and to perform the FFT. By adding up the energy in each frequency bin within (a) the signal, (b) the harmonics and (c) the rest of the noise floor, figures for SNR, THD and THD+N can be calculated. The figures were 88 dB SNR, 85 dB THD and 83 dB THD+N.

### AD50-EVM DAC Distortion Measurement



2-76

Input signal: 967 Hz, -3 dB --- FFT: 20ksps, 4096 freq bins, 5 averages

### AD50-EVM DAC Distortion Measurement

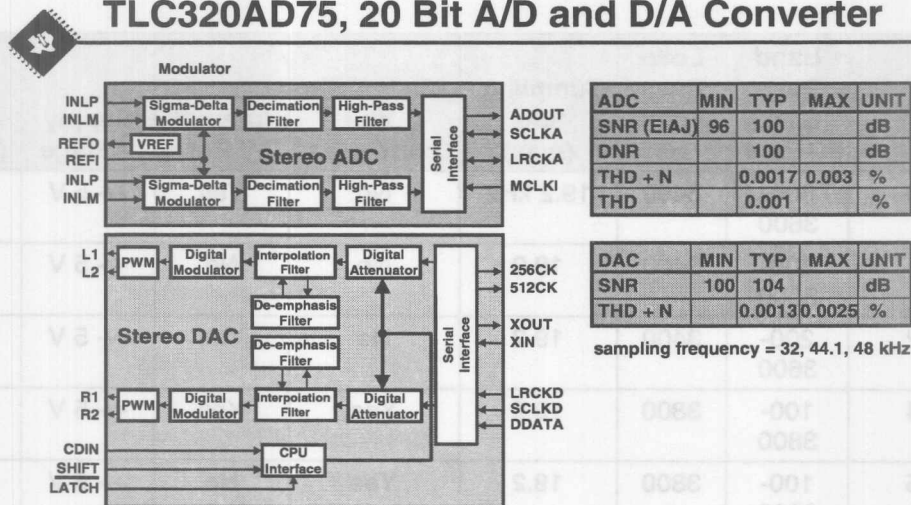
The DAC was measured in 16 bit mode using a sine-wave table lookup program running on a TMS320C54x DSK+ coupled to an AD50-EVM. The picture shows an FFT plot of the output from the AD50-EVM. This was measured using a Rohde & Schwarz audio analyzer (UPD). The SNR was 83.6 dB, the THD was 84 dB and the THD+N was 81 dB.

**Selection Guide: Analog Interface Circuits**

| Part Number | Band Pass Filter Hz | Low-Pass Filter Hz | Sampling Rate (max) | Sin x/x correction | Internal V Ref | Supply Voltage | PD (mW) | Ma / SL |
|-------------|---------------------|--------------------|---------------------|--------------------|----------------|----------------|---------|---------|
| TLC32040    | 300-3600            | 3400               | 19.2 kHz            | No                 | Yes            | +/- 5 V        | 430     | M       |
| TLC32041    | 300-3600            | 3400               | 19.2                | No                 | No             | +/- 5 V        | 430     | M       |
| TLC32042    | 200-3600            | 3400               | 19.2                | No                 | Yes            | +/- 5 V        | 430     | M       |
| TLC32044    | 100-3800            | 3800               | 19.2                | Yes                | Yes            | +/- 5 V        | 430     | M       |
| TLC32045    | 100-3800            | 3800               | 19.2                | Yes                | No             | +/- 5 V        | 430     | M       |
| TLC32046    | 300-7200            | 7200               | 25                  | Yes                | Yes            | +/- 5 V        | 430     | M       |
| TLC32047    | 300-11.4 k          | 11.4 k             | 25                  | Yes                | Yes            | +/- 5 V        | 430     | M       |
| TLC320AC01  | up to 10.8 k        | 10.8 k             | 25                  | Yes                | Yes            | + 5 V          | 110     | M/S     |
| TLC320AC02  | up to 10.8 k        | 10.8 k             | 25                  | Yes                | Yes            | + 5 V          | 110     | M       |
| TLC320AD50  | up to 8.82 k        | 8.82 k             | 22.05               | Yes                | Yes            | + 5 V/+3V      | 100     | M/S     |
| TLC320AD55  | up to 4.41 k        | 4.41k              | 11.025              | Yes                | Yes            | + 5 V          | 150     | M       |
| TLC320AD56  | up to 8.82 k        | 8.82 k             | 22.05               | Yes                | Yes            | + 5 V/+3V      | 100     | M       |

## Audio Converters

### TLC320AD75, 20 Bit A/D and D/A Converter



2-79

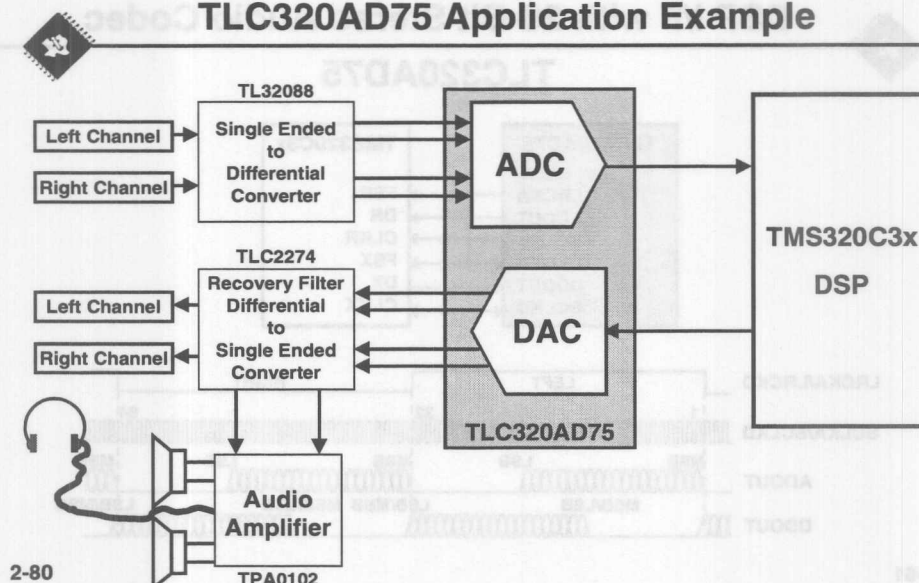
### TLC320AD75, 20 Bit A/D and D/A Converter

The TLC320AD75C is a high-performance stereo 20-bit analog-to-digital and digital-to-analog converter (ADA) using sigma-delta technology to provide four concurrent 20-bit resolution conversions from both analog-to-digital (A/D) and digital-to-analog (D/A) signal paths. Additional functions provided are digital attenuation, digital de-emphasis filtering, soft mute, and on-chip timing and control. Control words from a host controller or processor are used to implement these functions.

#### The main features are:

- Single 5-V (Analog/Digital) Power Level and 3.3-V to 5-V Digital Interface Level
- Sample Rates up to 48 kHz
- 20-Bit Resolution Conversions
- Internal Voltage Reference (V ref )
- Serial Port Interface
- Differential Architecture
- DAC Provides PWM Output
- Digital De-emphasis Filtering for 32-, 44.1-, and 48-kHz Sample Rates for the DAC
- Digital Attenuation/Soft Mute Function for the DAC

### TLC320AD75 Application Example



### TLC320AD75 Application Example

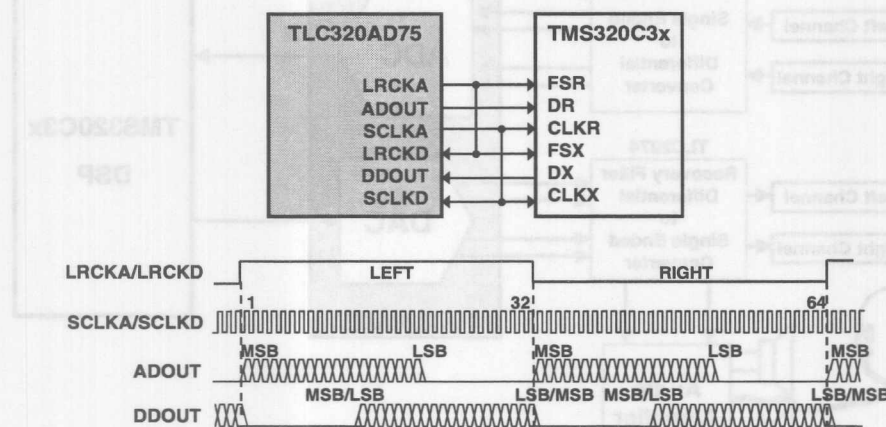
The picture shows an application example with the TLC320AD75, which was used to convert analog audio data into digital format. The TMS320C3x is here used to read out the ADC digital data and to transmit digital data to the DAC which then can be converted into analog domain again. The DSP is here used to manipulate the digital data (echo cancellation, echo generation, filtering, equalizer function, etc.). On the analog output, an audio amplifier can be used to connect passive speakers or a headphone.

LROKA is generated internally from MCLK. The frequency of LROKA is fixed at the sampling frequency  $f_s$  (MCLK/256). During the high period of LROKA, the left channel data is serially shifted to the output; during the low period, the right channel data is shifted to the output (ADOUT). The conversion cycle is synchronized with the rising edge of LROKA.

For the DAC, the conversion cycle is synchronized to the rising edge of LROKA, and the data must meet the setup requirements specified in the timing requirements. The input data is 16 or 20 bits with the MSB or LSB first as selected in the system register. The recommended SCLK frequency is  $64 \times f_s$ . The picture illustrates the input and output timing for ADC and DAC.

# DSP I/F with 20-Bit Stereo Audio Codec

## TLC320AD75



2-81

### Interface of the TLC320AD75 to the TMS320C3x

- The picture shows the glueless interface of the TLC320AD75 to the Texas Instruments digital signal processor TMS320C3x. To achieve this, the serial port of the DSP is configured in the variable mode. When the TLC320AD75 is configured as the master device (M\_S is connected to  $V_{DD1}$ ), the TLC320AD75C generates LRCKA and SCLKA from MCLKI. These signals are provided for synchronizing the serial port of a digital signal processor (DSP) or other control devices.

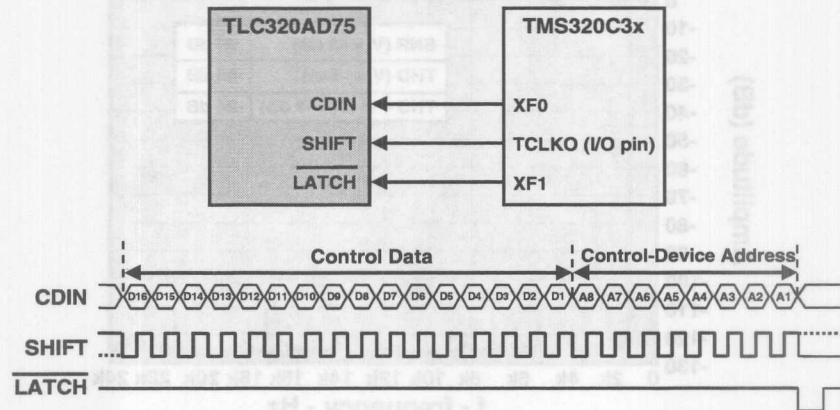
LRCKA is generated internally from MCLKI. The frequency of LRCKA is fixed at the sampling frequency,  $f_s$  ( $MCLKI/256$ ). During the high period of LRCKA, the left channel data is serially shifted to the output; during the low period, the right channel data is shifted to the output (ADOUT). The conversion cycle is synchronized with the rising edge of LRCKA.

For the DAC, the conversion cycle is synchronized to the rising edge of LRCKD, and the data must meet the setup requirements specified in the timing requirements. The input data is 16 or 20 bits with the MSB or LSB first as selected in the system register. The recommended SCLKD frequency is  $64 \times f_s$ . The picture illustrates the input and output timing for ADC and DAC.



## Glueless Control Interface to the TMS320C3x

The Attenuation Mode Register and the System Mode Register are programmed via the control interface.



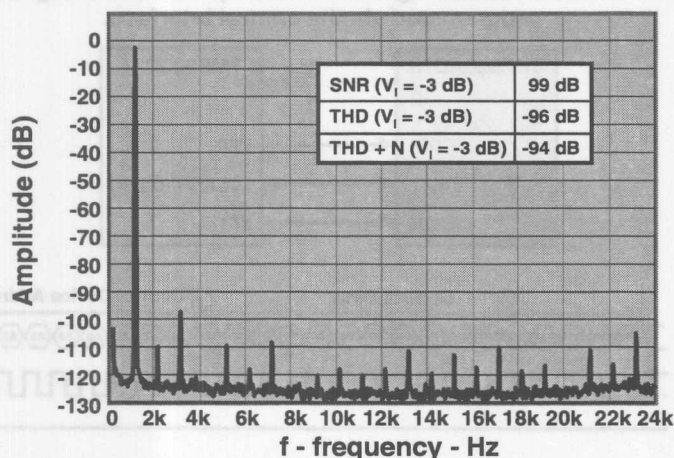
2-82

## Glueless Control Interface to the DSP TMS320C3x

- The TLC320AD75 has two internal registers, which are used to program the mode of the converter chip. These registers are accessible via a further interface.
- Also this interface can be built up glueless. It consists of three signals, SHIFT, CDIN and Latch. SHIFT is the clock signal of the interface. CDIN is the data information which has to be sent to the AD75. The LATCH input is used for latching the data information into the selected register of the device. The SHIFT signal is here generated with the timer pin TCLK0. The data bits are generated with the XF0 pin and the data is latched with the XF1 pin of the DSP.

## 2 Layer AD75-Board ADC Distortion

### Measurement



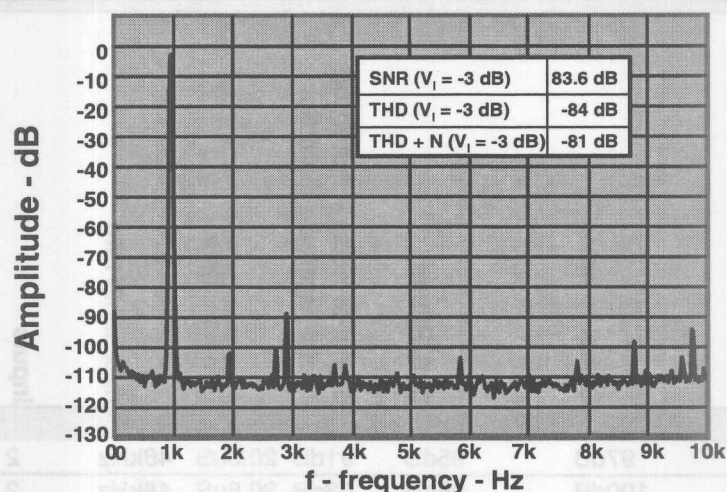
2-83

Input signal: 1 kHz, -3 dB - - - FFT: 48ksps, 4096 freq bins, 5 averages

### 2 Layer AD75-Board ADC Distortion Measurement

To evaluate the performance of the ADC channel of the 2-layer board of the TLC320AD75, FFT measurements were performed. The input signal was a 1 kHz sine wave at -3 dB relative to maximum input. An audio analyzer (UPD, Rohde & Schwarz) was used to produce the test signal and to perform the FFT. By adding up the energy in each frequency bin within (a) the signal, (b) the harmonics and (c) the rest of the noise floor, figures for SNR, THD and THD+N can be calculated. The figures were 99 dB SNR, 96 dB THD and 94 dB THD+N.

## AD50-EVM DAC Distortion Measurement



2-76

Input signal: 967 Hz, -3 dB --- FFT: 20ksps, 4096 freq bins, 5 averages

## 2 Layer AD75-Board DAC Distortion Measurement

To evaluate the performance of the DAC channel of the 2-layer board of the TLC320AD75, FFT measurements were performed. The input signal was a 1 kHz sine wave at -3 dB relative to maximum input, which was generated by an audio analyzer (UPD, Rohde & Schwarz). This analyzer was also used to perform the FFT. By adding up the energy in each frequency bin within (a) the signal, (b) the harmonics and (c) the rest of the noise floor, figures for SNR, THD and THD+N can be calculated. The figures were 106 dB SNR, 95 dB THD and 94 dB THD+N.

## Selection Guide: Audio Converters

| Stereo Audio ADCs                                                                                    |            |                          |            |                                                          |               |               |                |              |                |           |
|------------------------------------------------------------------------------------------------------|------------|--------------------------|------------|----------------------------------------------------------|---------------|---------------|----------------|--------------|----------------|-----------|
|                                                                                                      | Resolution | Signal-to-noise          | Dyn. Range | Signal-to-noise + distortion / Total harmonic distortion | Convers. time | max samp rate | inputs         | internal ref | Suppl. Voltage | Interface |
| Stereo Audio ADCs                                                                                    |            |                          |            |                                                          |               |               |                |              |                |           |
| TLC320AD57C                                                                                          | 2 x 18-bit | 97dB                     | 95dB       | 91dB                                                     | 20.8uS        | 48kHz         | 2              | Y            | 5V             | serial    |
| TLC320AD58C                                                                                          | 2 x 18-bit | 100dB                    | 95dB       | 93dB                                                     | 20.8uS        | 48kHz         | 2              | Y            | 5V             | serial    |
| Stereo Audio ADC/DAC                                                                                 |            |                          |            |                                                          |               |               |                |              |                |           |
| TLC320AD75C                                                                                          | 2 x 20-bit | 100dB(ADC)<br>104dB(DAC) | 100dB(ADC) | 0.003%                                                   | 20.8uS        | 48kHz         | 2 + 2          | Y            | 5 / 3.3-5V     | serial    |
| AC '97 Multimedia Audio Codec with Volume control, Mixer, Mux, Plug & Play                           |            |                          |            |                                                          |               |               |                |              |                |           |
| TLC320AD91                                                                                           | 2 x 18-bit | 80dB(ADC)<br>90dB(DAC)   |            |                                                          | 20.8uS        | 48 kHz        | 4 +<br>(4 x 2) | Y            | 3.3 - 5V       | serial    |
| Set Top Box Stereo DAC with digital & analog input mux, Volume/Balance control, wideband analog Mux, |            |                          |            |                                                          |               |               |                |              |                |           |
| TLC320AD80                                                                                           | 2 x 16-bit | 85dB                     |            | 0.02%                                                    |               | 48kHz         | 9              | Y            | 5V             | serial    |

## Data Converter Application Reports

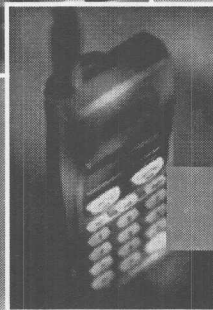
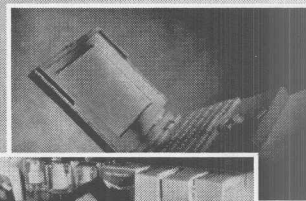
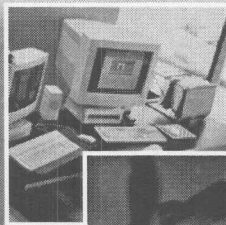
|                                                                                 |          |
|---------------------------------------------------------------------------------|----------|
| Interfacing the TLV1544/TLV1548 ADC to Digital Processors                       | SLAA022  |
| Interfacing the TLC5540 ADC to the TMS320C203-80 DSP                            | SLAA032  |
| Interfacing the TLC5510 ADC to the TMS320C203 DSP                               | SLAA029  |
| Interfacing ADCs TLC5540/10 to the DSKPLUS DSP Starter Kit TMS320C54X           | SLAAE14  |
| Interfacing the TLV1572 ADC to the TMS320C203 DSP                               | SLAA026A |
| Interfacing the TLV1544 ADC to the TMS320C50 DSP                                | SLAA025  |
| Interfacing the TLV1544 ADC to the TMS320C203 DSP                               | SLAA028  |
| Minimizing Input Design Problems with the TLV5590                               | SWCA001  |
| Interfacing the TLV1549 10-Bit Serial-Out ADC to Popular 3.3-V Microcontrollers | SLAA005  |
| Microcontroller Based Data Acquisition Using the TLC2543 12-Bit Serial Out ADC  | SLAA012  |
| Interfacing the TLC2543 ADC to the TMS320C25 DSP                                | SLAA017  |
| Signal Acquisition and Conditioning with Low Supply Voltages                    | SLAA018  |
| Understanding Data Converters                                                   | SLAA013  |
| TLC320AD57C Sigma-Delta Stereo Analog-to-Digital Converters                     | SLAA010  |
| TLC320AD58C Sigma-Delta Stereo Analog-to-Digital Converter                      | SLAA015  |
| TLC2932: PLL Building Block with Analog VCO & Phase Frequency Detector          | SLAA011B |

This is a representative sample and was accurate when this workbook was printed. For a complete up to date listing of application reports, designer note pages and EVMs please check the TI web site.

# Data Converter Application Reports

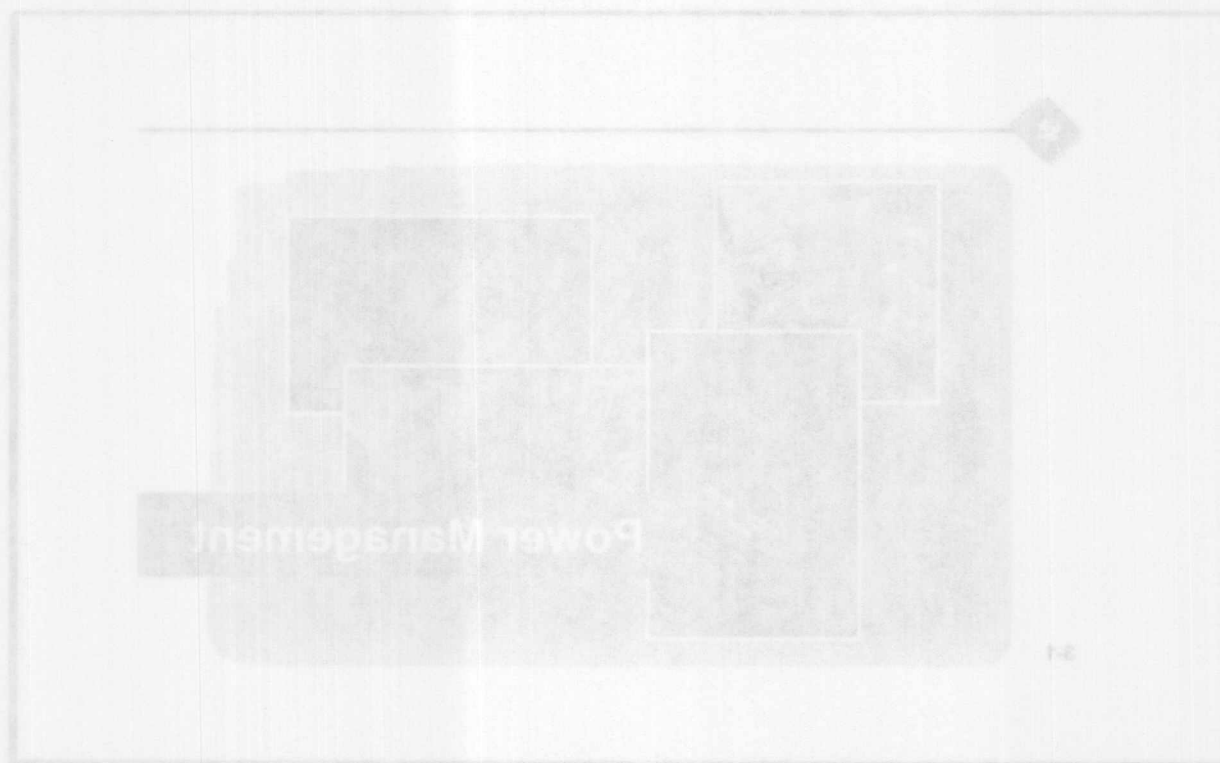
|          |                                                                                    |
|----------|------------------------------------------------------------------------------------|
| SLAA022  | Interfacing the TLV1544/TLV1548 ADC to Digital Processors                          |
| SLAA032  | Interfacing the TLC5540 ADC to the TMS320C203-80 DSP                               |
| SLAA028  | Interfacing the TLC5510 ADC to the TMS320C203 DSP                                  |
| SLAAE14  | Interfacing ADCs TLC554010 to the DSKPLUS DSP Starter Kit<br>TMS320C4X             |
| SLAA026A | Interfacing the TLV1572 ADC to the TMS320C203 DSP                                  |
| SLAA025  | Interfacing the TLV1544 ADC to the TMS320C203 DSP                                  |
| SLAA028  | Interfacing the TLV1544 ADC to the TMS320C203 DSP                                  |
| SWCA001  | Minimizing Input Design Problems with the TLV5590                                  |
| SLAA002  | Interfacing the TLV1548 10-Bit Serial-Out ADC to Popular 3-3-V<br>Microcontrollers |
| SLAA012  | Microcontroller Based Data Acquisition Using the TLC2543 12-Bit<br>Serial Out ADC  |
| SLAA017  | Interfacing the TLC2543 ADC to the TMS320C25 DSP                                   |
| SLAA018  | Signal Acquisition and Conditioning with Low Supply Voltages                       |
| SLAA013  | Understanding Data Converters                                                      |
| SLAA010  | TLC320AD57C Sigma-Delta Stereo Analog-to-Digital Converters                        |
| SLAA015  | TLC320AD58C Sigma-Delta Stereo Analog-to-Digital Converter                         |
| SLAA019  | TLC5932: PLL Building Block with Analog VCO & Phase Frequency<br>Detector          |

This is a representative sample and was accurate when this workbook was printed. For a complete up to date listing of application reports, designer note pages and EVMS please check the TI web site.



## **Power Management**

3-1

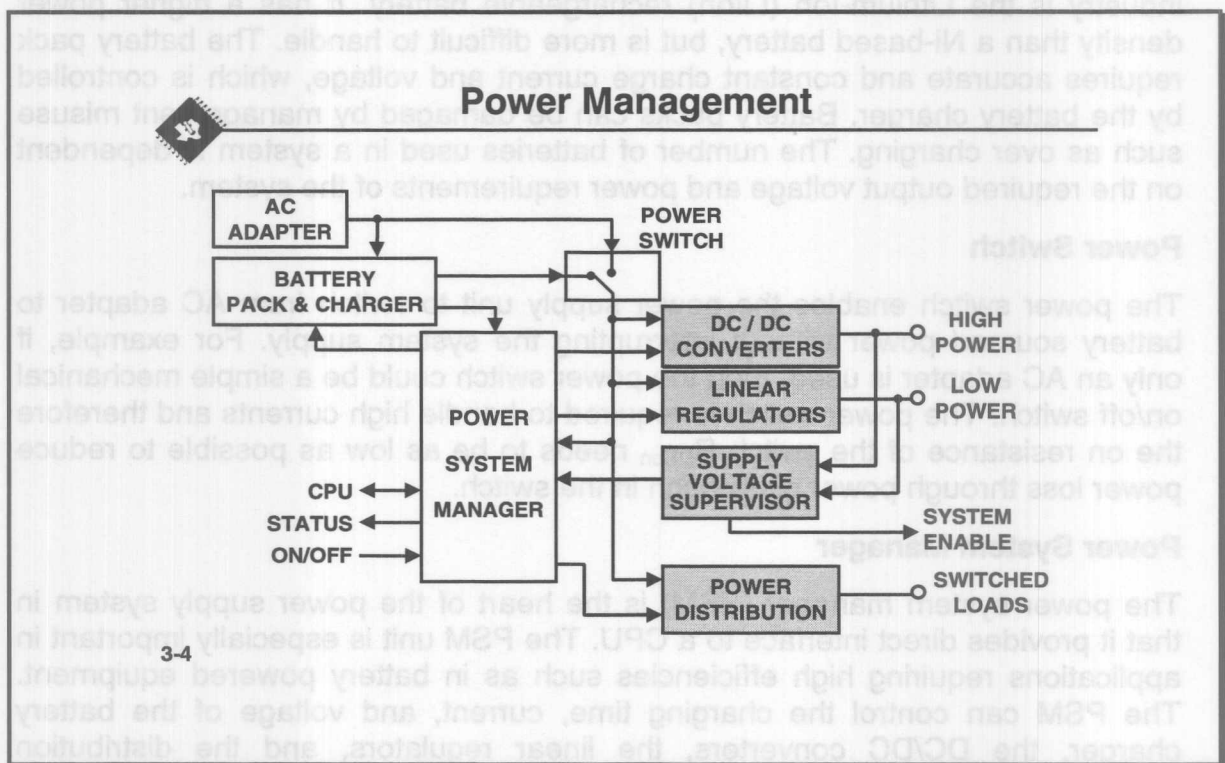


## Table of Contents

|                                                     |           |
|-----------------------------------------------------|-----------|
| <b>Power Management System Overview .....</b>       | <b>5</b>  |
| Power Management System Care Abouts .....           | 7         |
| <b>Linear Regulators .....</b>                      | <b>8</b>  |
| What is a Linear Regulator ? .....                  | 8         |
| Low Dropout Linear Voltage Regulators .....         | 10        |
| <b>Switch Mode (DC-DC) Power Supplies .....</b>     | <b>13</b> |
| Linear Regulator vs. Switch-Mode Power Supply ..... | 13        |
| Switch-Mode Regulator Topologies .....              | 14        |
| <b>Processor Power Supplies .....</b>               | <b>18</b> |
| Processor Power Requirements .....                  | 18        |
| DSP Power Supply Configurations .....               | 20        |
| DSP Power Requirements .....                        | 21        |
| Power Stage Considerations .....                    | 28        |
| Output Stage Considerations .....                   | 29        |
| Controller layout considerations .....              | 30        |
| Power Supply Layout Example .....                   | 31        |
| <b>Ripple Regulators .....</b>                      | <b>39</b> |
| Overview .....                                      | 39        |
| Voltage Mode Control .....                          | 39        |
| Average Current Mode .....                          | 40        |
| Peak current sensing .....                          | 41        |
| V <sup>2</sup> mode .....                           | 42        |
| Hysteretic (Ripple) mode control .....              | 43        |
| TPS5210 Ripple regulator .....                      | 44        |
| <b>Supply Voltage Supervisors .....</b>             | <b>46</b> |
| Supply Voltage Supervisor Selection Guide .....     | 47        |
| <b>Power Distribution .....</b>                     | <b>49</b> |
| PCMCIA Power Distribution Application .....         | 49        |
| PCMCIA Application .....                            | 51        |
| Universal Serial Bus Power .....                    | 52        |
| PC Connectivity .....                               | 53        |
| Self Powered USB Hub Application .....              | 55        |
| TPS2044 USB Power Application .....                 | 57        |

## Table of Contents

|    |                                               |
|----|-----------------------------------------------|
| 5  | Power Management System Overview              |
| 7  | Power Management System Core Abouts           |
| 8  | Linear Regulators                             |
| 8  | What is a Linear Regulator?                   |
| 10 | Low Dropout Linear Voltage Regulators         |
| 13 | Switch Mode (DC-DC) Power Supplies            |
| 13 | Linear Regulator vs. Switch-Mode Power Supply |
| 14 | Switch-Mode Regulator Topologies              |
| 18 | Processor Power Supplies                      |
| 18 | Processor Power Requirements                  |
| 20 | DSP Power Supply Configurations               |
| 21 | DSP Power Requirements                        |
| 28 | Power Stage Considerations                    |
| 29 | Output Stage Considerations                   |
| 30 | Controller layout considerations              |
| 31 | Power Supply Layout Example                   |
| 38 | Ripple Regulators                             |
| 38 | Overview                                      |
| 38 | Voltage Mode Control                          |
| 40 | Average Current Mode                          |
| 41 | Peak current sensing                          |
| 42 | V <sub>h</sub> mode                           |
| 43 | Hysteretic (Ripple) mode control              |
| 44 | TPS2210 Ripple regulator                      |
| 46 | Supply Voltage Supervisors                    |
| 47 | Supply Voltage Supervisor Selection Guide     |
| 48 | Power Distribution                            |
| 49 | PCMCIA Power Distribution Application         |
| 51 | PCMCIA Application                            |
| 52 | Universal Serial Bus Power                    |
| 53 | PC Connectivity                               |
| 55 | Self Powered USB Hub Application              |
| 57 | TPS2504 USB Power Application                 |



### Power Management System Overview

A power supply is required in every electrical and electronic system. When designing the power supply for the system, consideration needs to be given to the number of supply voltages required, the power handling capabilities of the supplies as well as the ultimate generator of the input. Depending on the power supply requirements of the system, there are eight building blocks that could be used to make up the power supply unit. The combination of the building blocks will depend on the input source and output power constraints of the system.

#### AC Adapter

The function of the AC adapter is to transform an AC voltage into a DC voltage. Traditionally, this has been accomplished by the use of a step-down transformer, bridge rectifier circuit, large smoothing capacitors and a linear regulator. However AC to DC converters are becoming popular due to the fact that they act as „intelligent switchers“. The AC input voltage can vary but the DC output must stay constant with little power dissipation in the module. This is difficult to achieve. The output voltage from the AC adapter can vary and is dependent on the voltage and power requirements of the application.

#### Battery Pack and Charger

Battery packs are generally made up of rechargeable batteries such as Nickel-Cadmium batteries (NiCd's), Nickel-Metal-Hydride batteries (NiMH's) or Lithium-Ion batteries (Lion's). The NiCd battery has long been the preferred chemistry technology due to its power density, but today NiMH is often used owing to the

environmental issues regarding NiCd. The newest development in the battery industry is the Lithium-Ion (Lion) rechargeable battery. It has a higher power density than a Ni-based battery, but is more difficult to handle. The battery pack requires accurate and constant charge current and voltage, which is controlled by the battery charger. Battery packs can be damaged by management misuse such as over charging. The number of batteries used in a system is dependent on the required output voltage and power requirements of the system.

### **Power Switch**

The power switch enables the power supply unit to switch from AC adapter to battery sourced power without interrupting the system supply. For example, if only an AC adapter is used, then the power switch could be a simple mechanical on/off switch. The power switch is required to handle high currents and therefore the on resistance of the switch  $R_{DSon}$  needs to be as low as possible to reduce power loss through power dissipation in the switch.

### **Power System Manager**

The power system manager (PSM) is the heart of the power supply system in that it provides direct interface to a CPU. The PSM unit is especially important in applications requiring high efficiencies such as in battery powered equipment. The PSM can control the charging time, current, and voltage of the battery charger, the DC/DC converters, the linear regulators, and the distribution supplies through commands from the CPU thus powering down sections of a system to save power. The PSM can also take inputs from the supply voltage supervisor (SVS) and act on the results or relate messages to the CPU if any problems occur during the power-on stage.

### **DC/DC Converters**

DC/DC converters change an input voltage level to either a higher, lower, or negative voltage. The input voltage source can be either the AC adapter or the battery pack. The efficiency in changing the input voltage to the required output voltage is important in both cases. The most common type of converter for high power is switching regulators.

### **Linear Regulators**

Linear regulators convert the input voltage to a lower output voltage by dissipating the power that is not needed. However, they are normally only used for low output power.

### **Supply Voltage Supervisors**

Supply voltage supervisors (SVS) are used to monitor the input voltage to the power supply unit for early warning and from the power supply unit to ensure that the system operates within a defined supply voltage window. The added feature is that devices sensitive to supply potentials can be protected during power-up and power-down stages.

**Power Distribution**

Distributed power supplies are generally used in power supply systems where power efficiency is critical. Instead of the power supply being routed around the board to the individual components, the board is laid out in groups dependent on component function, with a power supply control element being used to power-up and power-down the individual groups when required. This means that the overall power consumption of the system can be significantly reduced by turning off parts of the application that do not require power at a particular time.

**Power Management System Care Abouts****Power Management System Care Abouts****Voltage/Current output****Efficiency****Line/Load Regulation****Accuracy****Noise****System Cost**3-5 

Regardless of the system component or end application the factors which are important remain the same.

- What is the power requirement in voltage and current?

This is important both in terms of power supply capacity and response times. Power supply response times will be discussed in the Processor Power section.

- What efficiency is needed?

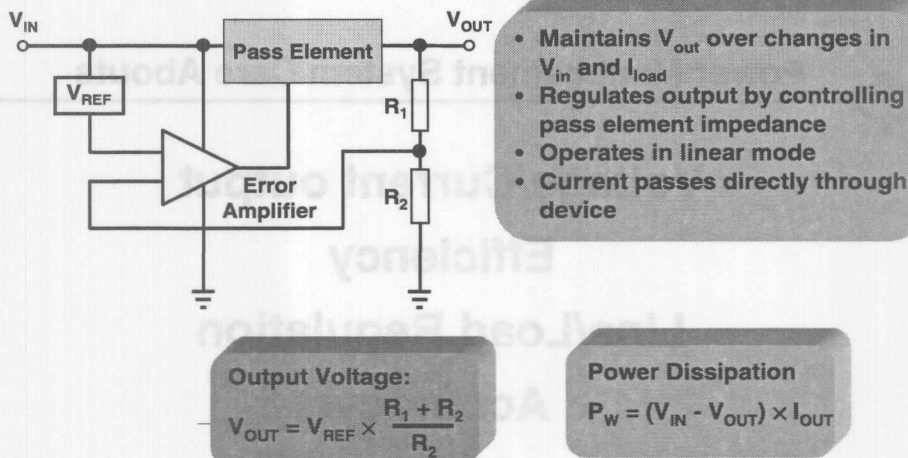
Efficiency is important in terms of heat and for portable applications battery life.

- Line/Load Regulation is an important factor especially as systems operate on lower voltages with less operating headroom.
- Accuracy is a factor in areas such as reference for high resolution data conversion systems.

- Noise generated by switching power supplies is important in sensitive analog circuits.
- System cost is always a factor often overlooked since power supply and distribution is often spread out across the entire system.

## Linear Regulators

### What is a Linear Regulator?



3-7

### What is a Linear Regulator ?

Linear series voltage regulators are often used where the input power source is unregulated or clean supplies are required in a noisy environment.

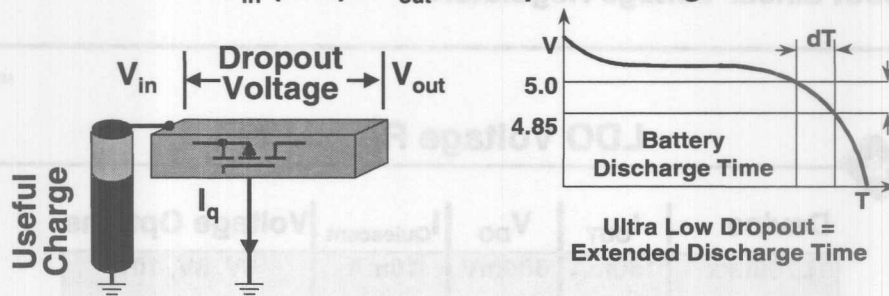
The input voltage of a linear regulator is always higher than the output voltage. The power that is not needed is dissipated by the pass element, i.e. converted into heat.

The output voltage is divided down with a resistive divider and compared with the reference voltage. If the output voltage is too low, the error amplifier drives the pass element more and if the output voltage is too high the error amplifier drives the pass element a little less. The output voltage is therefore regulated by the resistive divider and error amplifier.

The power dissipation of a linear regulator depends on the difference between the input and output voltage and the output current. This means a voltage regulator is only useful and efficient if the input-output differential is small compared to the output voltage.

## What is Drop-Out Voltage?

$$V_{in}(\text{min}) - V_{out} = \text{Dropout Voltage}$$



### Minimum Dropout Voltage

| nnp-Transistor                                                                                   | pnp-Transistor                                                       | PMOS-Transistor                                                       |
|--------------------------------------------------------------------------------------------------|----------------------------------------------------------------------|-----------------------------------------------------------------------|
| $V_{\text{Dropout}} = V_{\text{Opamp}} + V_{\text{BE}}$<br>(e.g. 2V - 3V for $\mu\text{A}7805$ ) | $V_{\text{Dropout}} \approx V_{\text{CE}}$<br>(e.g. 600mV for TL750) | $V_{\text{Dropout}} \approx V_{\text{DS}}$<br>(e.g. 32mV for TPS71xx) |

3-8

## What is Dropout Voltage

The dropout voltage is the voltage difference between input and output voltage when regulation ceases. It is also necessary to pay attention to the quiescent current if the regulator source is a battery. Both the dropout and the quiescent current reduce the battery life.

The dropout voltage of a regulator with a npn-transistor as pass element is very high and depends on the driver capability of the error amplifier, and is a minimum of one forward voltage of a diode. The quiescent current is not very critical because it is part of the output current. Both dropout and quiescent current can increase when the transistor is in saturation.

In a regulator with a pnp-transistor the dropout voltage is lower, i.e. the saturation voltage of the transistor, and is independent on the driver capability of the error amplifier because the base is driven to ground. The quiescent current in such a regulator is very critical because bipolar transistors are current driven and in a regulator with a pnp pass element, the current is lost (it flows from the input to ground). Therefore, this device would also decrease the battery life quickly.

Low dropout (LDO) voltage regulators with PMOS-transistor pass elements have a dropout voltage that is proportional to the output current. The dropout voltage is dependent on the on-resistance  $R_{\text{DSon}}$ . The quiescent current is very low (PMOS-transistors are voltage driven) and it stays low over load and input voltage. The load, line, and ripple rejection can be increased with good design techniques.

TI's latest generation of LDO regulators: the TPS71xx, TPS72xx, and TPS73xx families use an integrated PMOS pass transistor to achieve ultra low dropout.

The standby current is maximum 0.5  $\mu$ A. This, in combination with their extremely low quiescent currents, yields a more efficient voltage regulator that can significantly extend battery life.

## Low Dropout Linear Voltage Regulators

SHOW

### LDO Voltage Regulators

| Device     | I <sub>OUT</sub> | V <sub>DO</sub> | I <sub>Quiescent</sub> | Voltage Options       |
|------------|------------------|-----------------|------------------------|-----------------------|
| TL750Lxx   | 150mA            | 600mV           | 10mA                   | 5V, 8V, 10V           |
| TL751Lxx   | 150mA            | 600mV           | 10mA                   | 5V, 8V, 10V, 12V      |
| TPS72xx    | 250mA            | 85mV            | 225 $\mu$ A            | 3.3V, 4.85V, 5V, Adj. |
| TL75LPxx   | 300mA            | 600mV           | 6mA                    | 5V, 8V, 10V, 12V      |
| TLV2217-33 | 500mA            | 600mV           | 2mA                    | 3.3V                  |
| TPS71xx    | 500mA            | 32mV            | 350 $\mu$ A            | 3.3V, 4.85V, 5V, Adj. |
| TPS73xx    | 500mA            | 35mV            | 400 $\mu$ A            | 3.3V, 4.85V, 5V, Adj. |
| TL750Mxx   | 750mA            | 600mV           | 10mA                   | 5V, 8V, 10V, 12V      |
| TL751Mxx   | 750mA            | 600mV           | 10mA                   | 5V, 8V, 10V, 12V      |

All TI LDOs have a  $\pm 2\%$  tolerance, or better

3-9

SHOW

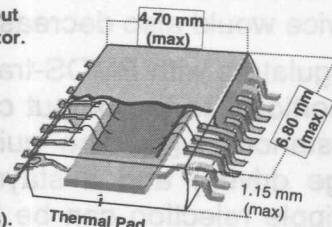
### Ultra-Low Drop-out Regulators

| Device   | Dropout Voltage (mV-max) | Load Current (mA-max) | Quiescent Current ( $\mu$ A-max) | Standby Current ( $\mu$ A-max) | Voltage Options |
|----------|--------------------------|-----------------------|----------------------------------|--------------------------------|-----------------|
| TPS71025 | 32                       | 500                   | 350                              | 0.5                            | 2.5 V           |
| TPS71xx  | 32                       | 500                   | 350                              | 0.5                            | The rest:       |
| TPS72xx  | 85                       | 250                   | 225                              | 0.5                            | Adj., 3.3 V     |
| TPS73xx  | 35                       | 500                   | 400                              | 0.5                            | 4.85 V. &       |
| TPS71Hxx | 32                       | 500                   | 350                              | 0.5                            | 5 V             |

**TPS71xx** - The best dropout performance of any regulator.

**TPS72xx** - A low cost TPS71xx alternative.

**TPS73xx** - TPS71xx performance with a microprocessor reset (SVS).



**20-pin TSSOP  
PowerPad™  
Package:**

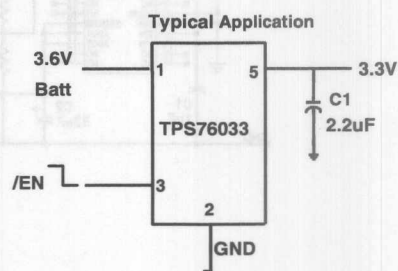
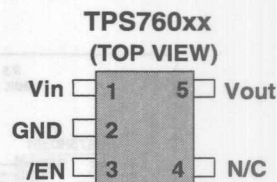
- Thermally enhanced surface mount (PWP) package  
 $R_{\theta JC} = 3.5^\circ\text{C/W}$
- Dissipates over 2 W  
4 X standard TSSOP power handling ability

3-10

## TPS760XX LDO REGULATOR

- 50mA Low Drop Out regulator (TPS760xx)
- 100mA Low Drop Out regulator (TPS761xx)
- Voltage options: 5.0, 3.8, 3.3, 3.2, 3.0
- Dropout, typically 100mV @ 50mA
- Thermal protection
- Less than 1uA quiescent current in shutdown
- -40°C to +85°C ambient operating temp. range
- 5-pin SOT-23 package

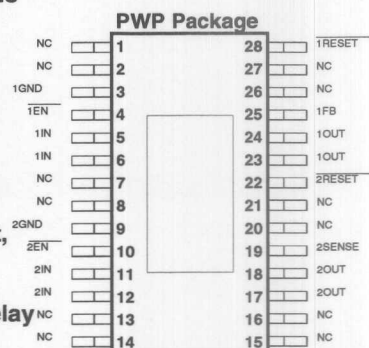
| PART NUMBER |             | VOLTAGE |
|-------------|-------------|---------|
| TPS76030DBV | TPS76130DBV | 3.0V    |
| TPS76032DBV | TPS76132DBV | 3.2V    |
| TPS76033DBV | TPS76133DBV | 3.3V    |
| TPS76038DBV | TPS76138DBV | 3.8V    |
| TPS76050DBV | TPS76150DBV | 5.0V    |



3-11

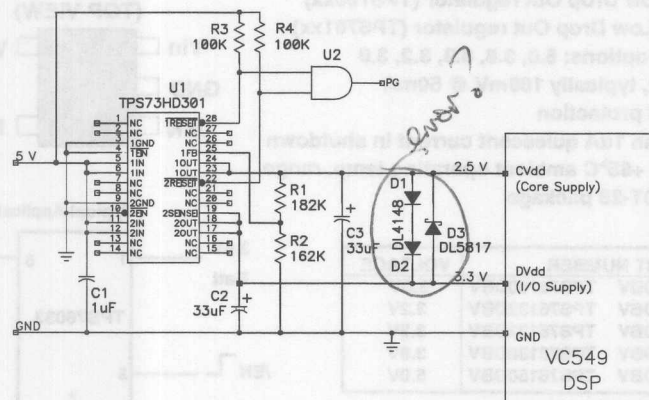
## TPS73HD301 Dual Output LDO

- 2 Output Voltages for Split-Supply Applications
- 3.3V fixed and 1.2V to 9.75V Adj. Outputs
- Dropout Voltage = 350mV at 750mA
- Low Quiescent Current, Independent of Load, Typically 340uA per Regulator
- Output Regulated to  $\pm 2\%$  Max for 3.3V Output
- Output Current Range to 750mA either Output, 1A max Device Rating
- Dual Active-Low Reset Signals with 200ms Delay
- Ultra-low Current Sleep State Mode, 2uA Max
- Thermally Enhanced PowerPad™



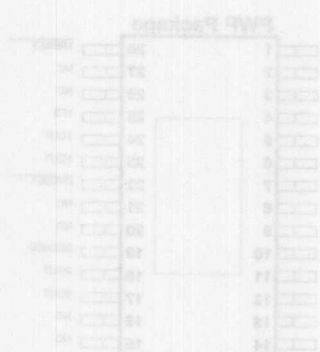
3-12

## TPS73HD301 DSP Application



3-13

## TPS73HD301 Dual Output LDO

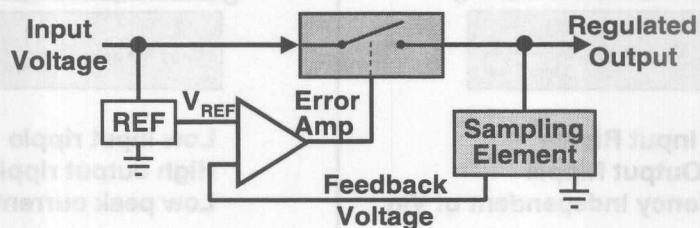


- 2 Output Voltages for Split-Supply Applications
- 3.3V fixed and 1.2V to 0.75V Adj. Outputs
- Dropout Voltage = 350mV at 750mA
- Low Quiescent Current, Independent of Load
- Typically 340µA per Regulator
- Output Regulated to  $\pm 2\%$  Load for 3.3V Output
- Output Current Ranges to 750mA either Output
- 1A max Device Rating
- Dual Active-Low Reset Signals with 200ms Delay
- Ultra-Low Current Sleep Mode, 2µA Max
- Thermally Enhanced PowerPAD™

3-12

## Switch Mode (DC-DC) Power Supplies

### What is a Switching regulator or DC/DC Converter?



**A network of components that transfers power from one DC level to another. The circuit may or may not provide isolation, and may step-up or step-down the input voltage**

3-15

### Linear Regulator vs. Switch-Mode Power Supply

The transistor used in a linear regulator works as a variable resistor that reduces the voltage by dissipating the power that is not needed. Therefore, the efficiency is low if the difference between the input and output voltage is high.

The transistor in a switch-mode power supply operates as a switch, either fully conducting or blocking. The switch is opened and closed at a high frequency and only closed as long as needed to transfer the necessary output power. The efficiency can be very high (90 % or more).

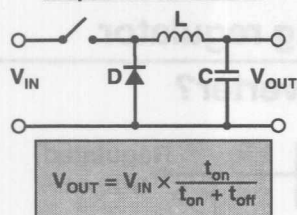
The advantages of a switch-mode power supply compared with a linear regulator are high efficiency, high power-to-weight ratio, and high input to output differential.

Nevertheless, there are also advantages of linear regulators. In a linear regulator the electrical noise is lower, the design of a linear regulator is less complex, and the output ripple is smaller.

## Switch Mode Regulator Topologies

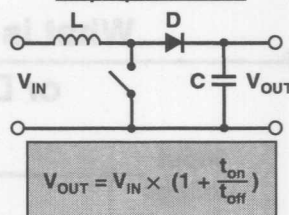


**Step-Down Converter**



High Input Ripple  
Low Output Ripple  
Efficiency Independent of  $V_{in}$

**Step-Up Converter**



Low input ripple  
High output ripple  
Low peak currents

3-16

## Switch-Mode Regulator Topologies

There are four different basic switch mode power supply topologies.

Switch-mode supplies are controlled by the opening and closing of a switch

Making the output voltage a function of  $t_{on}$  and  $t_{off}$ .

$t_{on}$ : time where current flows through the switch

$t_{off}$ : time where current flows through the diode (continuous-mode only)

### Step-Down Converter (also called Buck Converter)

When the switching element is closed, current flows through the inductor. When the switch is open the energy stored in the inductor maintains the current flow to the load and the charge on the capacitor.

Compared with the other three basic topologies the output ripple is the lowest because of the location of the inductor. This makes it appropriate for noise-sensitive loads. The disadvantages of this topology are that the switch has to be a PMOS-transistor or a floating drive must be used for the switch and usually there is a need for a significant input EMI filter.

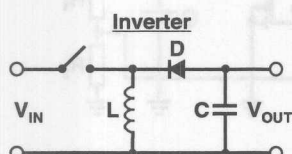
### Step-Up Converter (also called Boost Converter)

When the switching element is closed, current flows only into the inductor. When the switch opens the energy stored in the inductor plus the input voltage flows to the load and charges the capacitor.

The output ripple of this topology is relatively high. A step-up converter is very useful for low input voltages or low power applications, for example in battery-

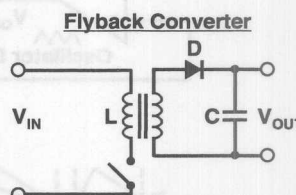
driven systems where some devices need 5-V supply voltage. The biggest disadvantage of this topology is the high output voltage ripple because the output capacitor has to supply the entire load during the transistor on-time.

## Switch Mode Regulator Topologies



$$V_{OUT} = -V_{IN} \times \frac{t_{on}}{t_{off}}$$

$V_{OUT} = -V_{IN}$   
High output ripple  
Efficiency independent of  $V_{IN}$



$$V_{OUT} = V_{IN} \times \frac{t_{on}}{t_{off}} \times \frac{1}{a}$$

High output ripple  
Sensitive to load changes  
High peak output currents

3-17

### Inverter (also called Buck-Boost Converter)

When the switching element is closed, current flows into the inductor. When the switch opens the diode-inductor junction goes negative and the energy stored in the inductor flows into the load and charges the capacitor.

The output ripple is also high because the output capacitor has to supply the entire load during one portion of the switching cycle. Some battery driven systems like mobile phones need a negative voltage to supply some RF amplifiers.

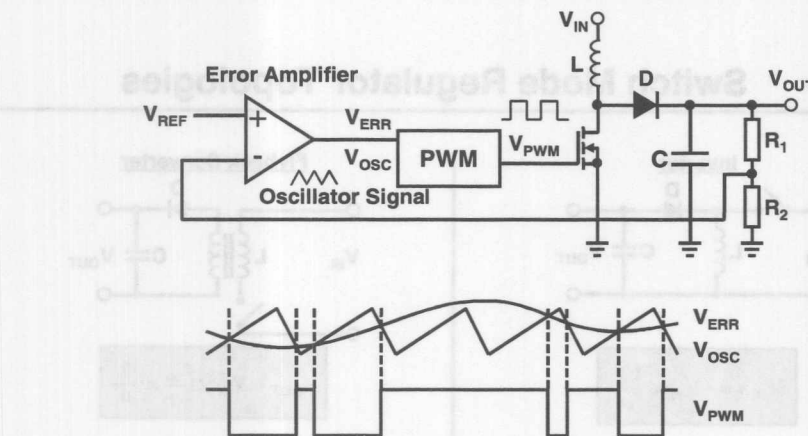
### Flyback Converter

When the switching element is closed, current charges the first inductor. When the switch is open the energy stored in the first inductor is transferred to the second inductor and then to the load and capacitor.

The output ripple is high because, during the on-time the output current is supplied entirely by the output capacitor. This converter can be used in a computer where the supply voltage needs to be decoupled from the net supply and the input voltage needs to be transformed down from, say, 24V to 3V or 5V. This sort of switch mode power supply is normally only used where the space needed for the inductor (transformer) is not a limiting factor.

## Pulse Width Modulation

### Voltage Mode "Boost" Converter



3-18

### Pulse Width Modulation (Voltage Mode)

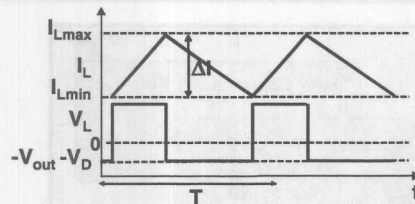
In a switch-mode voltage regulator the transistor operates as a switch. Pulse width modulation is the most common method used to control this switching transistor, the on and off time being controlled as a function of the output voltage.

The output voltage  $V_{out}$  that is to be regulated is divided by a resistive divider network  $R_1/R_2$ , and compared with the internal reference voltage by the error amplifier. The difference between the required and the actual value is amplified, and compared in the pulse width modulator with the oscillator signal. The output signal of the pulse width modulator is a square-wave pulse, of "constant" frequency (some pulses may be lost or the duty ratio may be 1) and variable pulse duty ratio. If the amplitude of the output signal of the error amplifier is greater than that of the oscillator signal, then the output of the pulse width modulator will drive the transistor on; if it is less, the transistor will be driven off.

## Continuous vs. Discontinuous Mode

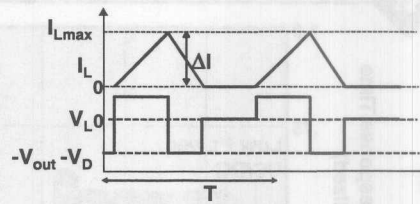


Continuous Operation



Current in the inductor or transformer of the converter flows during the entire cycle

Discontinuous Operation



Current in the inductor or transformer of the converter drops to zero and remains at zero for a finite period of time during each cycle

Minimum Output Current in Continuous Mode:

$$I_{OUTmin} = \frac{T}{2 \times L} \times V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

3-19

## Continuous vs. Discontinuous Mode

### Continuous Operation:

The current in the inductor does not drop to zero.

If the output current sinks below the minimum output current, the flow of current in the inductor will be interrupted. In order to avoid this, the pulse duty ratio must be changed; otherwise the output voltage will rise. Since the pulse duty ratio is limited to the finite switch-on time of the switching transistor, the inductance of the inductor should be chosen to insure that the current in the inductor is not interrupted at the minimum rated output current.

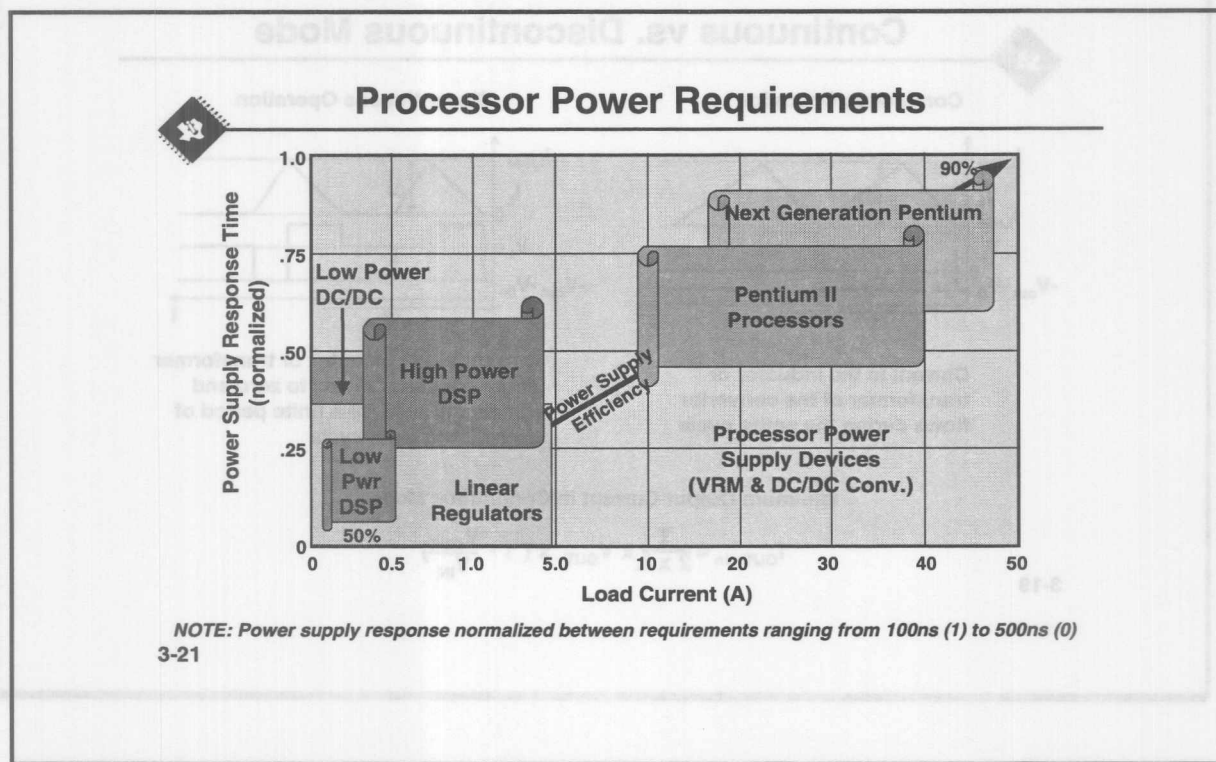
The changeover from the continuous mode to the discontinuous mode occurs when the current in the inductor touches the zero line.

### Discontinuous Operation:

The current in the inductor drops to zero for some period during each cycle.

For a given output power the discontinuous mode produces higher voltage and current stresses than the continuous mode and also more input and output filtering is required. However, in general, the discontinuous mode is easier to stabilize.

## Processor Power Supplies

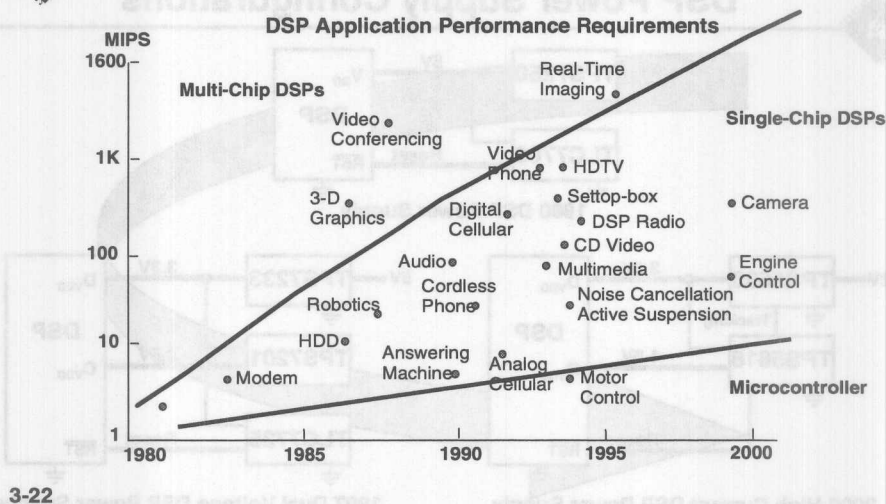


## Processor Power Requirements

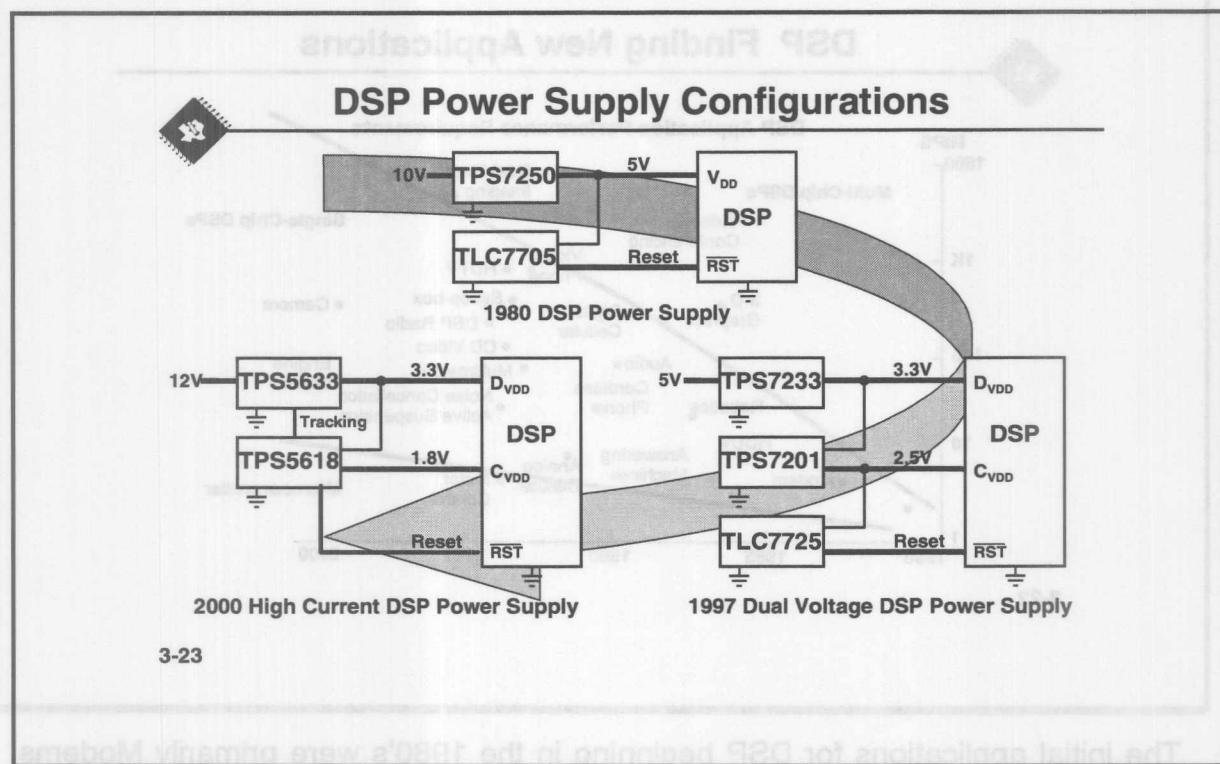
The chart above depicts the range of processors typically used today from low power DSPs to the next generation Pentiums. As you can see, as the processing power increases the power requirement increases and the required response times decrease. Although the power can be supplied to low power DSPs and low end microprocessor with conventional linear regulators and LDOs the higher performance parts require higher power and efficiencies.

This section will discuss the power requirements of the higher performance processors and the solutions currently available. Both efficiency and response times will be addressed.

## DSP Finding New Applications



The initial applications for DSP beginning in the 1980's were primarily Modems implemented with a single processor. Today applications are using processors with over three orders of magnitude increase in speed and in some cases, multiple processors. Each application represents a need for power supplies, which are efficient and have fast response to transients.



### DSP Power Supply Configurations

The typical power system for first generation DSPs was a single linear regulator and supply voltage supervisor. Current DSP designs use separate power supplies for the DSP core and the interface circuitry. The dual supply system allows for lower power consumption by the core while having a higher voltage for a standard interface to the rest of the system. A typical power supply system for the current DSPs may include two LDO linear regulators and a supervisor circuit.

The newest systems will require power levels such that switching supplies are preferred. In addition to the high efficiency a high transient response speed is required. Traditionally transient response has been addressed with bulk capacitance. As the requirements increase the bulk capacitance solution becomes more expensive and requires a larger space.

The last solution on the figure above shows the utilization of two of the newest switching regulators from Texas Instruments. The TPS56xx are a family of ripple regulators, which will be discussed later in this section.



## DSP Current Requirements

Current dependency can be broken down into two categories:

### System Related

Operational Frequency  
Supply Voltage  
Operating Temperature  
Output Load

### DSP Related

Operational Duty Cycle  
Number of Buses in use  
Wait States, Cache Usage  
Data Values

$$I_{\text{total}} = (I_q + I_{\text{iops}} + I_{\text{ibus}} + I_{\text{addr}} + I_{\text{data}} + I_{\text{cntl}}) * F * V * T$$

3-24

## DSP Power Requirements

The total current requirement for a DSP can be separated into two components.

System related factors are operating frequency, supply voltage, temperature and output load. DSP related factors are duty cycle, number of busses in use, wait states etc. The important issue is that the DSP related factors tend to be additive and the system factors are products. The result is that changes in system factors have a much larger impact on total power than the changes in the DSP factors.

$$I_{\text{total}} = (I_q + I_{\text{iops}} + I_{\text{ibus}} + I_{\text{addr}} + I_{\text{data}} + I_{\text{cntl}}) * F * V * T$$

**Where:**

**$I_{\text{total}}$  = total supply current**

**$I_q$  = quiescent current component**

**$I_{\text{iops}}$  = internal operations current component**

**$I_{\text{ibus}}$  = internal bus usage current (includes data value and cycle time dependency)**

**$I_{\text{addr}}$  = external address bus activity current component**

**$I_{\text{data}}$  = external data bus activity current component**

**$I_{\text{cntl}}$  = external control line activity current component**

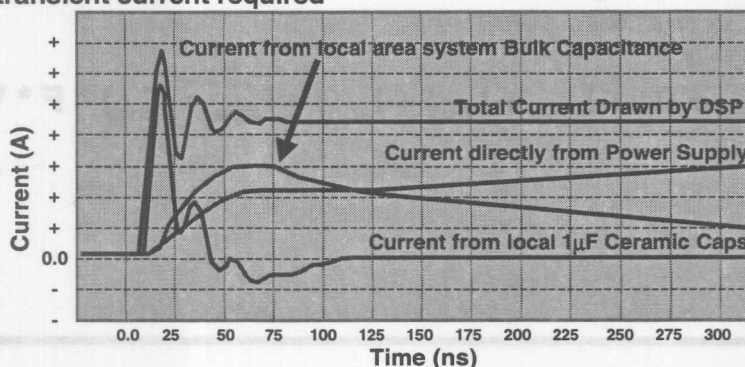
**$F$  = Scale factor for operating frequency**

**$V$  = Scale factor for supply voltage**

**$T$  = Scale factor for operating temperature**

## System Sources for Current

The power supply is not the only current source in the system, and in most cases is not the supplier of the bulk of the transient current required



Local bypass capacitors are good for "instantaneous" sources of current, but bulk capacitance will carry the lions share

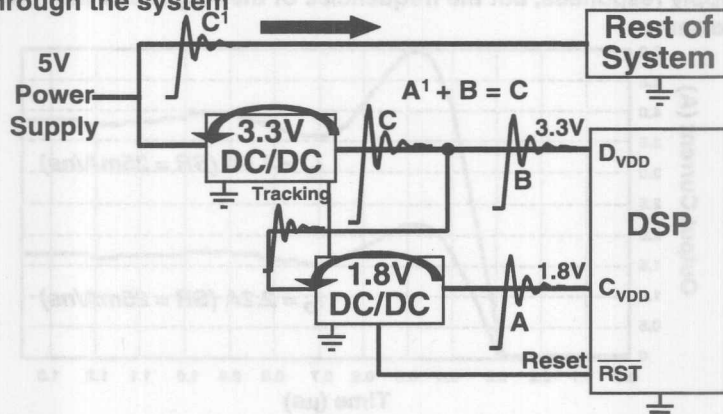
3-26

During operation the total current to the processor is provided by the power supply. When transients occur such as a result of changes in the DSP operation the instantaneous current is supplied first by the local bypass capacitors. The local bypass capacitors are usually ceramic; they respond quickly but are limited due to the relatively low capacitance values. The next source of current is typically bulk capacitors located near the processor or power supply output. The bulk capacitance supplies the current transient until the power supply can respond. The graph above shows typical response times for each of these components. For a system to operate without errors due to transients the power supply, local bypass and bulk capacitance must be sized to provide the required transient current.

### The Transient Path



Transient noise on any voltage rail can and will be fed back through the system



By placing additional capacitance in any of the areas transients pass through, or by increasing the main supply voltage, system noise transmission can be reduced

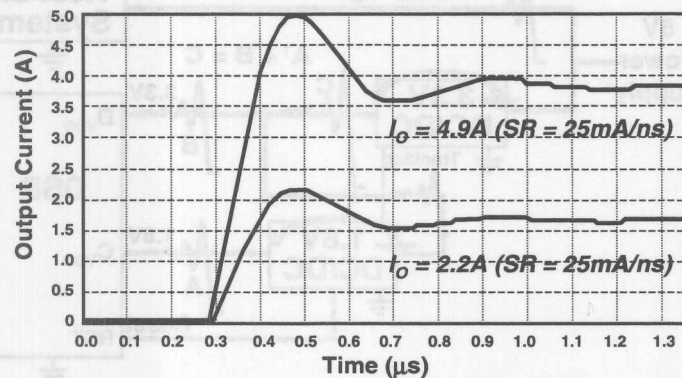
3-27

When considering power supply transients the entire system should be considered. The figure above is an example of a DSP system which has  $D_{VDD} = 1.8V$  and  $C_{VDD} = 3.3V$ . The 3.3V is generated from the system 5V supply. The 1.8V is generated from the 3.3V supply. Transients (A) occurring on the 1.8V supply which are not supplied by a bypass capacitor are coupled to the 3.3V line where the transients (B) are added. The total is then coupled to the 5V supply and can be propagated to the remainder of the system. Transients can be reduced by increasing the system voltage and additional bypass capacitors.



## Power Supply Transient Response

Different magnitudes of load current result in different power supply responses, but the frequencies of the responses will remain the same.



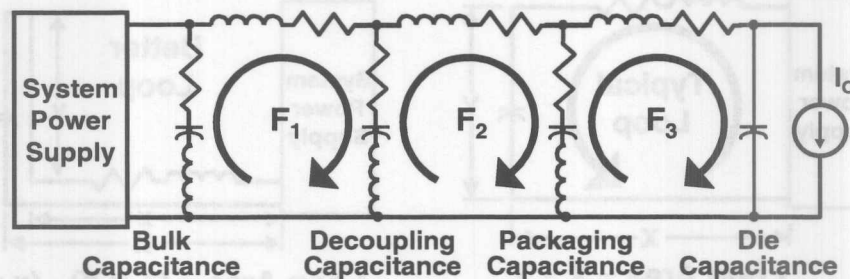
The rate of change of the load is much faster than the rate of change capability of any of the resonant loops in the system

3-28

The slide above is the current supplied at the power supply for a typical DSP. Notice that in both waveforms the frequency is the same although the peak current in the lower trace is 2.2A compared to 4.9A in the upper trace. This is due to the fact the response is dominated by the power supply itself since it is much slower than the actual DSP current transient. To further understand this the resonant loops in the power supply system should be considered.

## System Resonant Loops

Most DSP and Processor models can be considered as three distinct resonant loops, each with its own frequency.



Each loop is basically a second order system where the resonant frequencies have the relationship of:  $F_3 > F_2 > F_1$

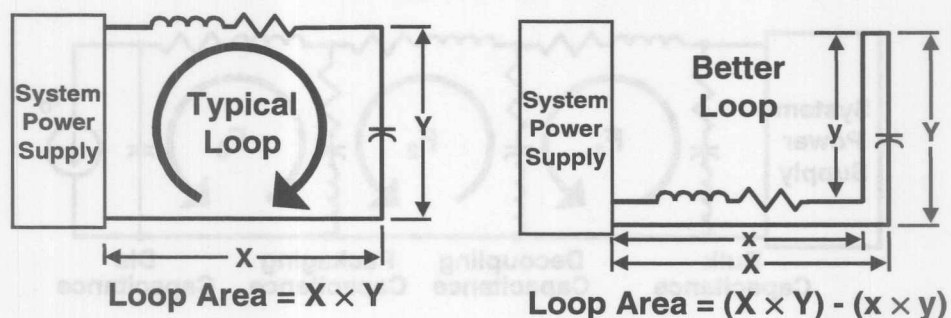
3-29

A system consisting of a power supply, bulk capacitor, decoupling capacitor, processor and the interconnections can be modeled as in the figure above. The bulk capacitance and decoupling capacitance form a resonant loop  $F_1$ . The decoupling capacitance and package capacitance form a resonant loop  $F_2$ . The package capacitance and processor die capacitance form a resonant loop  $F_3$ . Each of successive capacitance is smaller and therefore each loop has a higher resonant frequency with  $F_1$  being the lowest and  $F_3$  the highest resonant loop.

Each loop serves to dampen the transients coupled back into the system. A well-designed system minimizes the amount of transients coupled back to the power supply.

## Current Loops

Minimizing loop areas and keeping lead lengths short decreases system noise and trace inductance, and increases trace capacitance



Basically, loop area is the amount of physical board space trapped between the traces forming the current path from the supply to the system and back to the supply

3-30

Careful circuit layout can also minimize transients both coupled and radiated. A guideline for reducing this system noise is to minimize current loop areas. The area inside the resonant current loop can be minimized by running the supply and return adjacent to each other or over each other on separate board layers.

## Layout Methods



### **"Scatter"**

Throw the parts up and wherever they land, connect them per schematic.

### **"Digital "**

Line everything up in neat little rows and connect with tiny traces.

### **"Analog"**

Layout sensitive nodes first and work toward output.

### **"Ideal"**

Layout power stage, then output, then sensitive nodes, finally the rest.

3-31

Numerous methods are currently in use for PWB layout. Some of them are:

**Scatter** – produces an interesting topology, a variation of this is to squeeze all the parts into the smallest area then connect them up. In both cases the results are less than desirable.

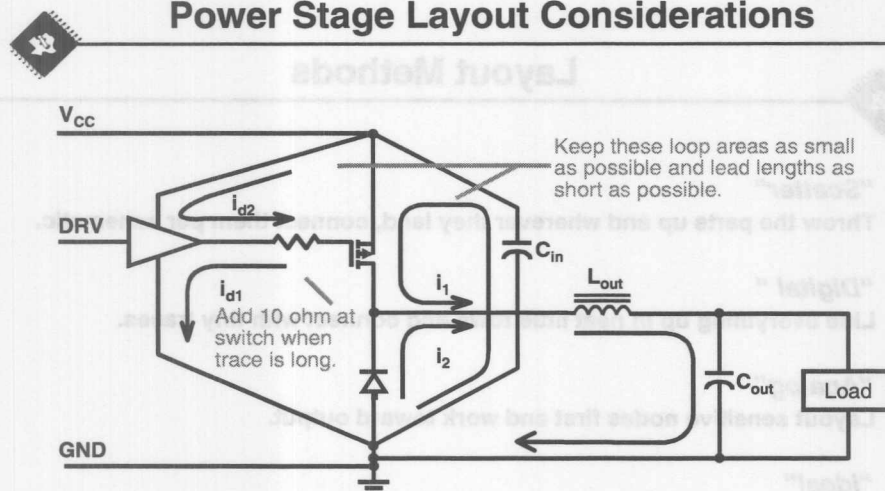
**Digital** – this method of neatly arranging the parts is the system preferred by automated layout software. Great for memory boards but do not use for power supplies.

**Analog** – laying out the sensitive nodes first is a step in the right direction and will work with most analog circuits.

**Ideal** – the best method for power supply layout is a stepwise approach dealing first with the high current nodes and loops then the sensitive nodes.

A good layout is absolutely essential both in terms of operation as well as noise especially with switching supplies. The following pages provide additional layout details.

## Power Stage Layout Considerations



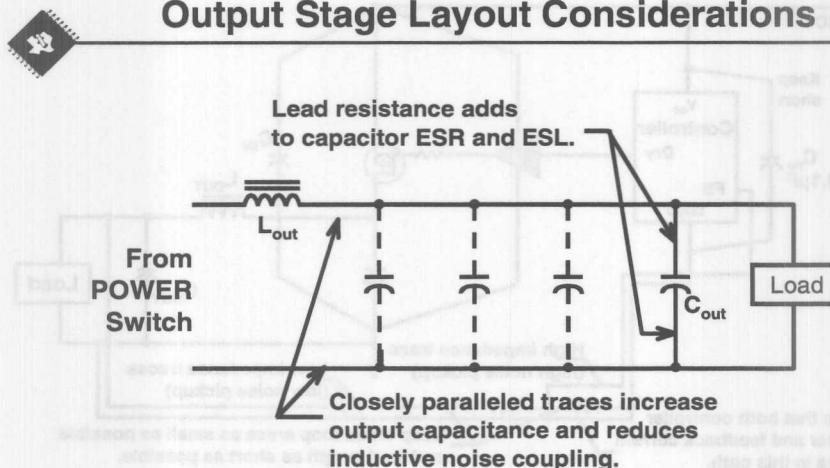
3-32

### Power Stage Considerations

The power stage includes the low-pass output filter, the power switch, and the input filter. It contains very high circulating currents and therefore should be given the highest priority when laying out the PCB. The figure above shows the current paths for a typical buck converter. The charging (forward) current,  $i_1$ , flows through the input capacitor, the power switch, and the inductor before splitting between the output capacitor and the load. The inductor discharge (commutating) current,  $i_2$ , flows through the commutating diode and the inductor, then to the output capacitor and the load. The peak value of these currents is the same. The paths for these currents should be as short as possible. Note that the input filter capacitor should be close to the power switch and the commutating diode.

Next in priority, due to its relatively high current level, is the drive circuit for the power stage. It should be placed as close to the power switch as possible. The power switch generally has a large input capacitance associated with its gate. High peak currents are used to achieve the very fast rise and fall times required for high efficiency. If the gate lead trace is longer than approximately two inches, a small (approximately 10  $\Omega$ ) resistor should be placed in the trace near the FET to damp the LC tank formed by the inductance of the trace and the gate capacitance of the FET. Current  $i_{d1}$  is the turn-on current that charges the gate capacitance and current  $i_{d2}$  is the turn-off current that discharges this capacitance. When using bipolar power switches, base capacitance is not a problem, but the average drive current is much higher, resulting in the same requirement for short current paths.

## Output Stage Layout Considerations



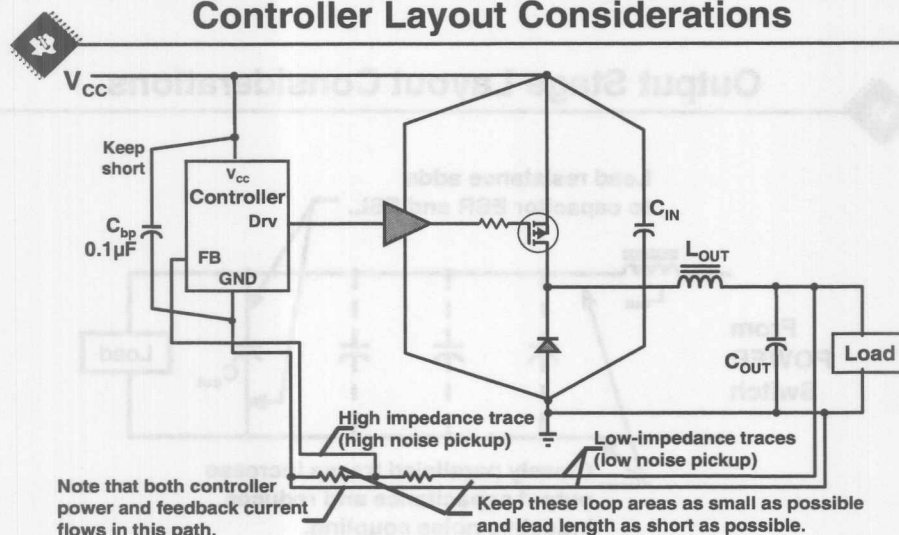
3-33

### Output Stage Considerations

The output filter capacitor placement is not as critical as the input filter. Output current flows through the output inductor to the load. Additional trace length in this path acts as additional capacitance as long as the power and return traces are physically close to each other. The trace length from the output capacitor to the main output trace should be kept as short as possible. This minimizes the series resistance and inductance between the capacitor and the main trace. In many cases, parallel capacitors are used in the output filter to reduce the equivalent series resistance (ESR). If the capacitors are connected at equal intervals along the output path, the effective ESR of the first capacitor is much lower than the last capacitor. Care must be used in this configuration to make sure that the higher ripple current that it must conduct does not overload the first capacitor in the string.

The ideal configuration on multi-layer boards is for the output and return traces to be directly over each other to minimize the enclosed loop inductance and to increase coupling capacitance. This technique can be beneficial when applied to almost any closed signal path. On single-sided boards, the optimum solution is closely paralleled traces.

### Controller Layout Considerations

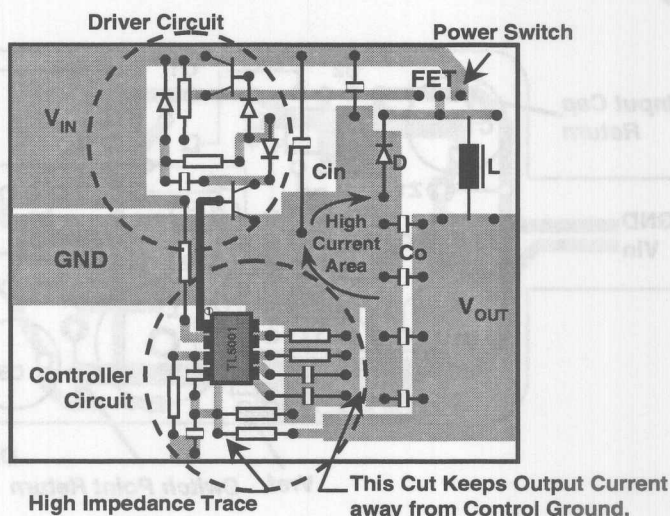


3-34

### Controller layout considerations

Ground connections are very critical in the control stage of a power supply. Any voltage difference between the feedback divider ground and controller ground will result in an error in the output voltage. Noise pickup in the sensing circuit will be amplified and fed directly to the output. Ideally, the controller supply current should not flow through the feedback path. The supply voltage should be bypassed to prevent transient currents from the controller from being propagated across the PCB. The bypass capacitor ( $C_{bp}$ ) should be located as close as possible to the controller with short leads to the VCC and ground pins. Surface mount chip capacitors mounted next to the controller will give the shortest possible routing. Again, current loops should be minimized with parallel traces to reduce noise radiation and pickup. The feedback path from the low impedance output through the resistor divider to the high impedance op amp inputs should be as short as possible and should consist of parallel paths to reduce noise pickup. Sometimes breaking the ground plane into two or more sections with a single common connection point can help in keeping the high output-return current from flowing around or near the controller circuitry. This technique can greatly reduce noise pickup by the sensitive controller circuitry.

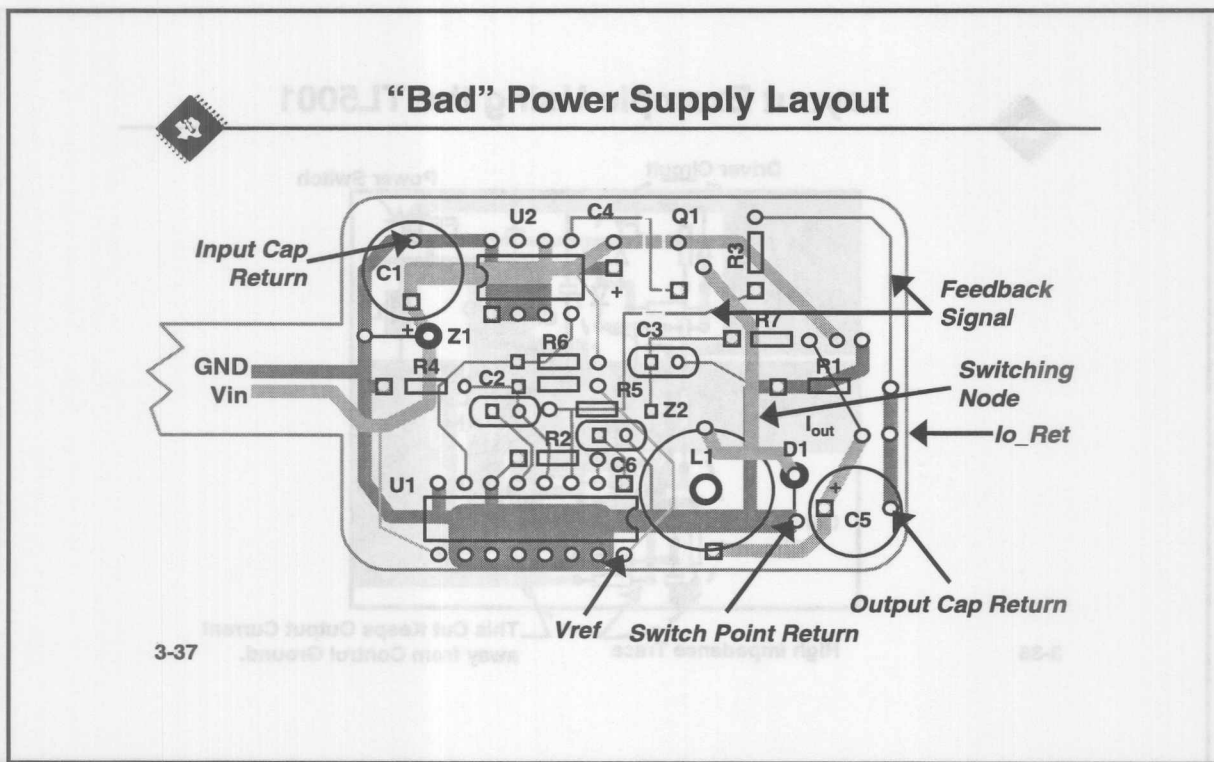
### Layout Example Using the TL5001



3-36

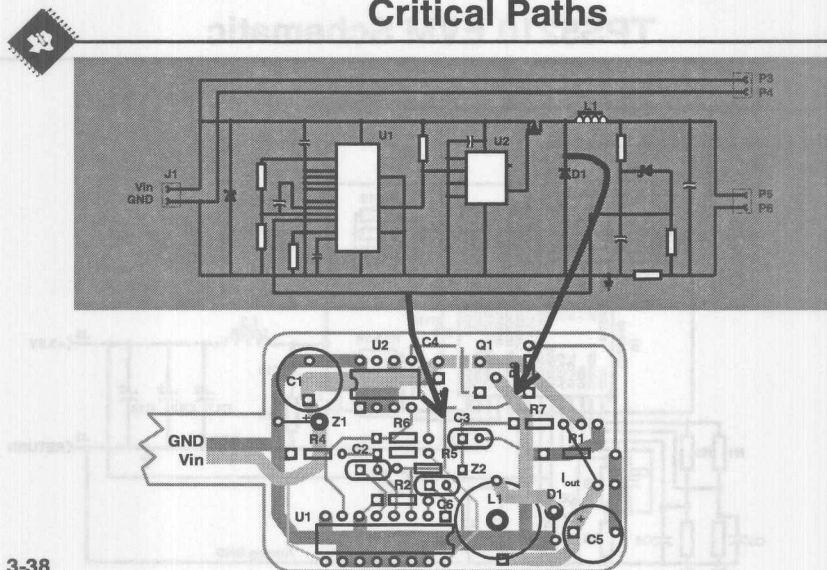
### Power Supply Layout Example

This figure shows a layout example using the TL5001. This circuit is a low-current, step-down converter. Note the tight loop in the area where the highest currents flow: from the input capacitor, through the clamp diode, and in the output capacitors. Getting this area tightly spaced will help greatly in keeping your circuit noise free. Note also the cut in the ground between the output capacitors and the control circuitry; this keeps output current from flowing in the control section reducing noise and load-induced regulation errors. The junction of output divider resistors and the input of the controller (pin 4) is a high-impedance junction that should be kept as short as possible and as far away from noise as possible. The top of the divider resistor is low impedance and can be longer as shown above.



This is an example of doing everything wrong. The high current paths are long with not heavy enough traces. The feedback signal is a very long path that snakes all over the high current node.

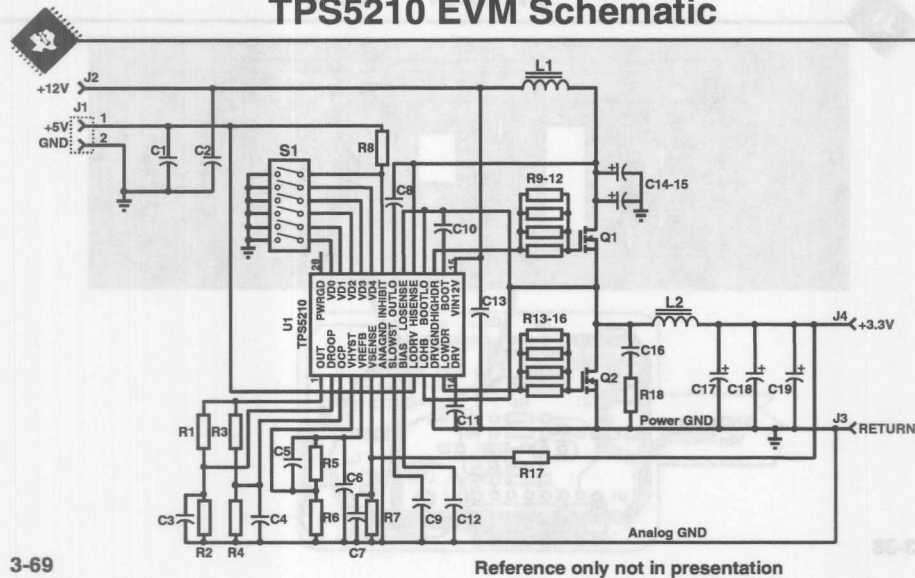
### Critical Paths



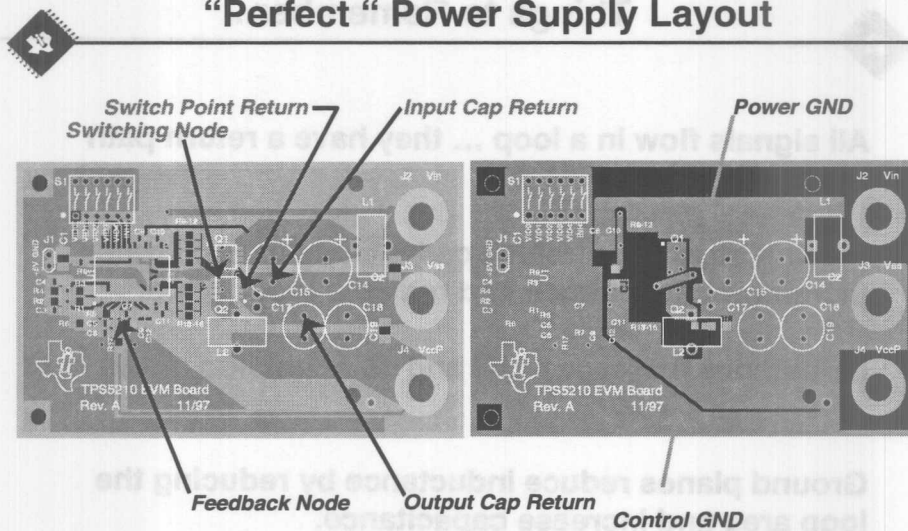
3-38

This figure further illustrates the poor layout by showing the correspondence between the layout and the schematic for the critical signals.

# TPS5210 EVM Schematic



## “Perfect “ Power Supply Layout



3-70

Reference only not in presentation



### Things to Remember...

---

**All signals flow in a loop ... they have a return path somewhere.**

**Placing signal and return paths close to each other increases capacitance and reduces inductance.**

**Inductance increases EMI and is a function of the loop area.**

**Ground planes reduce inductance by reducing the loop area and increase capacitance.**

3-39



### In Power Supply Layouts....

---

***COPPER IS  
OUR FRIEND***

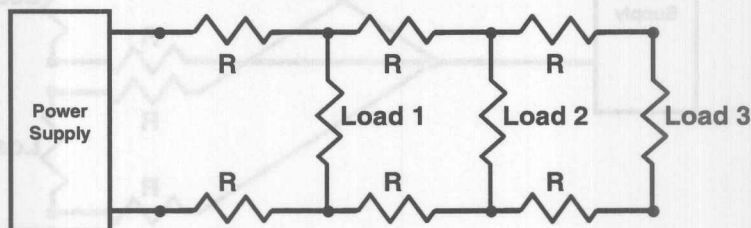
*(In Most Cases)*

3-40

## Parallel Power Distribution

Parallel Distribution of power generally provides a simpler layout, and may reduce routing requirements.

Parallel Voltage Drops ( $VD_p$ )  
Load 3  $VD >$  Load 2  $VD >$  Load 1  $VD$



However, each load compounds the voltage droop and amplifies the system noise seen by adjacent loops

3-41

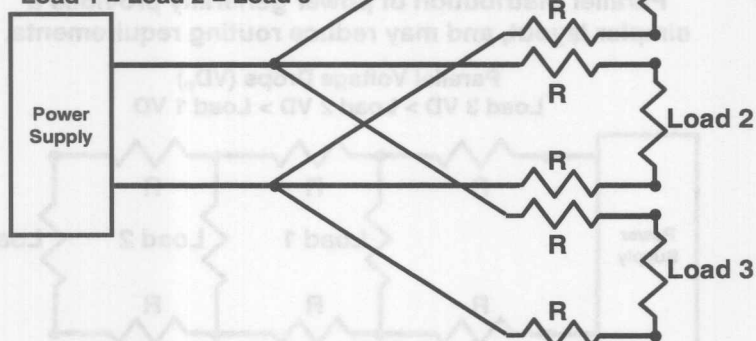
A final consideration in this area is power distribution or routing. System layout is often such that the power supply is on one side of the PWB; power and ground run across the board and the loads are effectively connected in parallel. When this is modeled including conductor resistances it is easy to see that a current transient in load 3 can cause voltage droop across load 1 and load 2.

### Radial Power Distribution



In a Radial power distribution scheme, each load feeds directly off the main supply

Radial Voltage Drops ( $VD_R$ )  
Load 1 = Load 2 = Load 3



This provides better transient response, noise response, ripple rejection, and better tolerancing

3-42

A star or radial power distribution system is shown in the figure above. This method has the advantage that each load has a direct path back to the power supply. None of the loads share a significant conductor resistance  $R$ . The result is that any current transient caused by a load is coupled directly back to the power supply. If the power supply can adequately supply the transient with any voltage droop then the other loads are not affected. This method can also be employed when connecting loads to bulk capacitance.

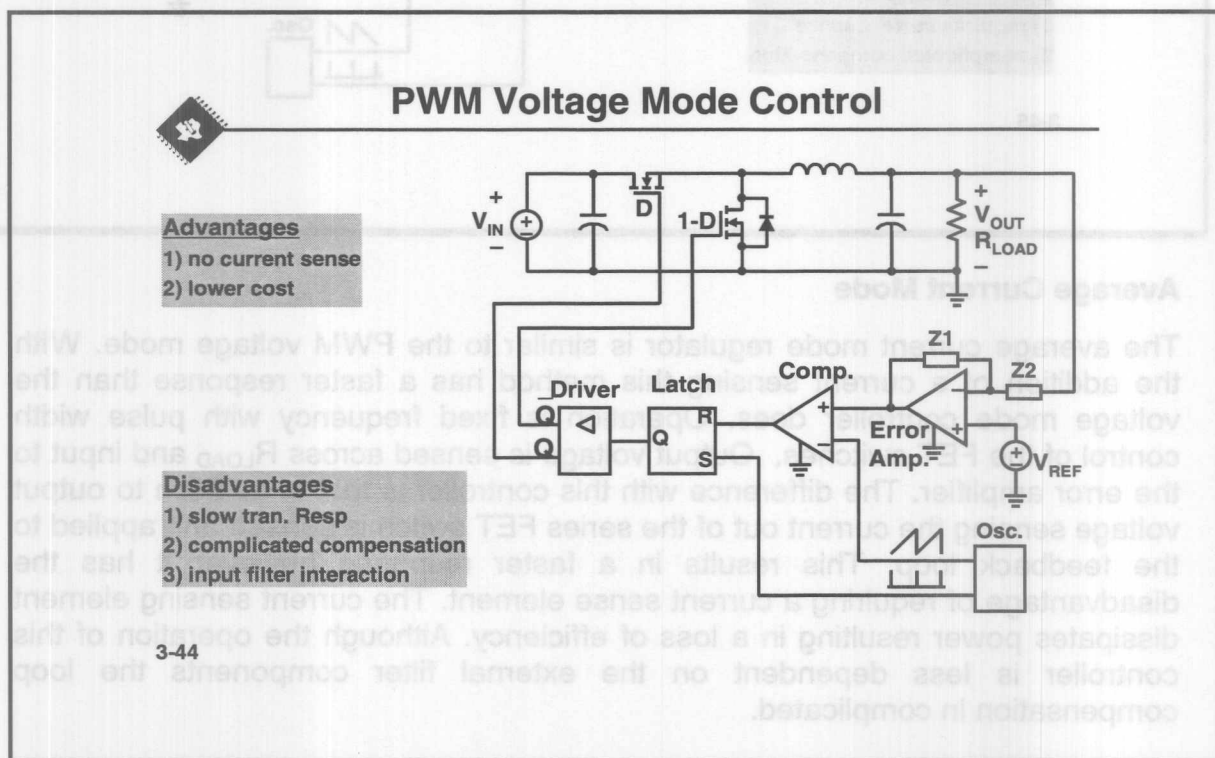
Often times radial connections are not possible, however one solution would be to place all high current loads such as processors in a radial configuration.

## Ripple Regulators

### Overview

Ripple regulators represent a high performance class of switching power supplies. The ripple or hysteretic controller offers fast response times without some of the other disadvantages associated with other switching regulator topologies.

This section will describe several switching topologies with their advantages and disadvantages relative to processor power requirements. The topologies discussed will be: PWM voltage mode, average current mode, peak current mode,  $V^2$  mode, and ripple mode. They will be discussed in order of transient response speed.



### Voltage Mode Control

The first switching topology considered in this discussion is the PWM voltage mode controller. This circuit operates at a constant frequency and varies the width of the drive signals to the FET switches to control the output. The output voltage is sensed across the load  $R_{LOAD}$  the feedback path is into an error amplifier, which then serves to vary the pulse width of the latch reset.

This method has the advantages of a simple circuit, which does not require current sensing and is relatively inexpensive.

The feedback is voltage and not current, fast current transients are not detected and the overall circuit response is slow. Compensation of the feedback system is complicated and the input filter affects the circuit operation.

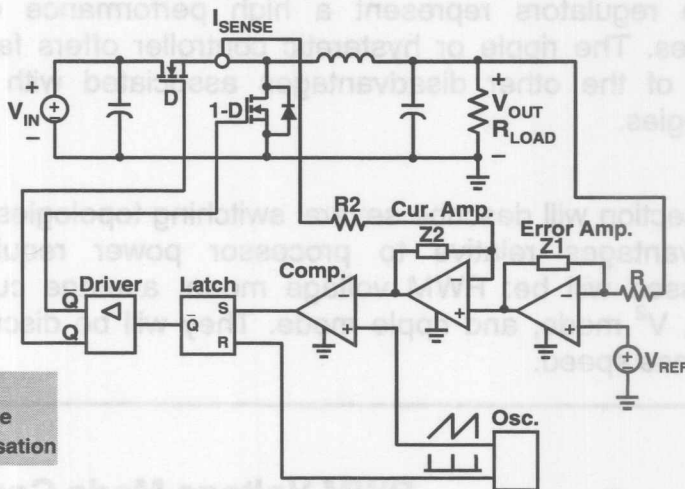
## Average Current Mode Control

### Advantages

- 1) no high frequency current instabilities
- 2) larger  $V_{IN}$  range
- 3)  $V_{IN}$  feed-forward (improved line reg)

### Disadvantages

- 1) requires current sense
- 2) complicated compensation



3-45

## Average Current Mode

The average current mode regulator is similar to the PWM voltage mode. With the addition of a current sensing this method has a faster response than the voltage mode controller does. Operation is fixed frequency with pulse width control of the FET switches. Output voltage is sensed across  $R_{LOAD}$  and input to the error amplifier. The difference with this controller is that in addition to output voltage sensing the current out of the series FET switch is sensed and applied to the feedback loop. This results in a faster response however it has the disadvantage of requiring a current sense element. The current sensing element dissipates power resulting in a loss of efficiency. Although the operation of this controller is less dependent on the external filter components the loop compensation is complicated.

## Peak Current Mode Control

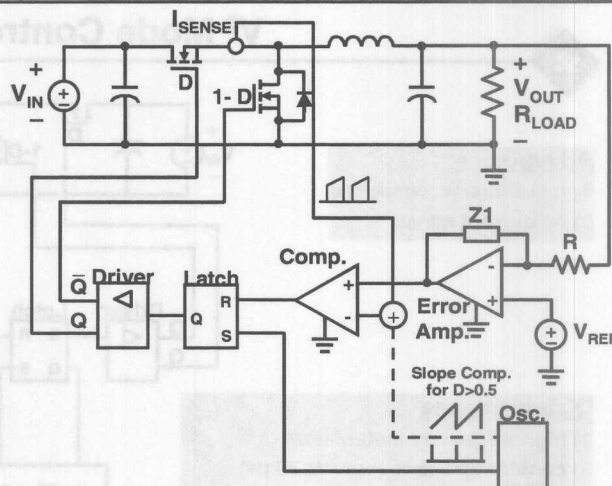
### Advantages

- 1) simpler compensation
- 2) larger  $V_{IN}$  range
- 3)  $V_{IN}$  feed-forward (Improved line reg)

### Disadvantages

- 1) requires current sense
- 2) high freq  $I$  instability
- 3) input filter interaction
- 4) subharmonic oscillations (req. slope compensation)

3-46



## Peak current sensing

This controller is again similar to the previous controller (average current mode). Both a voltage and current feedback loop are employed however in this mode the current feedback is used to control the oscillator output slope. Peak current mode provides increased response speed in addition to the advantages of the average current mode controller. The compensation for this controller is simpler than that for the average current mode. This controller normally operates in the 250kHz range and does have the advantages of some high frequency instabilities.

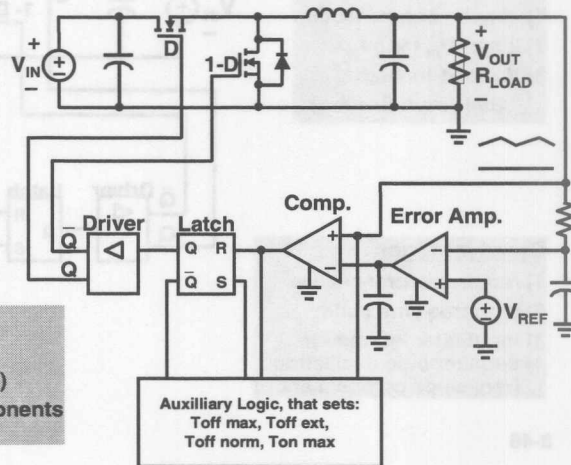
## V<sup>2</sup> Mode Control

### Advantages

- 1) fast transient response
- 2) no current sense

### Disadvantages

- 1) high frequency instabilities
- 2) constant off-time (approx 20  $\mu$ s)
- 3) frequency dependent on components and operating conditions



3-47

## V<sup>2</sup> mode

This patented mode is faster than any of the modes discussed previously. It has no current feedback therefore improving efficiency. The feedback is voltage sensed across the load, however the difference between the V<sup>2</sup> and the voltage mode is that a dual feedback path is provided. One path is directly into the comparator the other path is through a low pass filter into an error amplifier. This controller has a variable frequency operation controlled by the changes in the output voltage. The disadvantages of this control method are high frequency instabilities, which require additional external logic for proper operation. This system is very dependent on the output filter characteristics.

## Hysteretic (Ripple) Mode Control



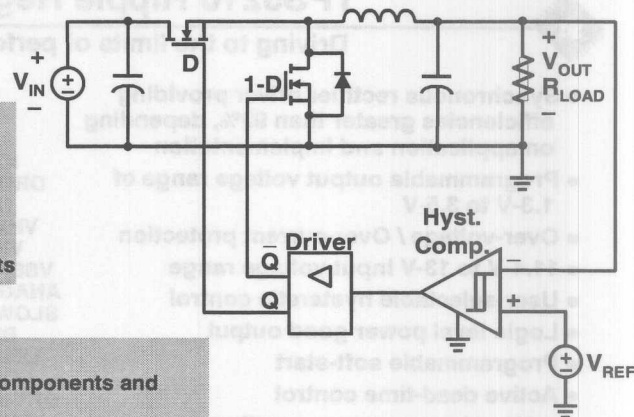
### Advantages

- 1) fast transient response
- 2) no current sensing
- 3) no compensation ckts
- 4) no input filter interaction
- 5) low droop during transients

### Disadvantages

- 1) frequency dependent on components and operating conditions
- 2) high frequency instabilities (noise sensitivity)  
(TPS52xx has internal circuits to address this)

3-48



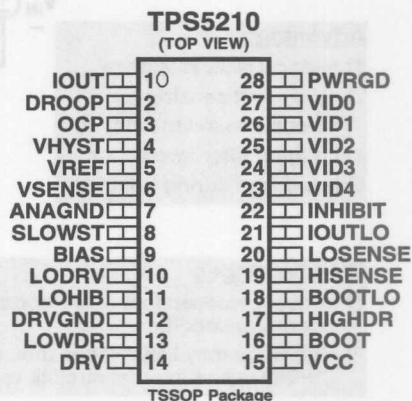
## Hysteretic (Ripple) mode control

The ripple mode is the fastest of the five controller typologies discussed in this section. This method uses voltage feedback into a comparator, which has hysteresis. The sensed voltage is compared to a reference voltage and controls the switching of the FETs as the output changes between the limits of the comparator hysteresis. This is a variable frequency controller, which typically operates in the 300-350 kHz range. High efficiencies can be obtained since no current sensing element is needed. No compensation circuits are needed and the circuit is not sensitive to the input filter. The disadvantages include interaction with the output filter and some high frequency instabilities.

## TPS5210 Ripple Regulator

Driving to the limits of performance

- Synchronous rectifier driver providing efficiencies greater than 92%, depending on application and implementation
- Programmable output voltage range of 1.3-V to 3.5-V
- Over-voltage / Over-current protection
- 11.4-V to 13-V input voltage range
- User-selectable hysteretic control
- Logic level power good output
- Programmable soft-start
- Active dead-time control
- $\pm 1\%$  reference over operating temperature range
- Droop compensation improves load transient regulation



3-49

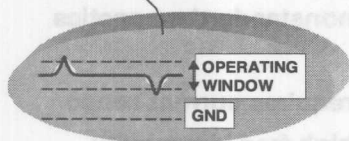
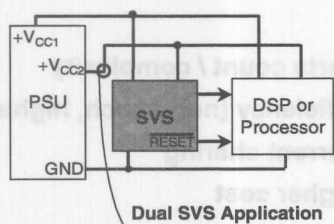
### TPS5210 Ripple regulator

Considering the various topologies of switching regulator the ripple regulator has the fastest response time and provides significant advantages for a processor power supply. The TPS5210 is the first of a series of advanced ripple regulators from Texas Instruments. Key features include programmable output voltage, selectable hysteretic control, and 1% reference accuracy. The TPS5210 includes internal compensation to eliminate high frequency instabilities. The internal circuitry also prevents over regulation that can occur in other controller modes. The output frequency and circuit operation is dependent on the characteristics of the output filter capacitor, specifically the ESR.

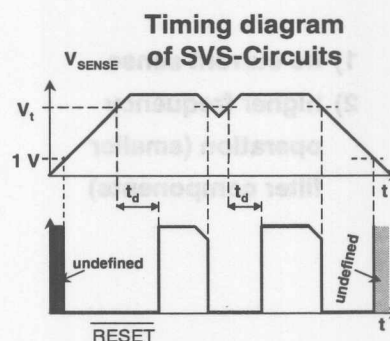
## Regulator Mode Comparison

| <u>Topology</u>              | <u>Advantages</u>                                                                                                                                                                                                            | <u>Disadvantages</u>                                                                                                                                                                                                                                          |
|------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>V-mode</b>                | <ol style="list-style-type: none"> <li>1) no current sense</li> <li>2) lower cost</li> </ol>                                                                                                                                 | <ol style="list-style-type: none"> <li>1) slow tran. Resp</li> <li>2) complicated compensation</li> <li>3) input filter interaction</li> </ol>                                                                                                                |
| <b>Interleaved V-mode</b>    | <ol style="list-style-type: none"> <li>1) no current sense</li> <li>2) higher frequency operation (smaller filter components)</li> </ol>                                                                                     | <ol style="list-style-type: none"> <li>1) parts count / complexity</li> <li>2) efficiency (non-synch, higher frequency)</li> <li>3) current sharing</li> <li>4) higher cost</li> <li>5) input filter interaction</li> <li>6) nonstandard magnetics</li> </ol> |
| <b>peak I-mode</b>           | <ol style="list-style-type: none"> <li>1) simpler compensation</li> <li>2) larger <math>V_{IN}</math> range</li> <li>3) <math>V_{IN}</math> feed-forward (improved line reg)</li> </ol>                                      | <ol style="list-style-type: none"> <li>1) requires current sense</li> <li>2) high freq I instability</li> <li>3) input filter interaction</li> <li>4) subharmonic oscillations (requires slope compensation)</li> </ol>                                       |
| <b>avg I-mode</b>            | <ol style="list-style-type: none"> <li>1) no high frequency current instabilities</li> </ol>                                                                                                                                 | <ol style="list-style-type: none"> <li>1) requires current sense</li> <li>2) complicated compensation</li> </ol>                                                                                                                                              |
| <b><math>V^2</math> mode</b> | <ol style="list-style-type: none"> <li>1) fast transient response</li> <li>2) no current sense</li> </ol>                                                                                                                    | <ol style="list-style-type: none"> <li>1) high frequency instabilities</li> <li>2) constant off-time (approx. 20 <math>\mu</math>s)</li> <li>3) frequency dependent on components and operating conditions</li> </ol>                                         |
| <b>Ripple</b>                | <ol style="list-style-type: none"> <li>1) fast transient response</li> <li>2) low droop during transients</li> <li>3) no current sensing</li> <li>4) no compensation ckts</li> <li>5) no input filter interaction</li> </ol> | <ol style="list-style-type: none"> <li>1) frequency dependent on components and operating conditions</li> <li>2) high frequency instabilities (noise sensitivity) (TPS5210 has internal circuits to address this)</li> </ol>                                  |

## SVS Application and Timing



3-51



### Supply Voltage Supervisors

In order to ensure the reliable operation of a digital system, it is important that the circuits of which it is composed should have a clearly defined initial state. With microcomputers and microprocessors, this initial state is implemented with a reset signal. This ensures that the system is only switched into an active state when the supply voltage has reached its nominal value. In the same way, a break down of the supply voltage affects the operation of integrated circuits and can result in faulty operation.

In order to avoid such problems, a circuit is needed which will generate a defined reset signal. The simplest way of implementing this is with the help of a RC network at the RESET input.

The voltage at the RESET input rises with a delay determined by the time constant  $t = R \times C$ , until the threshold value of the RESET input has been reached. At this point, the system is switched into an active state.

This method of generating the reset pulse is however not very reliable, since the reset time depends on the boundary conditions of the power supply and of the complete system.

Since this circuit only fulfills (with some reservations) the requirements for a reliable system reset, more extensive precautions must be taken to exclude faults of this kind.

The following requirements must thus be fulfilled:

- The reset signal must be applied long enough for the supply voltage to have reached its nominal value.
- After the nominal supply voltage has been reached, the reset signal must stay active for a certain time, in order to ensure error free initialization and correct operation of the system.
- The reset signal must again initialize the system, should the supply voltage go below the minimum permissible value.

For these applications, Texas Instruments has developed a range of **Supply Voltage Supervisors** that meet the above requirements.

### Supply Voltage Supervisor Selection Guide

#### Supply Voltage Supervisors

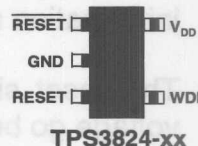
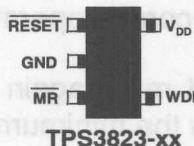
| Product Family | Sense Input | Sense Thres | % Toler. | Output Config. | Remarks                                      |
|----------------|-------------|-------------|----------|----------------|----------------------------------------------|
| TL7702A        | Prog        | 2.5 V       | 1        | Open Collector | $I_Q = 1\text{mA TYP}$                       |
| TL7705A        | 5 V         | 4.55 V      | 1        | Open Collector |                                              |
| TL7709A        | 9 V         | 7.6 V       | 1        | Open Collector |                                              |
| TL7712A        | 12 V        | 10.8 V      | 1        | Open Collector |                                              |
| TL7715A        | 15 V        | 13.5 V      | 1        | Open Collector |                                              |
| TL7702B        | Prog        | 2.53 V      | 1        | Open Collector | $I_Q = 1\text{mA TYP}$                       |
| TL7705B        | 5 V         | 4.55 V      | 1        | Open Collector |                                              |
| TL7757         | 5 V         | 4.55 V      | 2.6      | Open Collector | Only Reset, 3-Pin<br>$I_Q = 45\text{mA TYP}$ |
| TL7759         | 5 V         | 4.55 V      | 2.6      | Open Collector |                                              |
| TL7770-5       | 5 V         | 4.55 V      | 1        | Open Collector | $I_Q = 3\text{mA TYP}$<br>Duals              |
| TL7770-12      | 12 V        | 10.9 V      | 1        | Open Collector |                                              |
| TL7770-15      | 15 V        | 13.64 V     | 1        | Open Collector |                                              |
| TLC7701        | Adj         | 1.1 V       | 1        | Totem Pole     | $I_Q = 10\mu\text{A TYP}$                    |
| TLC7725        | 2.5V        | 2.28V       | 1        | Totem Pole     |                                              |
| TLC7730        | 3.0V        | 2.78V       | 1        | Totem Pole     |                                              |
| TLC7733        | 3.3 V       | 3.08 V      | 1        | Totem Pole     |                                              |
| TLC7705        | 5 V         | 4.55 V      | 1        | Totem Pole     |                                              |

3-52

## TPS382X: Supply Voltage Supervisors

### Device Features

- Power-on reset generator
- 2.5 V, 3.0 V, 3.3 V, 5.0 V options
- Fixed 200ms delay time
- Watchdog Timer
- Manual Reset input (TPS3823-xx)
- 25  $\mu$ A supply current
- No external components
- SOT-23 Package



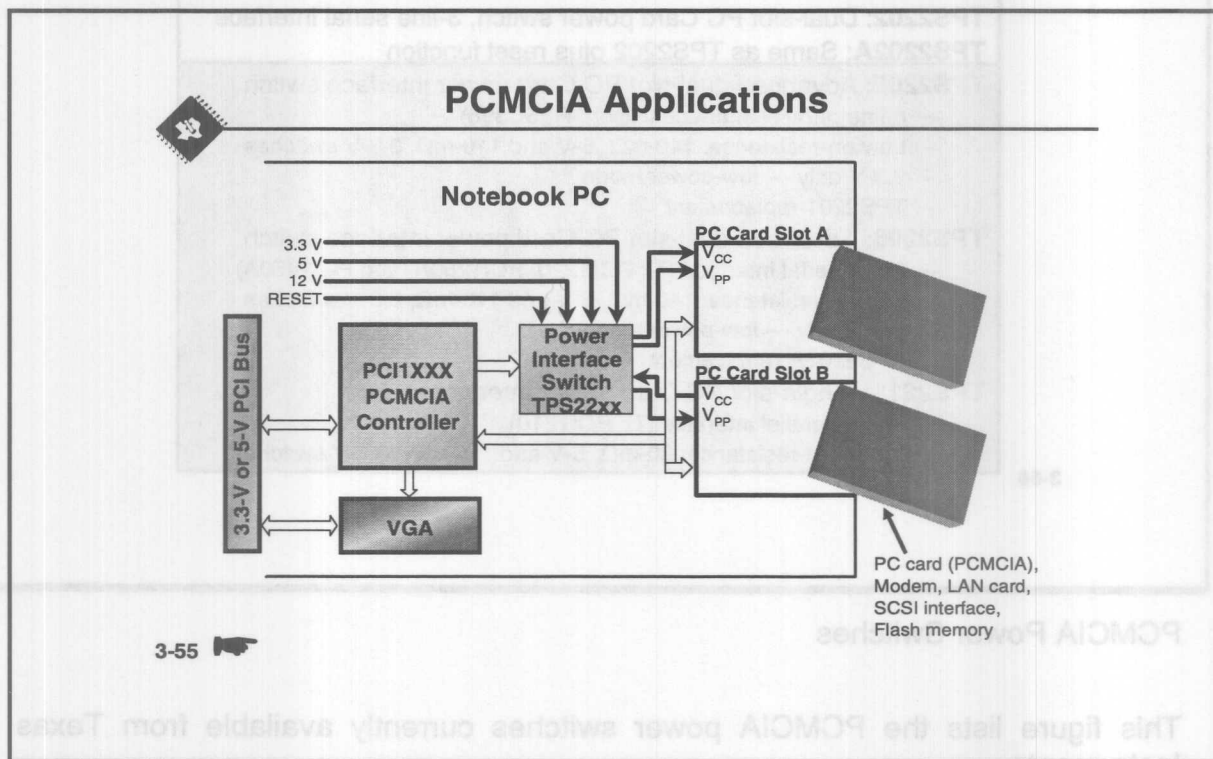
| Product Family | Sense Input | Sense Thres | % Toler. | Output Config. | Remarks             |
|----------------|-------------|-------------|----------|----------------|---------------------|
| TPS3823-25     | 2.5V        | 2.25V       | 1        | Totem Pole     | Watch-dog interrupt |
| TPS3823-30     | 3.0V        | 2.83V       | 1        | Totem Pole     | No ext. cap req.    |
| TPS3823-33     | 3.3V        | 2.93V       | 1        | Totem Pole     | Manual reset on     |
| TPS3823-50     | 5.0V        | 4.55V       | 1        | Totem Pole     | TPS3823 family      |

3-53

The newest member of the supply voltage supervisors are the TPS3823-xx supervisors feature integrated watchdog timers and are available in the SOT-23 package.

## Power Distribution

This section will deal with power distribution products. This refers to the control of power as it is distributed to various parts of a system. Power distribution systems are used for functions such as: energy conservation, "hot plugging" of system components, and device protection.



## PCMCIA Power Distribution Application

A PCMCIA or card bus application is usually associated with laptop PCs but can be found on point of sale terminals, digital cameras etc. The PCMCIA power system must deliver 3.3V, 5V, and 12V depending on the specific card requirements. When a card is plugged into the card slot the card indicates what voltages are required for operation. An example is a flash memory card which needs 12V but only when it is being written to. The other requirement is that the cards must be plugged and unplugged with system power on and not damage either the card or the system. The complete PCMCIA power distribution system includes both the digital controller which interfaces the power control and status information to the host and the power switches to control the power to the card.

## PCMCIA Power Switches



**TPS2201:** Dual-slot PC Card power switch, parallel interface

**TPS2202:** Dual-slot PC Card power switch, 3-line serial interface

**TPS2202A:** Same as TPS2202 plus reset function

**TPS2205:** Advanced dual-slot PC Card power interface switch

- 8-line parallel interface (Ricoh: RF5C396)
- Low on-resistance: 140-m $\Omega$ , 5-V and 110-m $\Omega$ , 3.3-V switches
- 3.3-V only — low-power mode
- TPS2201 replacement

**TPS2206:** Advanced dual-slot PC Card power interface switch

- 3-line serial interface (TI: PCI1220, PCI1250A, and PCI1450A)
- Low on-resistance: 140-m $\Omega$ , 5-V and 110-m $\Omega$ , 3.3-V switches
- 3.3-V only — low-power mode
- TPS2202A replacement

**TPS2211:** Single-slot PC Card power interface switch

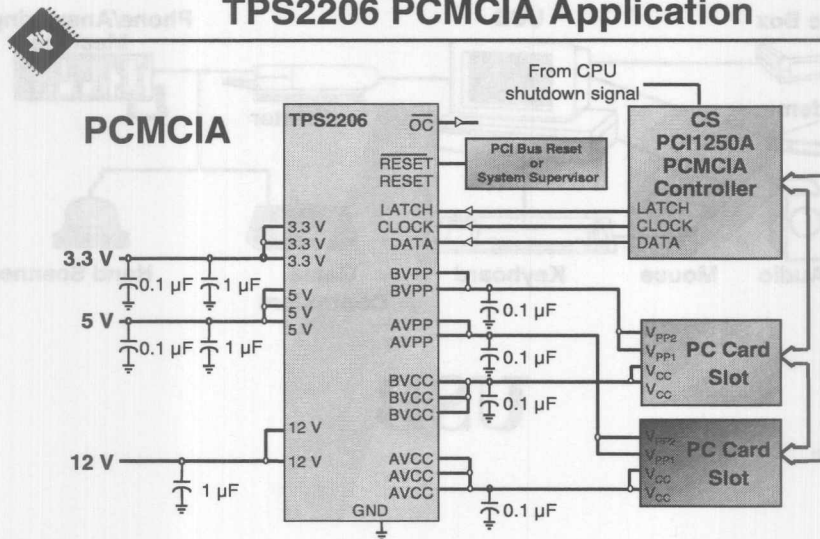
- 4-line parallel interface (TI: PCI1210)
- Lower on-resistance: 90-m $\Omega$ , 5-V and 110-mW, 3.3-V switches

3-56

## PCMCIA Power Switches

This figure lists the PCMCIA power switches currently available from Texas Instruments.

## TPS2206 PCMCIA Application

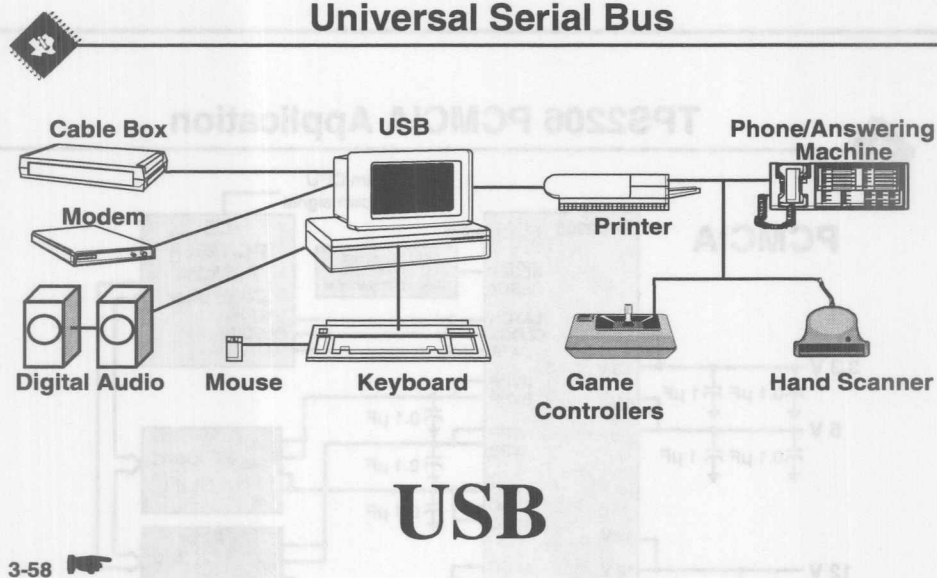


3-57

### PCMCIA Application

The figure above is a complete PCMCIA power distribution application. The PCI1250A controller interfaces with the host and the TPS2206 power switch.

## Universal Serial Bus



3-58

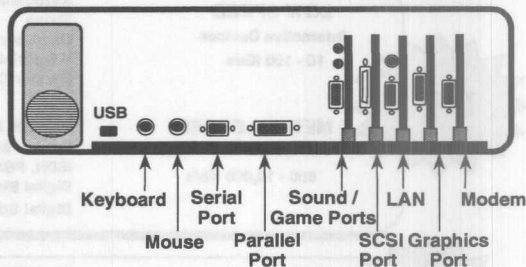
### Universal Serial Bus Power

The Universal Serial Bus (USB) is a self-powered, medium speed data bus commonly associated with PCs. USB is a 12 mbps data & power bus which utilizes four wires. USB provides "hot plugging" for both hardware and software. A USB peripheral can be plugged into the host and will receive operating power over the bus and is automatically software configured into the system.

## PC Connectivity Today and Tomorrow

### USB in 1996:

Initially introduced as an incremental add-on for new applications



### USB Future:

The PC evolves into a simpler, easier appliance type system.

Telephony, Modem, Keyboard  
Mouse, Game ports, Serial  
ports Device, Digital Audio,  
Printer, Scanner





3-59

## PC Connectivity

Today the back of a PC is a maze of connectors each providing interface to a unique peripheral. The future configuration of many PCs will consist of only USB and 1394 interfaces which will serve all of the peripherals.

## Serial Bus Solutions - USB & 1394

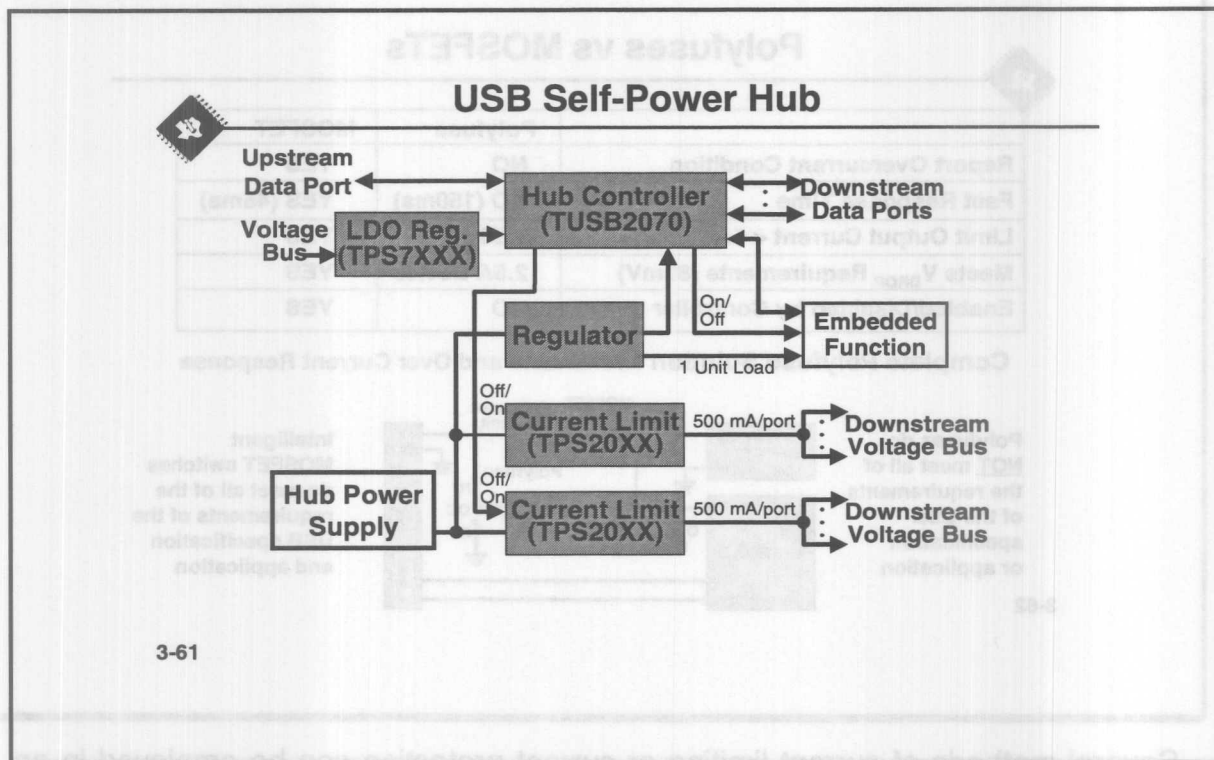
|                                                                                                  | PERFORMANCE                                                         | APPLICATIONS                                                                                                                  | ATTRIBUTES                                                                                                          |
|--------------------------------------------------------------------------------------------------|---------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|
| <br><b>USB</b>  | <b>LOW SPEED</b><br>Interactive Devices<br>10 - 100 Kb/s            | Keyboard, Mouse<br>Stylus<br>Game peripherals<br>V R peripherals<br>Monitor Control                                           | Lower cost<br>Hot plug-unplug<br>Easy of use<br>Multiple peripherals                                                |
|                                                                                                  | <b>MEDIUM SPEED</b><br>Phone, Audio, Bulk Data<br>500 - 10,000 Kb/s | ISDN, 28.8, DSVD Modems<br>Printer, Scanner, Fax<br>ISDN, PBX, POTS Telephony<br>Digital Stereo Audio<br>Digital Still Camera | Low cost<br>Ease of use<br>Guaranteed latency<br>Guaranteed Bandwidth<br>Dynamic Attach- Detach<br>Multiple devices |
| <br><b>1394</b> | <b>HIGH SPEED</b><br>Video, Disk, LAN<br>100 - 400 + Mb/s           | Hard Disk, CD-ROM, DVD<br>Set Top Box<br>Digital Video Monitor<br>Home Networks                                               | High Bandwidth<br>Guaranteed latency<br>Real-Time Data                                                              |

With USB and 1394, standard 2-way digital communication links, the paradigm of PC Peripherals is destined to change

3-60

This comparison shows the performance differences between USB and PCI interfaces as well as typical peripheral applications.

Texas Instruments makes components to support both of these standards.



### Self Powered USB Hub Application

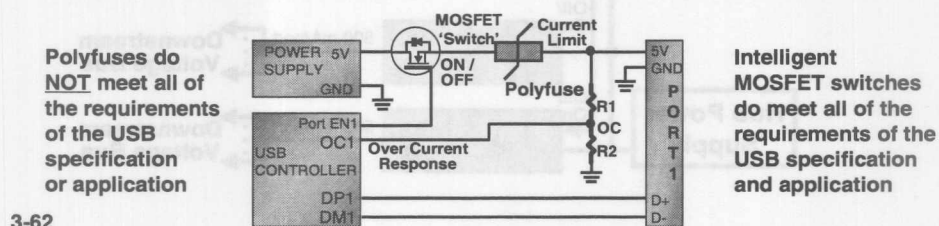
This figure shows the power distribution circuitry needed to implement a self-powered USB hub. Voltage is provided from the bus and regulated at the hub by a TPS7xxx LDO regulator. A LDO is used due to the fact that the bus voltage can be as low as 4.1-4.2V depending on the connection to the bus. The TUSB2070 hub controller interfaces the power control signals to the data bus. Current limit must be provided to each of the hub ports. Both power switching and current limiting are provided by TPS20xx switches.

Current limiting is required to protect both the hub and any circuit, which is connected to the hub port.

# Polyfuses vs MOSFETs

|                                      | Polyfuse    | MOSFET     |
|--------------------------------------|-------------|------------|
| Report Overcurrent Condition         | NO          | YES        |
| Fast Response Time                   | NO (150ms)  | YES (45ms) |
| Limit Output Current < 5A            | YES         | YES        |
| Meets $V_{DROP}$ Requirements (80mV) | 2.5A Device | YES        |
| Enabled/Disabled by Controller       | NO          | YES        |

## Complete Polyfuse Solution with Enable and Over Current Response



Several methods of current limiting or current protection can be employed in an application such as USB. One device used is the polyfuse. The polyfuse uses a positive temperature coefficient carbon granule structure. When the device temperature reaches its limit the impedance increases to a very large value. When the device cools the internal resistance returns to the nominal value. The disadvantages of this device are response time and the fact that the internal resistance causes a loss of power and thus reduces efficiency. Another issue is that polyfuses alone do not meet all the USB specification and must be combined with a MOSFET switch for the total solution.

Conventional fuses can also be used for current limiting. They also have a time response problem and will require replacement after each overcurrent event.

## TPS2044 USB Application

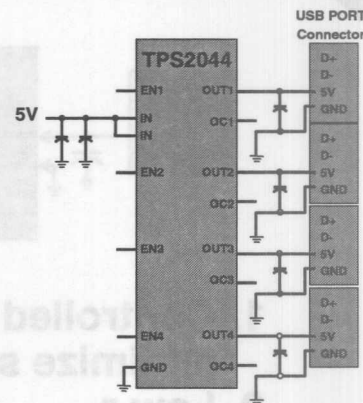


### Truly Independent Switches

- Independent Enables
- Independent Over Current Response
- Independent Over Temperature Function

135mΩ max  $r_{DS(on)}$

Controlled Rise And Fall Time



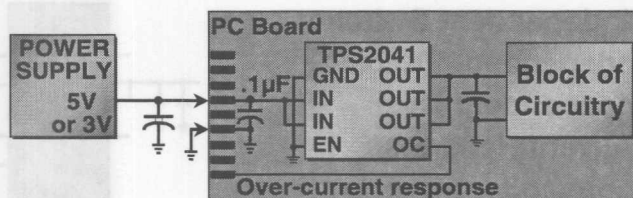
### Maintenance Free Power Distribution

3-63


### TPS2044 USB Power Application.

The TPS2044 contains four MOSFET power switches. Each switch is independently controlled and has a separate over current and over temperature function, allowing a single switch to be shut off without turning power off to all four channels. This product uses MOSFET switches for both power control and over current control giving fast response and no maintenance. The switches have controlled rise and fall times to minimize supply line transients.

## Hot-Plug Applications



1. Controlled switch rise times minimize surge currents
2. Low  $r_{DS(on)}$  minimizes voltage drops

3-66 

One final general-purpose application is for any system requiring "hot plugging". The basic requirement for this application is to be able to apply and remove power to a circuit without damage to the circuit or transients to the host supply. The TPS2041 can switch the power with controlled rise and fall times in addition to over current protection.



**Texas Instruments**  
**“Helping you make POWER MANAGEMENT**  
**one of your first decisions instead of the last,**  
**by making it simple”**

3-68

### **TI's USB Product Portfolio**



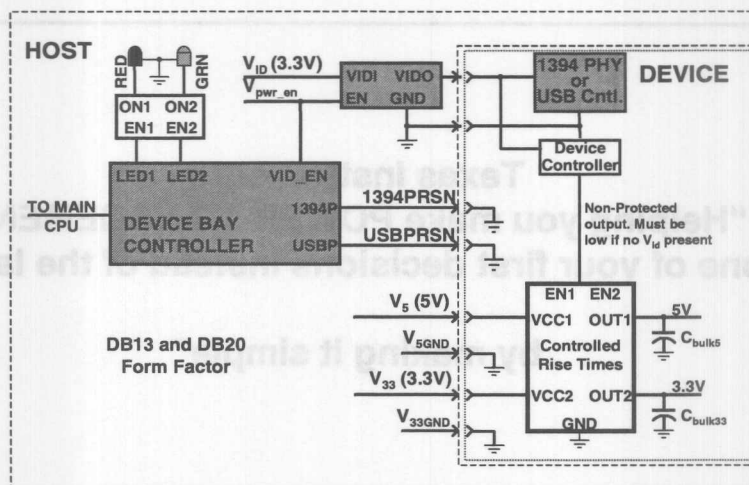
➤ Products & Samples Available Now:

- **TUSB2040 Chips & EVM - 4 Port USB Hub**
- **TUSB2070 Chips & EVM - 7 Port USB Hub**
- **TUSB2140 - 4 Port Hub with I<sup>2</sup>C Interface**
- **TPS2014/15 - Power Distribution Switches**
- **SN75240 - Dual Port Transient Suppressor**
- **TPS7133 - 3.3V Dropout Voltage regulator**

Not only does TI offer a Broad-Based Family of USB Products,  
TI is the only SC vendor offering a complete Hub solution

3-65 

## Device Bay Applications





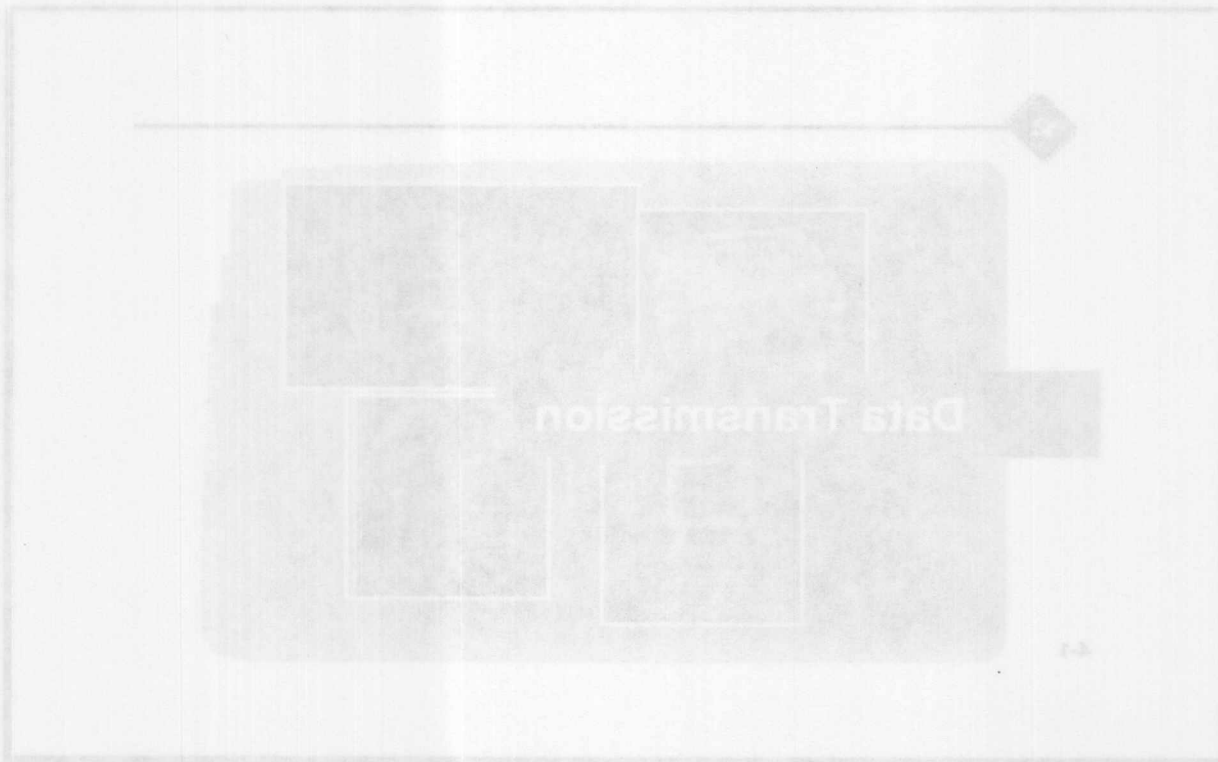
**Texas Instruments**  
**“Helping you make POWER MANAGEMENT**  
**one of your first decisions instead of the last,**  
**by making it simple”**

3-68



## Data Transmission

4-1



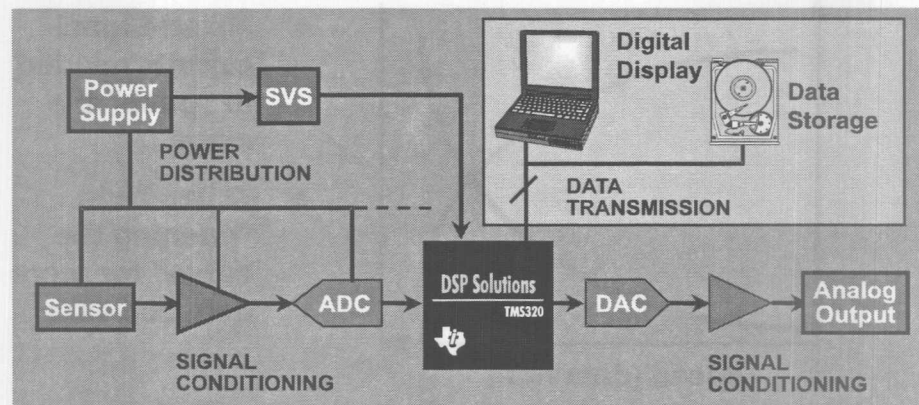
## Table of Contents

|                                                        |           |
|--------------------------------------------------------|-----------|
| <b>What is Data Transmission?</b> .....                | <b>5</b>  |
| Data transmission tradeoffs .....                      | 6         |
| Why follow standards?.....                             | 7         |
| <b>ANSI Standards</b> .....                            | <b>8</b>  |
| ANSI standard physical layer .....                     | 8         |
| ANSI standard parameters.....                          | 10        |
| TIA/EIA-232-F .....                                    | 10        |
| TIA/EIA-422-B and TIA/EIA-485A.....                    | 11        |
| TIA/EIA 644.....                                       | 11        |
| <b>Low Voltage Differential Signaling (LVDS)</b> ..... | <b>12</b> |
| LVDS Definition .....                                  | 12        |
| TIA/EIA-644 .....                                      | 13        |
| Electrical Specifications .....                        | 13        |
| EMI .....                                              | 14        |
| LVDS Benefits .....                                    | 16        |
| Designing with LVDS.....                               | 18        |
| LVDS Products .....                                    | 20        |
| General-Purpose:.....                                  | 20        |
| LVDM: .....                                            | 20        |
| Flatlink: .....                                        | 21        |
| N-Link: .....                                          | 21        |
| <b>RS-232, 422 and 485 Products</b> .....              | <b>28</b> |

## Table of Contents

|                                                 |    |
|-------------------------------------------------|----|
| What is Data Transmission? .....                | 3  |
| Data transmission tradeoffs .....               | 3  |
| Why follow standards? .....                     | 7  |
| ANSI Standards .....                            | 8  |
| ANSI standard physical layer .....              | 8  |
| ANSI standard parameters .....                  | 10 |
| TIA/EIA-232-F .....                             | 10 |
| TIA/EIA-422-B and TIA/EIA-422A .....            | 11 |
| TIA/EIA 644 .....                               | 11 |
| Low Voltage Differential Signaling (LVDS) ..... | 15 |
| LVDS Definition .....                           | 15 |
| TIA/EIA-644 .....                               | 15 |
| Electrical Specifications .....                 | 15 |
| EMI .....                                       | 14 |
| LVDS Benefits .....                             | 16 |
| Designing with LVDS .....                       | 16 |
| LVDS Products .....                             | 20 |
| General Purpose .....                           | 20 |
| LVDM .....                                      | 20 |
| Printed .....                                   | 21 |
| In-Link .....                                   | 21 |
| RS-232, 422 and 485 Products .....              | 22 |

## Data Transmission



4-2

## What is Data Transmission?

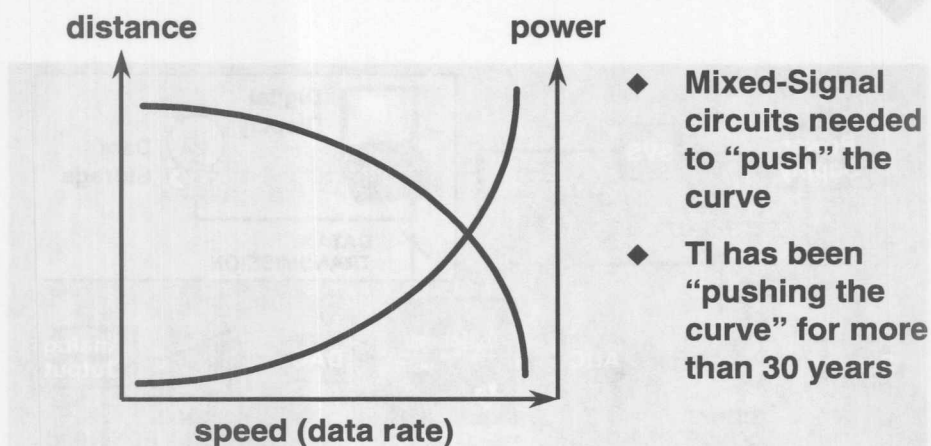
Data Transmission as part of Texas Instruments' Mixed-Signal Product portfolio is concerned with the standards involving transmitting data at relatively high speeds down long line lengths, the considerations for which are primarily of an analog more than a digital nature.

TI has been a leading supplier of data transmission products for many years and is continually providing innovation for new fields. Although the following presentation is limited to the more common interface standards, TI actively is involved in many new emerging standards and markets such as 1394 and PCI bus.

With considerable expertise in design, product definition, and a range of technologies, TI is the ideal choice for supplying your data transmission product requirements. In this section of the seminar we will review the different ANSI standards that exist and we will introduce the new ANSI/TIA/EIA-644 standard, otherwise known as LVDS.



## Data Transmission Tradeoffs



- ◆ Mixed-Signal circuits needed to “push” the curve
- ◆ TI has been “pushing the curve” for more than 30 years

4-4

### Data transmission tradeoffs

The challenge to the designers of data transmission circuits is to balance the tradeoffs between speed, power, and distance. These tradeoffs lead to the need for specialized ICs and technologies. Traditionally, the robustness of bipolar technologies has been utilized; however, the additional need for low power consumption and high levels of integration no longer makes this attractive. Semiconductor (SC) manufacturers now have to develop their technologies to accommodate these requirements. TI has introduced its proprietary LinBiCMOS™ technology, which combines the robustness of bipolar together with the power consumption and integration afforded by CMOS. The results of these technologies are very specialized and reliable products that are able to withstand the harsh environment unique to data transmission products.

## Why Follow Standards?



- **Interchangeability of equipment and components**
  - Lowers component cost through economies of scale and competition
- **Reduced risk and cycle times**
  - Design “by committee” of industry experts is generally very robust
  - Standards live for decades

4-5

### Why follow standards?

Data Transmission Standards evolved for two main reasons: from the need to transmit data reliably over long distances and to provide a standard interface to facilitate communication between equipment from different suppliers.

Semiconductor manufacturers know what specifications to comply with to make catalog devices fully compatible with the standard and enable devices adhering to the standard to communicate. Users then know how to configure the system so the equipment may communicate (cable lengths, signaling rates, etc.).

Since the devices are designed according to a standard, there is lower design risk and a shorter cycle time for the system. The devices are also catalog parts, meaning they are released devices available for purchase today. Catalog components enjoy economies of scale over proprietary devices since everyone in the industry can purchase the devices and through collectively larger volumes, cause lower costs.

FAIL SAFE RESISTORS  
(NEED?)

## ANSI Standards



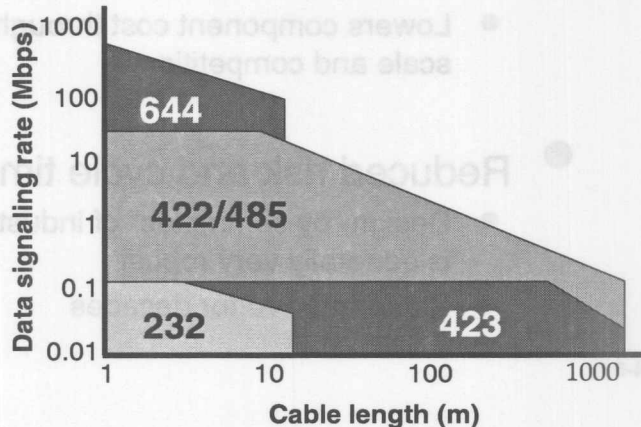
### ANSI Standard Physical Layer

#### Differential

- Long line lengths
- High data rates
- Common mode cancellation

#### Single Ended

- Low data rates
- Poor noise immunity
- Low cost



4-6

### ANSI standard physical layer

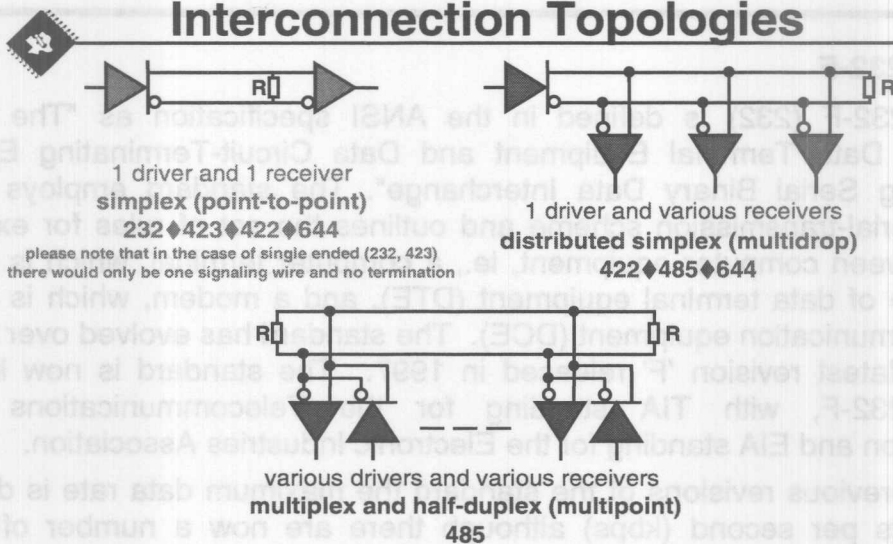
The American National Standard Institution (ANSI) standards cover a wide range of signaling rates and distances. One of the first questions designers must ask themselves when choosing a data transmission standard is how far? and how fast? The above figure shows a general guideline of each transmission standard when comparing data signaling rates and line lengths.

Basically, these standards may be divided into two transmission categories: 1) single-ended (232,423) and 2) differential (422, 485, 644), each one having its advantages and disadvantages.

The advantages of single-ended transmission are simplicity and low cost of implementation. A single-ended system requires one line per signal making it a cost-effective solution for low signaling rates and short distances. The main disadvantage of the single-ended solution is its poor noise immunity. Because the ground wire forms part of the system, transient voltages or shifts in voltage potential may be induced, leading to signal degradation. Crosstalk is also a major concern, especially at high frequencies. These problems will normally limit the distance and speed of reliable operation for a single-ended link.

At high data rates, on long lines or under noisy conditions, differential data transmission has an advantage over single-ended because it is more immune to noise interference. A differential transmission involves using two signal-carrying wires between the driver and the receiver. Any noise induced on one of the lines will also be induced on the other. The receiver is only concerned with the difference between these two signals, and any noise coupled onto the two wires appears as common-mode noise and is rejected. This is true in cases of crosstalk from neighboring signal lines. It is also true for noise from other noise sources as long as the common-mode voltage does not go beyond the common-mode range of the receiver. The common-mode rejection of the receiver eliminates also to a certain degree noise caused by a ground voltage difference between the driver and the receiver. All these advantages come with some drawbacks. Due to the more complex circuit technique required to achieve the high performance these circuits may have a higher cost. Furthermore the high data rate requires well-defined line impedance and a correct line termination to avoid line reflections. Also twisted pair cable instead of inexpensive multi-core cables need to be used.

## Interconnection Topologies



4-7

## ANSI standard parameters



### ANSI Standard Parameters

| Parameter                            | TIA/EIA<br>232-F     | TIA/EIA<br>423-A | TIA/EIA<br>422-B                                  | TIA/EIA 485-A                             | TIA/EIA 644<br>(LVDS)                          |
|--------------------------------------|----------------------|------------------|---------------------------------------------------|-------------------------------------------|------------------------------------------------|
| Mode of Operation                    | Single-Ended         | Single-Ended     | Differential                                      | Differential                              | Differential                                   |
| Transmission Modes                   | Simplex              | Simplex          | Simplex,<br>Distributed<br>simplex<br>(multidrop) | Half-Duplex,<br>Multiplex<br>(multipoint) | Simplex,<br>Distributed Simplex<br>(multidrop) |
| Maximum Cable Length (m)             | 20                   | 1200             | 1200                                              | 1200                                      | 30                                             |
| Maximum Data Rate (bps)              | 20 k                 | 120 k            | 10 M                                              | 50 M                                      | 655 M                                          |
| Maximum Ground<br>Offset Voltage (V) | $\pm 3$              | $\pm 3$          | $\pm 7$                                           | -7 to 12                                  | $\pm 1$                                        |
| Minimum Driver Output Levels (V)     | $\pm 5$              | $\pm 3.6$        | $\pm 2$                                           | $\pm 1.5$                                 | $\pm 0.247$                                    |
| Driver Load ( $\Omega$ )             | 3 k to 7 k           | 450 (Min)        | 100 (Min)                                         | 60 (Min)                                  | 100                                            |
| Driver Slew Rate                     | 30 V/ $\mu$ s (Max.) | NA               | NA                                                | NA                                        | $\sim 2.3$ V/ns                                |
| Receiver Sensitivity (V)             | $\pm 3$              | $\pm 200$ m      | $\pm 200$ m                                       | $\pm 200$ m                               | $\pm 100$ m                                    |

4-8

#### TIA/EIA-232-F

TIA/EIA-232-F (232) is defined in the ANSI specification as "The Interface Between Data Terminal Equipment and Data Circuit-Terminating Equipment Employing Serial Binary Data Interchange". The standard employs a single ended serial-transmission scheme and outlines the set of rules for exchanging data between computer equipment, ie., a computer terminal, which is classified as a type of data terminal equipment (DTE), and a modem, which is a type of data communication equipment (DCE). The standard has evolved over the years with the latest revision 'F' released in 1997. The standard is now known as TIA/EIA-232-F, with TIA standing for the Telecommunications Industry Association and EIA standing for the Electronic Industries Association.

As with previous revisions of the standard the maximum data rate is defined as 20 kilobits per second (kbps) although there are now a number of software applications that push this data rate above 200 kbps, well outside the standard. The maximum line length for a 232 connection is defined in terms of load capacitance. The maximum load capacitance is specified as 2500 pF, which indicates the uses of standard cables between 15 and 20 meters long. Line length and signaling rates are limited, as the standard employs single-ended communication that is prone to external factors.

**TIA/EIA-422-B and TIA/EIA-485A**

TIA/EIA-422-B (422) specifies a balanced transmission circuit whose maximum line length is undefined but is nominally 1.2 km for 24-AWG cable, based on 6-dB signal attenuation. The maximum signaling rate also is undefined but is specified by the relationship of signal rise time to bit time, which is influenced by the line driver, the line length, and the line loading. In the majority of applications, it is the line length that is the limiting factor on signaling rate due to signal dispersion. TIA/EIA-485-A (485) is primarily an upgrade to the 422 standard which allows half-duplex and multiplex transmission modes. It specifies only the electrical layer of the transmission scheme, and hardware such as the connector is left to the user to define.

**TIA/EIA 644**

TIA/EIA-644 (644) was developed by the TR30.2 committee of the TIA to address the demand for ever-increasing signaling rates and lower power consumption. It is similar to 422 in that it is a balanced signaling scheme for simplex or distributed simplex circuits. It differs in the common-mode voltage range and driver output levels, both of which reduce the maximum transmission distance relative to 422 but allow higher signaling rates, lower power, and lower EMI.

**LVDS Definition**

Low voltage differential signaling (LVDS) technology is redefining data transmission at the physical layer interface where many of the critical bottlenecks occur in any application that requires high bandwidth. LVDS brings high speeds, low power and low EMI to today's and tomorrow's networking, telecommunications and multimedia applications. It is the most promising technology for this physical layer interface.

Two new standards define LVDS, ANSI TIA/EIA-644 and IEEE 1598.3-1998. The standard TIA/EIA-644 "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits", provides a general-purpose interface for signaling rates as high as 655Mbps (megabits per second). The standard specifies the electrical characteristics of the driver and receiver, along with minimum media specifications and full-rate operation of the receiver under fault condition. It does not define functional specifications such as the hardware nor protocols. The IEEE's 1598.3-1998 "IEEE Standard for Low-Voltage Differential Signaling (LVDS) for Scalable Coherent Interface (SCI)" specifies signaling levels (electrical specifications) for the physical-layer interface and also defines signal encoding that allows transfer of SCI packet over data path. The standards are compatible and may communicate at the electrical level. The former standard is

## Low Voltage Differential Signaling (LVDS)

### LVDS

- **Low Voltage Differential Signaling**
- Signaling method used for high-speed, low-power transmission of binary data over copper.
- Intended application if for baseband data transmission over controlled impedance media of approximately 100  $\Omega$ , where the transmission media may be printed circuits board (PCB) traces, backplanes, or cables.
- Standards include
  - ANSI TIA/EIA-644
  - IEEE 1596.3

4-10

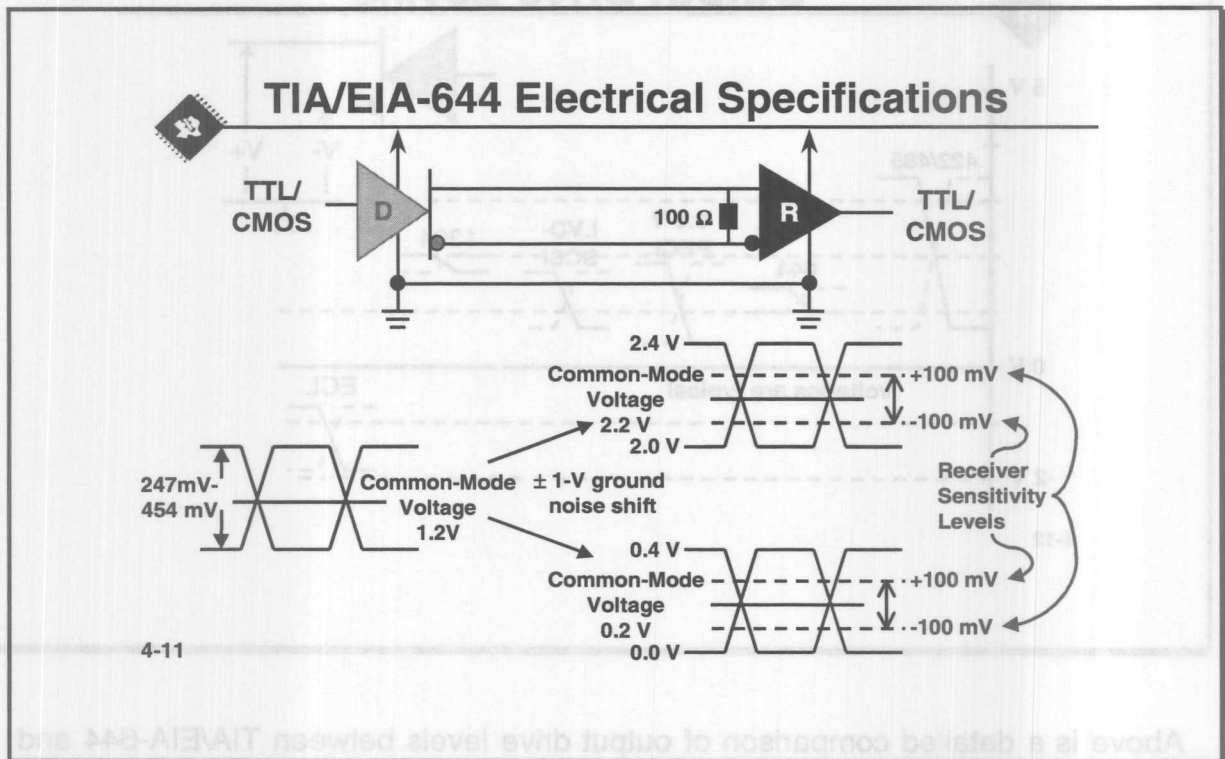
### LVDS Definition

Low voltage differential signaling (LVDS) technology is redefining data transmission at the physical layer interface where many of the critical bottlenecks occur in any application that requires high bandwidths. LVDS brings high speeds, low power and low EMI to today's and tomorrow's networking, telecommunications and multimedia applications. It is the most promising technology for this physical layer interface.

Two new standards define LVDS, ANSI TIA/EIA-644 and IEEE 1596.3-1996. The standard TIA/EIA-644 "Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits", provides a general-purpose interface for signaling rates as high as 655Mbps (megabits per second). The standard specifies the electrical characteristics of the driver and receiver, along with minimum media specifications and fail-safe operation of the receiver under fault condition. It does not define functional specifications such as the hardware nor protocols. The IEEE's 1596.3-1996 "IEEE Standard for Low-Voltage Differential Signals (LVDS) for Scalable Coherent Interface (SCI)" specifies signaling levels (electrical specifications) for the physical-layer interface and also defines signal encoding that allows transfer of SCI packet over data paths. The standards are compatible and may communicate at the electrical level. The former standard is

the more generic and popular of the two, and is the basis of the rest of this presentation and the standard TI's LVDS products meet and exceed.

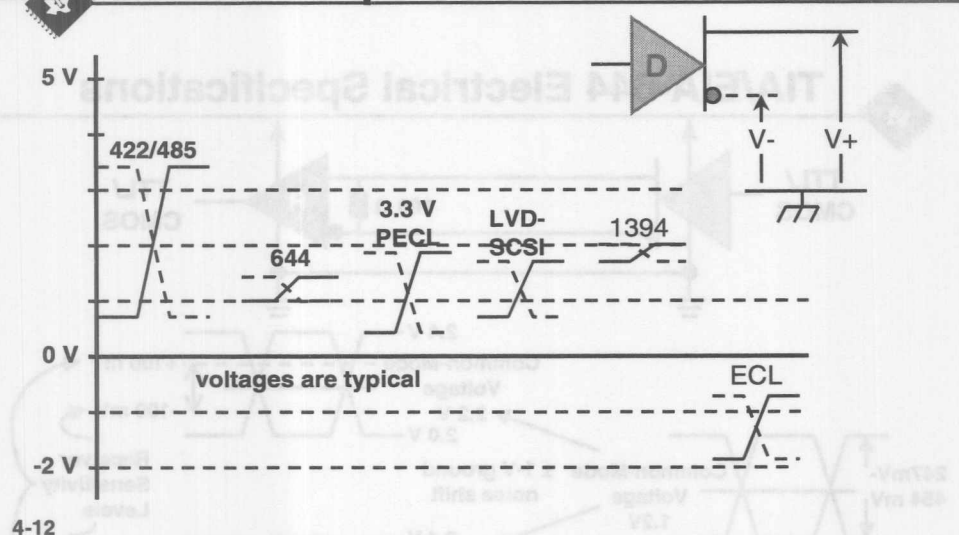
## TIA/EIA-644



### Electrical Specifications

The LVDS driver accepts TTL/CMOS input levels and transforms them using current-mode drivers to deliver a differential output in the range of 247 mV to 454 mV with a typical offset voltage of 1.2 V relative to ground. The transmission line must be terminated and matched to its impedance to complete the current loop and to terminate high speed signaling. At the end of the line, the receiver is capable of detecting signals as low as  $\pm 100$  mV with as much as  $\pm 1$ -V ground noise. The recommended voltage applied to the receiver is between ground and 2.4 V with a common mode range of 0.2 V to 2.2 V.

## Output Drive Levels



Above is a detailed comparison of output drive levels between TIA/EIA-644 and other technologies for driving 100 ohm and lower line impedance. As may be noted LVDS has one of the lowest offset voltage and lowest voltage swings. In order to transmit data over a long distance 422 and 485 need large voltage swings. PECL and ECL are both consider "power-hungry" technologies by today's standards and ECL has the disadvantage of needing to use multiple supplies. LVD-SCSI is the proposed standard of 1142-D SCSI Parallel Interface-2 (SPI-2) and has all the benefits of LVDS for multiplex applications.

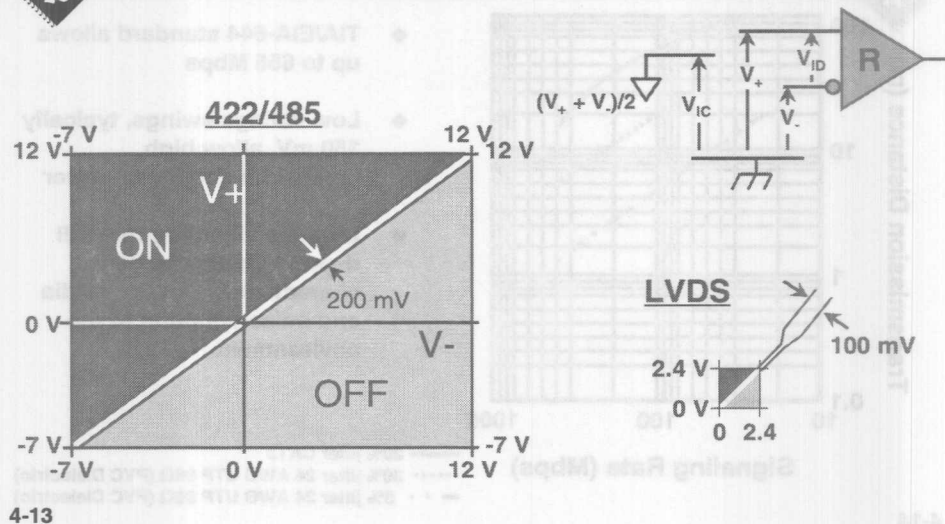
### EMI

LVDS offers low electromagnetic interference (EMI) due to its low-voltage signaling and differential data transmission. The typical 350-mV low-voltage signaling has switching currents much lower than CMOS/TTL and thus offers less radiation of EMI. Of greater importance is that the balanced differential lines have equal but opposite signals. The concentric magnetic fields radiated by each of the two conductors react with one another, bending toward each other and, ultimately, cancel a significant portion of the EMI emissions each of the two lines would generate on their own.

There are many design considerations that need to be implemented to reduce EMI. For example, signal traces must be as close to each other as possible and matched in length and there should only be one path for return current between the host controller and the target controller PCBs.

More on EMI testing may be found in TI's application note "Reducing EMI with Low Voltage Differential Signaling".

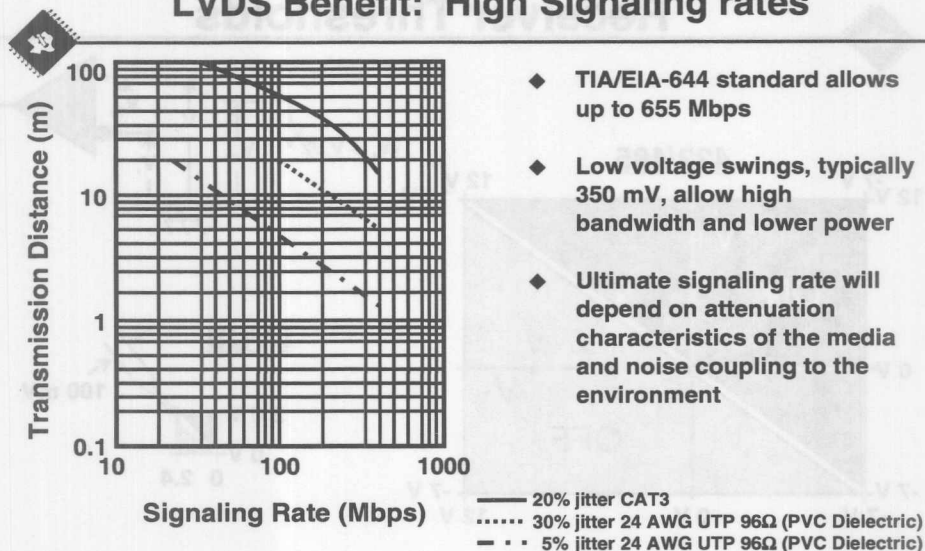
## Receiver Thresholds



Above are the LVDS receiver thresholds compared to 422/485. The threshold on 422/485 is needed for transmitting over long distances in noisy environments and thus is quite large. In order to reduce power and have high signaling rates, LVDS standard specifies a common-mode range of  $\pm 1$  V with a 1.2-V offset. Meaning the receiver threshold varies from 0 to 2.4 V. Although this range may not sound very large, it offers twice the noise margins of others reduced-swing interface standards such as BTL and GTL. Furthermore, LVDS has a receiver sensitivity of 100 mV, which offers better signal reliability as compared to 422/485's 200 mV.

## LVDS Benefits

### LVDS Benefit: High Signaling rates



4-14

TIA/EIA-644 specifies drivers and receivers capable of operating at data signaling rates up to 655Mbps, and a theoretical maximum limit is calculated at 1.923 gbps. LVDS greatly exceeds the signaling rate capabilities of former differential standards like 485 and 422. And although PECL and ECL devices are also capable of high data rates, they can consume up to 10 times more the power than LVDS.

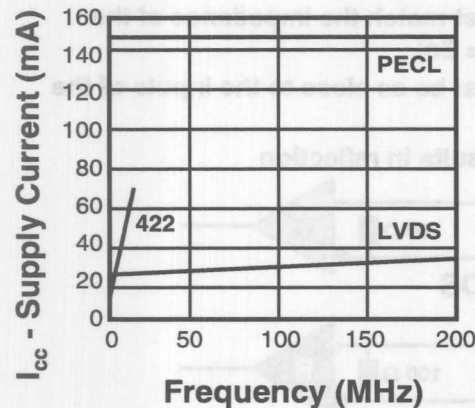
Since the differential transmission in LVDS greatly reduces noise, lower signaling swings may be used. Without the use of lower signaling swings, data rates could not be raised. The less a voltage level must change, the faster it can achieve the desired state. The LVDS signals change a maximum of 454 mV and a minimum of 247 mV, centered at 1.2 V with respect to the driver ground. These swings are several times lower than traditional TTL/CMOS swings.

LVDS devices may be used in PCB traces, backplanes, or cable environments. Since neither standard specifies a transmission media, any of the copper transmission-media options may be used. Each application has its own set of requirements, and the ultimate rate and distance of LVDS data transfer will be dependent on the attenuation characteristics of the media and the noise coupling to the environment.

The graph shown above plots different signaling rates vs. distance according to cables used when transmitting LVDS signals. Balanced cables are recommended over unbalanced cables due to their noise reduction and thus better signaling quality. As expected, on the graph it may be noted that UTP

cables have a lower performance than CAT3 cable. At high signaling rates it becomes imperative to use high quality cable such as CAT3 or CAT5.

## LVDS Benefit: Low Power



- ◆ Current-mode driver -- more power efficient than the previous voltage-mode drivers
- ◆ Low voltage swings of 350 mV
- ◆ Power consumption is relatively independent of frequency ( $I_{CC}$  vs Frequency plot)
- ◆ Ability to operate independently from the power supply voltage

4-15

Current-mode drivers and low voltage swings allow LVDS to have low power. Since LVDS is a differential transmission, noise is reduced. This allows for low voltage swings (350 mV typical) to be used which reduce power dissipation. Current-mode drivers are more power efficient than voltage-mode drivers as previously used in other standards. The current-mode drivers produce a constant current, which allows power consumption to be relatively independent of frequency. Meaning, driver power consumption remains almost constant as operating frequency increases.

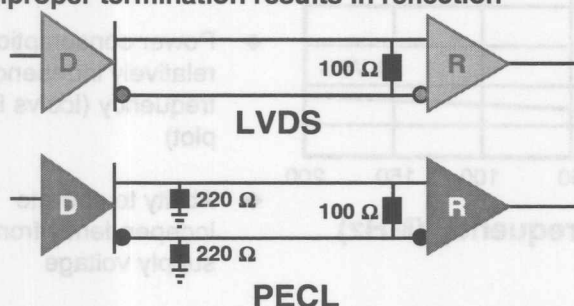
The graph above shows LVDS supply current compared to PECL and 422. As you can see the LVDS driver  $I_{CC}$  is about 1/8 that of PECL and as the frequency increases, it is also evidently lower than 422. The lower voltage of LVDS and its current-mode drivers greatly reduce power and, as shown on the graph, the  $I_{CC}$  of LVDS remains virtually flat over the frequency range.

Another characteristic of LVDS is its independence of power supply. Neither of the standards specify power-supply voltages. The supply voltage may be 5 V, 3.3 V, and even go as low as 2.7 V since the differential signal centers at 1.2 V. LVDS may be used at lower supply voltages while still maintaining the same signaling levels and performance. This feature facilitates design for systems that may be moving to lower voltages in the near future.

## Designing with LVDS

## Termination

- ◆ Single 100-Ω resistor to terminate line
- ◆ Terminating resistor must match the impedance of the transmission media ( $R_t = Z_o$ )
- ◆ Terminating resistor must be as close to the inputs of the receiver as possible
- ◆ Improper termination results in reflection

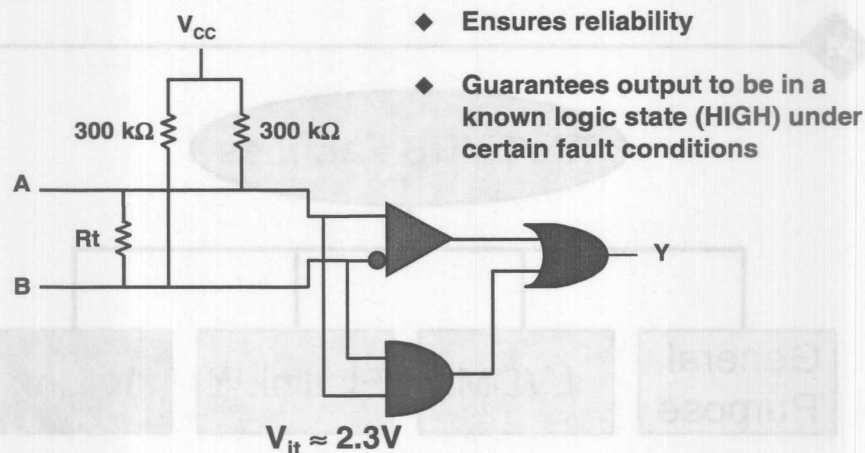


4-17

Termination at the far end of the interconnect from the transmitter is mandatory. A termination resistor matched to the impedance of the transmission media ( $\pm 10\%$ ) prevents reflections that cause noise. Ideally,  $R_t = Z_o$ . The value of the resistor is recommended to be between 90 Ω to 132 Ω. The resistor should be located within 2 cm of the LVDS receiver. Stub lengths greater than 2 cm will cause the propagating signal to bounce off the high impedance end of the stubs and degrade the signal. Proper terminations not only avoid reflection problems, but also reduce unwanted electromagnetic emissions.

The simplicity of the LVDS termination scheme makes it easy to implement in most applications. ECL and PECL require more complex terminations than the single resistor solution for LVDS. PECL drivers use two 220-Ω pull-down resistors at the outputs of the driver and a 100-Ω resistor at the input of the receiver. LVDS simplifies the layout and lowers the cost by terminating the line with a single 100-Ω resistor.

## Fail-safe receivers



4-17

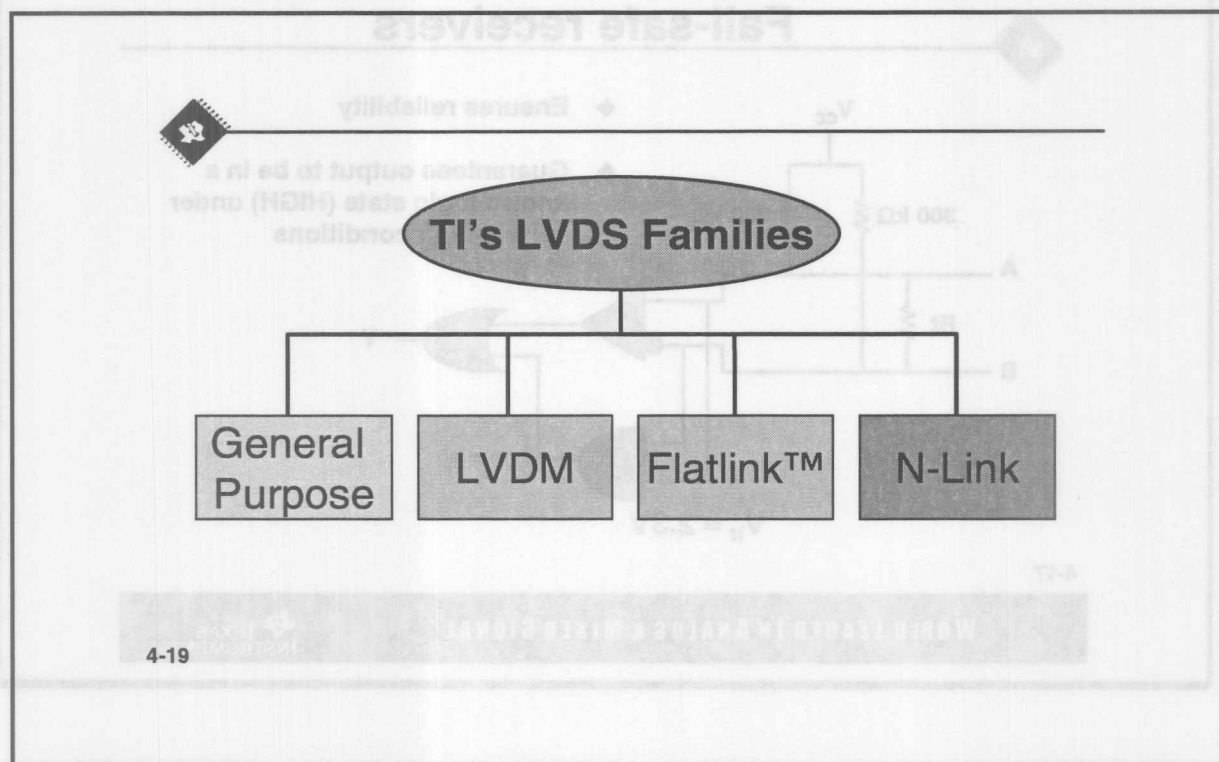
WORLD LEADER IN ANALOG &amp; MIXED SIGNAL


**TEXAS  
INSTRUMENTS**

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receivers are like most differential line receivers, in that, its output logic state can be indeterminate when the differential input voltage is between  $-100\text{ mV}$  and  $100\text{ mV}$  when within its input common-mode voltage range. This situation occurs when there is little or no input current to the receiver from the data line itself, known as open circuit. This may happen when the driver is in a high-impedance state or the cable is disconnected. The LVDS receiver is different in how it handles the open-input circuit situation however.

When the system is in open-circuit, the LVDS receiver will pull each line of the signal pair to near  $V_{CC}$  through  $300\text{-k}\Omega$  resistors as shown above. The fail-safe feature uses an AND gate with input voltage thresholds at about  $2.3\text{ V}$  to detect this condition and force the output to a high-level regardless of the differential input voltage. It is only under these conditions that the output of the receiver will be valid with less than a  $100\text{mV}$  differential input voltage magnitude. The presence of the termination resistor,  $R_t$ , does not affect the fail-safe function as long as it connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pull-up currents from the receiver and the fail-safe feature.

## LVDS Products



TI has four LVDS families that support various configurations and applications. The General-purpose, Flatlink and N-Link families meet or exceed TIA/EIA 644, the LVDM family offers all of the LVDS benefits in multiplex and half-duplex applications (note: multipoint application was not covered in 644, the standard for multipoint LVDS is currently being written and TI takes part in that committee).

**General-Purpose:**

As the name implies these are general-purpose drivers, receivers, and drivers/receivers which follow popular, industry footprints. TI offers a variety of configurations of these devices to help designers have the most cost-effective solution to their LVDS needs. This family is characterized for signaling rates up to 400 Mbps, 3.3-V power supply, and ESD greater than 8 kV.

**LVDM:**

The LVDS family allows for multiplex and half-duplex interconnections. Although this family is not under the 644 standard it offers all of the LVDS benefits. TI takes part in the committee that is working on the development of this new standard. This family requires higher output currents, more sensitive receivers, and termination at both ends of the transmission line (  $\sim 50 \Omega$  each). The devices may be used to implement any type of multipoint parallel differential bus including proprietary buses, backplane systems, and direct board-to-board connections.

Under this family there exist the LVD-SCSI transceivers which are SPI-2 compliant transceivers (SN75LVDM976/977).

## Flatlink:

Flatlink devices are PLL based transmitters and receivers with a throughput of 1.3 - 1.8 Gbps and a serialization of 28:4 and 21:3. Flatlink was developed to transfer data and control signals from portable computer video display processors to flat-panel displays.

## N-Link:

N-Link is TI's newest LVDS family, which supports the needs of networking and telecom equipment developers. N-link devices, like Flatlink, are PLL based transmitters and receivers with a throughput of 1.3 - 1.8 Gbps and serialization of 28:4 and 21:3.

The above devices all fall under the category of general-purpose LVDS products. All devices meet or exceed TIA/EIA-644 and have some general characteristic in common. For example, all devices in the general-purpose category are single 3.3-V supply voltages and have a minimum of 8 kV ESD on the bus pins. These features, and all those shown on the slide, provide substantial benefits that enhance a system's performance resulting in total system cost savings.

The General-purpose products may be used in simplex and distributed simplex interconnections. The simplex interconnection is the preferred solution. Signal quality is superior in this uncomplicated configuration since no stubs or discontinuity in impedance are present. In distributed simplex configuration up to 17 receivers with no common-mode termination and up to 36 receivers with common-mode termination may be tied to the bus. The stubs between the line and each receiver must be kept to a minimum (<7 mm) since at high signaling rates they may act as transmission lines creating reflections and they may also cause an impedance discontinuity. A terminating resistor must only be placed at the end of the transmission line as shown above. Multiple terminating resistors would attenuate the signal since they would present a low impedance load to the driver.

SN75LVDS31/32 16-pin quad driver and receiver are the first general-purpose devices TI released. They follow the popular pin-out (footprint) of AM26LV31 and AM26LV32.

## General-Purpose Products

# General-Purpose Products

The Texas Instruments logo, featuring a stylized diamond shape with a 'T' and 'I' inside, and a small 'TI' monogram below it.

## Drivers

SN65LVDS31  
quad

SN65LVDS3487  
quad with enable

SN65LVDS9638  
dual

## Receivers

SN65LVDS32  
quad

SN65LVDS3486  
quad with enable

SN65LVDS9637  
dual

## Drivers/ Receivers

SN65LVDS051\*  
dual with  
drivers enable

SN65LVDS050\*  
dual with drivers and  
receivers enable

SN65LVDS180\*  
single with driver and  
receiver enable

SN65LVDS179\*  
single

SN65LVDS22\*  
Mux/demux

\* Available 4Q98

4-20

The above devices all fall under the category of general -purpose LVDS products. All devices meet or exceed TIA/EIA-644 and have some general characteristic in common. For example, all devices in the general-purpose category are single 3.3-V supply voltages and have a minimum of 8 kV ESD on the bus pins. These features, and all those shown on the slide, provide substantial benefits that enhance a system's performance resulting in total system cost savings.

The General-purpose products may be used in simplex and distributed simplex interconnections. The simplex interconnection is the preferred solution. Signal quality is superior in this uncomplicated configuration since no stubs or discontinuity in impedance are present. In distributed simplex configuration up to 17 receivers with no common-mode termination and up to 36 receivers with common-mode termination may be tied to the bus. The stubs between the line and each receiver must be kept to a minimum (<7 mm) since at high signaling rates they may act as transmission lines creating reflections and they may also cause an impedance discontinuity. A terminating resistor must only be placed at the end of the transmission line as shown above. Multiple terminating receivers would attenuate the signal since they would present a low impedance load to the driver.

SN65LVDS31/32-16-pin quad driver and receiver are the first general-purpose devices TI released. They follow the popular pin-out (footprint) of AM26LS31 and AM26LS32.

SN65LVDS3486/87-16-pin quad driver and receiver which feature an enabling scheme whereby only two of the four drivers or receivers may be enabled at a time instead of requiring that all four lines are enabled simultaneously as is the case with the 'LVDS31/32.

SN65LVDS9637/9638-8-pin dual driver and receiver have the same innovative characteristics as the quad drivers and receivers. These devices follow the industry's standard pin-configuration of  $\mu$ A9638 and  $\mu$ A9637 for easy flow-through interconnections.

SN65LVDS179/180-each has a single driver/receiver. The 'LVDS179 comes in an efficient 8-pin package. The 'LVDS180 feature an enabling scheme which allows the device to be used as a single driver, or as a single receiver, or as a driver/receiver; it is in a 14-pin package.

SN65LVDS050/051- both devices contain two drivers and two receivers. The 'LVDS050 has an enabling scheme that allows the designer to operate only the drivers, or only the receivers, or all the drivers/receivers. The 'LVDS051 has an enabling scheme for the drivers only. The designer can choose to operate both drivers or only one driver. Both devices are 16-pin packages

SN65LVDS22-It's a dual 2:1 mux or 1:2 splitter with LVDS inputs and outputs. The receiver outputs can be switched to either driver or both drivers through multiplexer control signals. This characteristic allows the flexibility to perform splitter or signal routing functions with a single device. This product solves many of the designer's headaches of muxing and splitting signals in a one-chip LVDS solution. The 'LVDS22 is also available with twice the output current to accommodate multipoint applications and it is designated the SN65LVDM22 featured in the next slide.



## **General-Purpose Products Features**

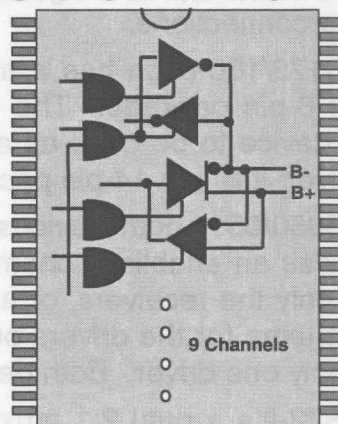
- **Signaling rates up to 400 Mbps**
- **Low-power**
  - **25 mW/driver at 400 Mbps**
  - **60 mW/receiver at 400 Mbps**
- **ESD protection exceeds 8 kV (HBM) on bus pins**
- **Single 3.3-V power supply**
- **5-V tolerance on LVTTTL pins of drivers/receivers**

4-21

## **LVDM Product:**

### **SN75LVDM976 and SN75LVDM977**

- 9 channel dual-mode SCSI transceiver
- Supports single-ended and LVD-SCSI
- Up to 40 Mxfer/s
- 'LVDM976 -- CMOS
- 'LVDM977 -- TTL



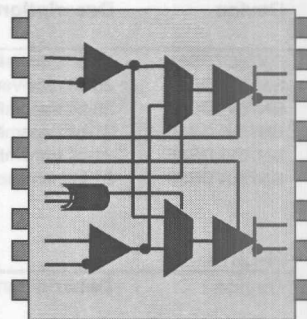
4-22

TI's LVDM products are the ultimate solution to multiplex and half-duplex interconnections. These products enable bi-directional connections while still enjoying all the LVDS benefits. Their application usually includes any type of multipoint differential bus including proprietary buses, backplane systems and direct board-to-board connections.

The SN75LVDM976/977 were the first discrete transceivers in the industry to support both single-ended and LVD signaling. These devices allow designers to upgrade their small computer system interface (SCSI) peripheral devices and other products like SCSI host bus adapters to the faster data transfer rates and longer bus segments of LVD-SCSI while still maintain compatibility with existing single-ended signaling. The LVDM976/977 has all of the benefits of LVDS such as significant power reduction and low EMI. They are available in TSSOP packaging with 20-mil lead pitch, which reduces the board area and follows the popular pin-out of its predecessor SN75976A.

## LVDM Product: SN65LVDM22

- Dual multiplexed LVDS repeater
- Performs splitter or signal routing functions
- Single 3.3-V power supply
- Up to 400 Mbps
- Available 4Q98



4-23

The SN65LVDM22 is a dual 2:1 mux or 1:2 splitter with LVDS inputs and outputs. The receiver outputs can be switched to either driver or both drivers through multiplexer control signals. This characteristic allows the flexibility to perform splitter or signal routing functions with a single device. This product solves many of the designer's headaches of muxing and splitting signals in a one-chip LVDS solution. The 'LVDM22 has twice the output current than the SN65LVDS22 (general-purpose LVDS) in order to support multipoint applications.

\*\*Device available 4Q98\*\*

## Flatlink and N-link Products

### Flatlink

| Device     | Description        | Throughput<br>(MHz) | Clock<br>Trigger | TSSOP<br>Package |
|------------|--------------------|---------------------|------------------|------------------|
| SN75LVDS81 | 28-bit transmitter | 68                  | falling          | 56-pin           |
| SN75VLDS82 | 28-bit receiver    | 68                  | falling          | 56-pin           |
| SN75VLDS83 | 28-bit transmitter | 68                  | selectable       | 56-pin           |
| SN75VLDS84 | 21-bit transmitter | 68                  | falling          | 48-pin           |
| SN75VLDS85 | 21-bit transmitter | 68                  | rising           | 48-pin           |
| SN75VLDS86 | 21-bit receiver    | 68                  | falling          | 48-pin           |

### N-Link

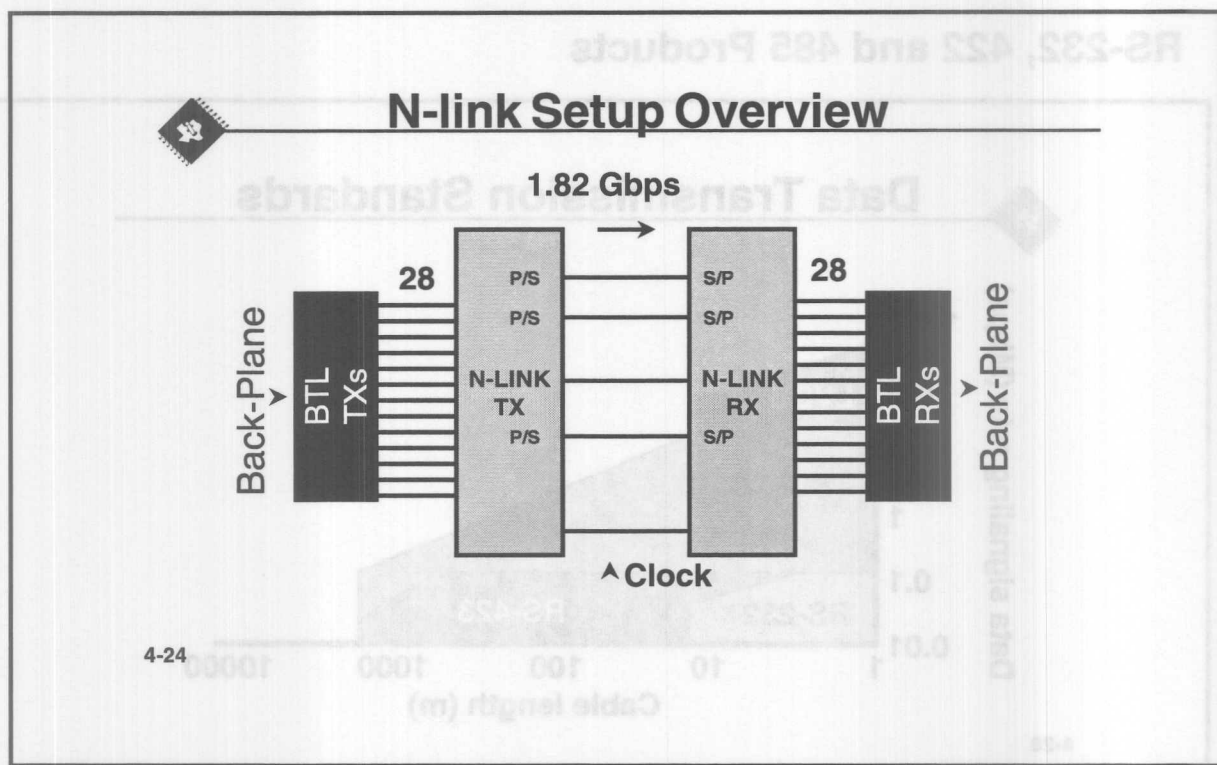
| Device     | Description        | Throughput<br>(MHz) | Clock<br>Trigger | TSSOP<br>Package |
|------------|--------------------|---------------------|------------------|------------------|
| SN65LVDS93 | 28-bit transmitter | 68                  | selectable       | 56-pin           |
| SN65VLDS94 | 28-bit receiver    | 68                  | rising           | 56-pin           |
| SN65VLDS95 | 21-bit transmitter | 68                  | rising           | 48-pin           |
| SN65VLDS96 | 21-bit receiver    | 68                  | rising           | 48-pin           |

4-25

Currently, developers are using proprietary solutions that often require a large number of parallel lines in order to meet their high bandwidth backplane interconnect requirements. As bandwidth requirements increase over time, these designs will become more complicated. Flatlink and N-Link provide developers with a more elegant solution and a better performance roadmap that does not require a complete re-design to their equipment.

Some of the advantages of Flatlink and N-link include:

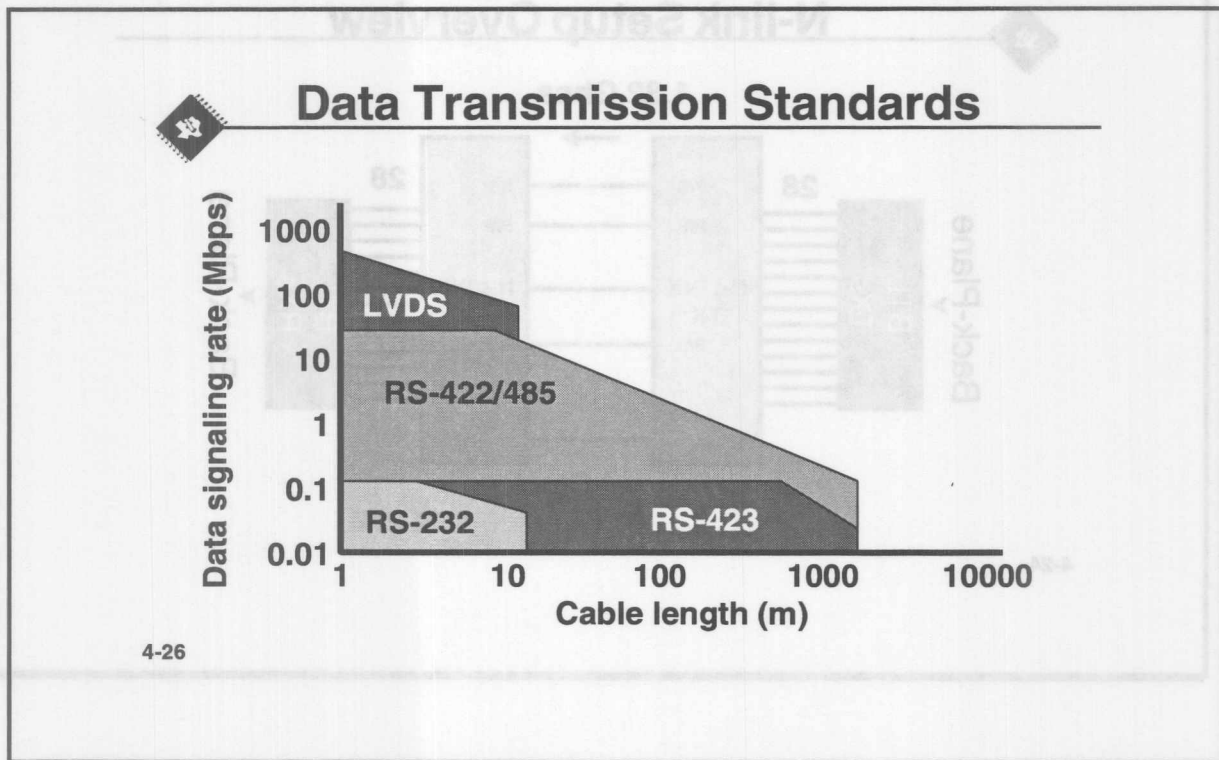
- Substantial reduction in cable size
- No ground referencing needed
- Reduction of EMI
- Overall throughput of 1.82 Gbps
- Power down mode = 1mW
- Simpler design , More cost effective, Faster time to market



N-Link can provide multiple Gbps of throughput in any one direction. The above application can easily be replicated in the opposite direction to provide a full duplex solution running at 1.8 Gbps.

Each of the LVDS lines above actually represent an LVDS balanced twisted pair cable or copper trace pair. This enables N-link to serialize 28 data channels into 4 LVDS balanced pairs for transmission to the receiver in addition a clock line is also sent to the receiver to synchronize the PLL.

## RS-232, 422 and 485 Products



As shown in the beginning of this presentation, besides LVDS there are other standards which TI supports. TI has 30 years of experience in the Data Transmission arena; and it is therefore no wonder that along with its efforts to extend the data transmission capabilities of new technologies like LVDS, it also continues to improve currently implemented transmission specifications such as 232, 422, 485, and others.

The preceding are some more of TI's products offerings in Data Transmission.

## **TI's 422/485 Technology Selection**

|                  | <u>172</u>            | <u>173</u> | <u>174</u> | <u>175</u>        | <u>176</u> | <u>179</u> | <u>180</u>        | <u>184</u> |
|------------------|-----------------------|------------|------------|-------------------|------------|------------|-------------------|------------|
| <b>Bipolar</b>   | X                     | X          | X          | X                 | X          | X          |                   |            |
| <b>ALS</b>       | X                     | X          | X          |                   | X          |            | X                 |            |
| <b>LBC</b>       | X                     | X          | X          | X                 | X          | X          | X                 | X          |
|                  | <b><u>Bipolar</u></b> |            |            | <b><u>ALS</u></b> |            |            | <b><u>LBC</u></b> |            |
| <b>Power</b>     | high                  |            |            | moderate          |            |            | <b>LOW</b>        |            |
| <b>Max Speed</b> | 10 Mbps               |            |            | <b>30 Mbps</b>    |            |            | 12 Mbps           |            |
| <b>Cost</b>      | <b>LOW</b>            |            |            | moderate          |            |            | higher            |            |

4-27

TI's 422/485 family may be easily arranged into 3 sub-categories according to the technology used: 1) Bipolar, 2) Advanced low-power Schottky (ALS), and 3) LinBiCMOS™ (LBC). Depending on the system specifications, one of these sub-categories may well fit the specific system care-about. For example, if a designer's concern is low power in a 485 device, s/he would be advice to look into the LBC family of TI's 422/485 products. LinBiCMOS technology has the best features of CMOS and bipolar processes of fast switching speeds, low quiescent power, high voltage breakdowns, voltage or current precision, and stability.

By offering different technologies in 422/485 products, TI aims to provide the most innovative and complete product offering in the industry. This broad selection of products is bound to give the designer the most cost-effective and easy-to-design-with solution for their data transmission needs in 422/485.

# TIA/EIA-485 Products

|                                                      | Driver/<br>Receiver | Device       | Key                   |
|------------------------------------------------------|---------------------|--------------|-----------------------|
| Line<br>Drivers                                      | 4/0                 | SN75172      | Industry Standard     |
|                                                      |                     | SN75174      | Industry Standard     |
|                                                      |                     | SN75ALS172A  | High Speed            |
|                                                      |                     | SN75ALS174A  | High Speed            |
|                                                      |                     | SN75LBC172   | Low Power             |
|                                                      |                     | SN75LBC174   | Low Power             |
| Line<br>Receivers                                    | 0/4                 | SN75173      | Industry Standard     |
|                                                      |                     | SN75175      | Industry Standard     |
|                                                      |                     | SN75ALS173   | High Speed            |
|                                                      |                     | SN75LBC173   | Low Power             |
|                                                      |                     | SN75LBC175   | Low Power             |
|                                                      |                     |              |                       |
| Line<br>Transceivers<br><br>(Drivers /<br>Receivers) | 1/1                 | SN75176A     | Reduced Slew-rate     |
|                                                      |                     | SN75176B     | Industry Standard     |
|                                                      |                     | SN75178B     | Standard Repeater     |
|                                                      |                     | SN75179B     | Industry Standard     |
|                                                      |                     | SN75ALS176   | High Speed            |
|                                                      |                     | SN75ALS176A  | Very High Speed       |
|                                                      |                     | SN75ALS176B  | Ultra High Speed      |
|                                                      |                     | SN75LBC176   | Ultra- Low Power      |
|                                                      |                     | SN75LBC179   | Low Power             |
|                                                      |                     | SN75ALS180   | Full Duplex Com       |
|                                                      |                     | SN75LBC180   | Low Power             |
|                                                      |                     | SN75ALS181   | Full Duplex Com       |
|                                                      |                     | SN75LBC184   | Transient Suppression |
|                                                      | 2/2                 | SN751177     | High Speed            |
|                                                      |                     | SN751178     | High Speed            |
|                                                      |                     | SN75ALS1177  | High Speed            |
|                                                      |                     | SN75ALS1178  | High Speed            |
|                                                      | 3/3                 | SN75ALS170   | High Speed            |
|                                                      |                     | SN75ALS170A  | High Speed, Low power |
|                                                      |                     | SN75ALS171   | High Speed            |
|                                                      | 9/9                 | SN75ALS171A  | High Speed, Low power |
|                                                      |                     | SN75976A1/A2 | High Speed            |
|                                                      |                     | SN75LBC978   | Low Power + WRAP      |
|                                                      |                     | SN75LBC968   | Active Termination    |

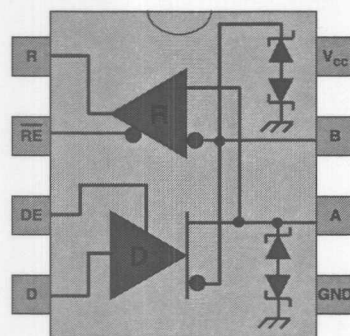
4-28

Standards, such as 485 and 422, are differential technologies that are used in a broad selection of general-purpose applications, including industrial control, telecommunications, point-of-sale terminals, alarm systems and other environments that are high in electrical interference. TI offers a wide variety of these products which include many combinations of drivers, receivers and transceivers. Among TI's 485 products also exist 9-channel SCSI transceivers, which have taken differential SCSI into a new level of performance. TI's discrete SCSI transceivers such as the SN75976A and the SN75LBC976 offer designers a cost-effective solution to their multipoint applications without having to adhere to expensive ASICs. TI also offers single-ended SCSI transceivers such as the SN75LBC968 and LVD-SCSI transceivers such as the SN75LVDM976/977 (shown previously).



**RS-485 Transceiver with Transient Suppression**

**SN65LBC184 and SN75LBC184**



SN65LBC184  
SN75LBC184

- Integrated transient voltage suppression (400-W peak)
- 15-kV ESD on bus pins (IEC1000-4-2 compliance)
- Improved data transmission at 250 Kbps
- 1/2 unit load -- up to 64 similar devices connected on a bus
- Controlled driver slew rates

4-29

The SN65/75LBC184 is the industry's first '176 standard footprint 485 differential transceiver to offer integrated transient voltage protection up to 400-W peak. The SN65/75LBC184 provides significant protection from large over-voltage transients on the bus pins, which can be caused by secondary effects of a lightning strike or power system switching disturbances.

These devices are well suited for electrically noisy environments requiring large over-voltage and common mode swing protection. The SN75LBC184 and SN65LBC184 provide substantial benefits for improved reliability and enhanced system performance resulting in total system cost savings.

Transient voltage suppression – protection from large noise transients to reduce down time

Integrated solution – on-chip to minimize cost and printed board-space requirement

Controlled driver slew rates – for reduced EMI and improved data transmission at 250 Kbps over longer unterminated cable runs and stub lengths

15 kV ESD (HBM)– Improves system's reliability.

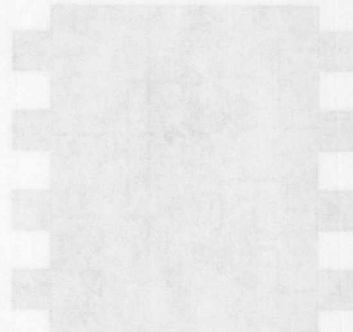
Half unit load – for up to 64 similar devices connected on a bus

Compatibility – drop-in replacement of current '176 designs and meets or exceeds EIA RS-485 and ISO/IEC 8482:1993(E) standards.

The SN65/75LBC184 is a cost-effective, footprint-compatible, device delivering a high level of bus protection without the need of external discrete clamping diodes and costly multi-chip modules.

These devices are available in 8-pin DIP and SOIC. The SN65LBC184 is characterized for industrial temperatures (-40° to 80 ° C) while the SN75LBC184 is characterized for commercial temperature (0 ° to 70 ° C)

- Integrated transient voltage suppression (400-W peak)
- 15-kV ESD on bus pins (IEC1000-4-2 compliance)
- Improved data transmission at 250 Kbps
- 1/2 unit load -- up to 64 similar devices connected on a bus
- Controlled driver slew rates



SN65LBC184  
SN75LBC184

4-32

The SN65/75LBC184 is the industry's first 178 standard footprint 485 differential transceiver to offer integrated transient voltage protection up to 400-W peak. The SN65/75LBC184 provides significant protection from large over-voltage transients on the bus pins, which can be caused by secondary effects of a lightning strike or power system switching disturbances.

These devices are well suited for electrically noisy environments requiring large over-voltage and common mode swing protection. The SN75LBC184 and SN65LBC184 provide substantial benefits for improved reliability and enhanced system performance resulting in total system cost savings.

Transient voltage suppression -- protection from large noise transients to reduce down time

Integrated solution -- on-chip to minimize cost and printed board-space requirement

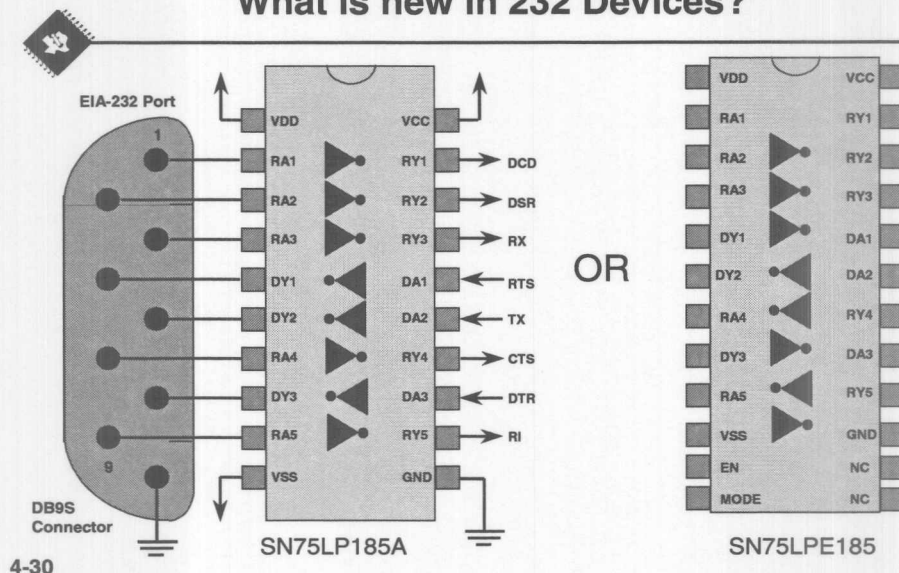
Controlled driver slew rates -- for reduced EMI and improved data transmission at 250 Kbps over longer unterminated cable runs and stub lengths

15 kV ESD (HBM) -- improves system's reliability

Half unit load -- for up to 64 similar devices connected on a bus

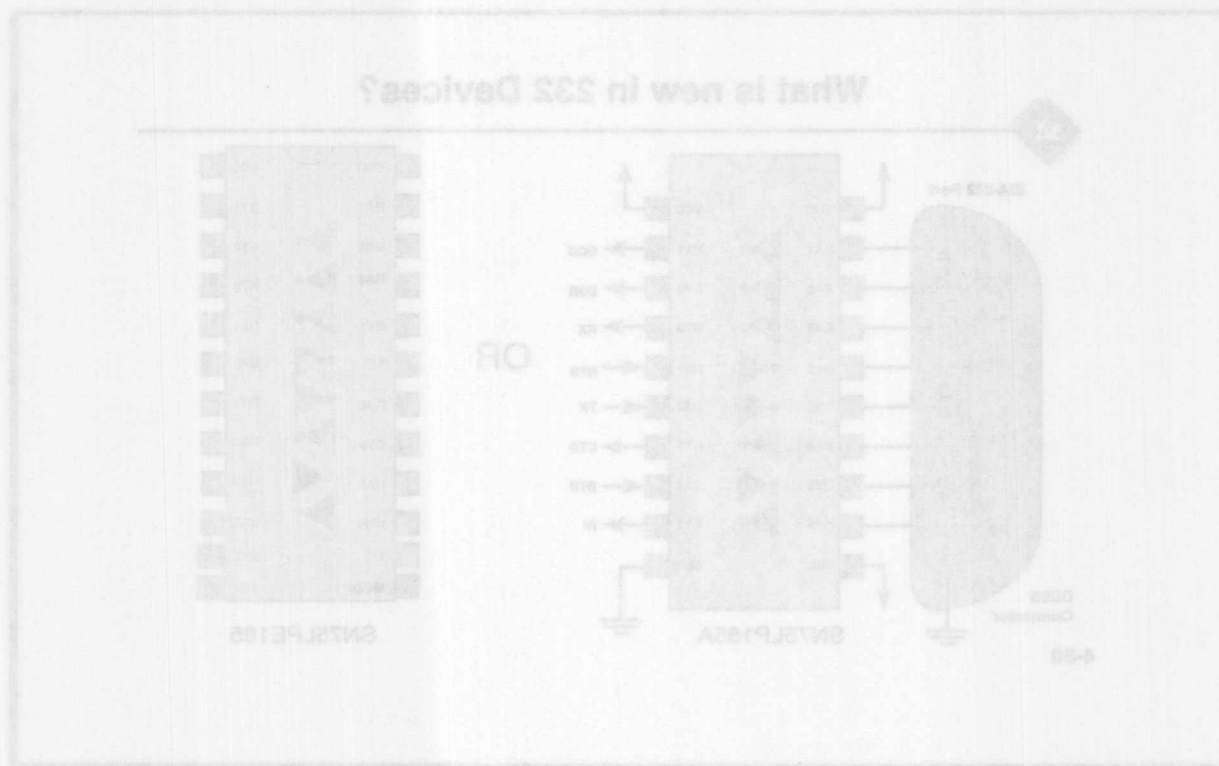
Compatibility -- drop-in replacement of current 178 designs and meets or exceeds EIA RS-485 and ISO/IEC 8485:1993(E) standards.

# What is new in 232 Devices?



The SN75LP185A and SN75LPE185 shown above are application specific to the 9-pin DB9S Personal computer Data Terminal Equipment (DTE) serial interface, which effectively is a subset of the full 232 standard. As a semiconductor manufacturer, TI finds that the majority of 232 applications are moving to this interface. Due to the nature of the signals (five receiver and three transmit line), the older established 232 products no longer provide an optimum solution. This interface is now driving the need for single-chip 232 solutions. Additional features such as single-supply operation, higher data-signaling rates, voltage-clamped outputs, increased ESD protection, and power-down modes have evolved from the desirable features to the essential features of today's interface.

The SN75LP185A and SN75LPE185 are one of TI's first products in this new Family of Next Generation 232 devices. These devices are low-power bipolar products containing three drivers and five receivers with 15-kV ESD protection on the bus pins with respect to each other. The pin-out of the 'LP185A matches the flow-through design of the industry-standard SN75185 and SN75C185. The 'LPE185 also follows this same flow-through pin-out, but it adds four pins for control signals. The 'LPE185 has flexible control options for power management when the serial power is inactive. The flow-through pin-out of both devices allows easy interconnection of the UART and serial-port connector of the IBM PC/AT and compatible. The 'LP185A and 'LPE185 combine high data rates (250 kbps), high ESD (15 kV HBM), low power (13.95mW), EMI reduction circuitry, relatively low cost, and the power of TI's World Wide sales and distribution network to the deliver the most resourceful 232 product in the market.



The SN75LP185A and SN75LP185B shown above are application specific to the 8-pin DB9 Personal Computer Data Terminal Equipment (DTE) serial interface, which effectively is a subset of the full 332 standard. As a semiconductor manufacturer, TI finds that the majority of 332 applications are moving to this interface. Due to the nature of the signals (five receiver and three transmit lines), the older established 332 products no longer provide an optimum solution. This interface is now driving the need for single-chip 332 solutions. Additional features such as single-supply operation, higher data-signaling rates, voltage-clamped outputs, increased ESD protection, and power-down modes have evolved from the desirable features to the essential features of today's interface.

The SN75LP185A and SN75LP185B are one of TI's first products in this new Family of Next Generation 332 devices. These devices are low-power bipolar products containing three drivers and five receivers with 15-kV ESD protection on the bus pins with respect to each other. The pin-out of the LP185A matches the flow-through design of the industry-standard SN75185 and SN75C185. The LP185 also follows the same flow-through pin-out, but it adds four pins for control signals. The LP185 has flexible control options for power management when the serial power is inactive. The flow-through pin-out of both devices allows easy interconnection of the UART and serial-port connector of the IBM PC/AT and compatible. The LP185A and LP185B combine high data rates (250 kbps), high ESD (15 kV HBM), low power (13.95mW), EMI reduction circuitry, relatively low cost, and the power of TI's World Wide sales and distribution network to deliver the most resourceful 332 product in the market.

**For more information:**

**<http://www.ti.com>**

**Engineering Design Center**

Product Information

Development Support

Specialized Searches

**<http://www.ti.com/sc/docs/eedesign.htm>**

**Mixed Signal and Analog Products**

Product Information

Device/Documentation Search

**<http://www.ti.com/sc/docs/msp/prodinfo/prodinfo.htm>**

**Mixed Signal & Analog Marketing**

New products

Interesting announcements

Individual home pages for each product family

Links to Showcase

Link to Sine-On

**<http://www.ti.com/sc/docs/msp/msphome.htm>**

## TI Worldwide Technical Support

### Internet

TI Semiconductor Home Page

<http://www.ti.com/sc>

TI Distributors

<http://www.ti.com/sc/docs/distmenu.htm>

### Product Information Centers

#### Americas

Phone +1(972) 644-5580

Fax +1(972) 480-7800

Email [sc-infomaster@ti.com](mailto:sc-infomaster@ti.com)

#### Europe, Middle East, and Africa

Phone

Deutsch +49-(0) 8161 80 3311

English +44-(0) 1604 66 3399

Francais +33-(0) 1-30 70 11 64

Italiano +33-(0) 1-30 70 11 67

Fax +33-(0) 1-30-70 10 32

Email [epic@ti.com](mailto:epic@ti.com)

#### Japan

Phone

International +81-3-3457-0972

Domestic +0120-81-0026

Fax

International +81-3-3457-1259

Domestic +0120-81-0036

Email [pic-japan@ti.com](mailto:pic-japan@ti.com)

## Product Information Centers (continued)

### Asia

#### Phone

International +886-2-23786800

Domestic Local Access Code TI Number

Australia 1-800-881-011 -800-800-1450

China 10811 -800-800-1450

Hong Kong 800-96-1111 -800-800-1450

India 000-117 -800-800-1450

Indonesia 001-801-10 -800-800-1450

Korea 080-551-2804 -Malaysia

1-800-800-011 -800-800-1450

New Zealand +000-911 -800-800-1450

Philippines 105-11 -800-800-1450

Singapore 800-0111-111 -800-800-1450

Taiwan 080-006800 -Thailand

0019-991-1111 -800-800-1450

Fax 886-2-2378-6808

Email [tiasia@ti.com](mailto:tiasia@ti.com)

Important Notice: The products and services of Texas Instruments and its subsidiaries described herein are sold subject to TI's standard terms and conditions of sale. Customers are advised to obtain the most current and complete information about TI products and services before placing orders. TI assumes no liability for applications assistance, customer's applications or product designs, software performance, or infringement of patents. The publication of information regarding any other company's products or services does not constitute TI's approval, warranty or endorsement thereof.

A060198

## Product Information Centers (continued)

### Asia

#### Phone

International +886-2-23788800

Domestic Local Access Code TI Number

Australia 1-800-881-011-800-800-1450

China 10811-800-800-1450

Hong Kong 800-98-1111-800-800-1450

India 000-117-800-800-1450

Indonesia 001-801-10-800-800-1450

Korea 080-521-2804-Malaysia

1-800-800-011-800-800-1450

New Zealand +000-911-800-800-1450

Philippines 102-11-800-800-1450

Singapore 800-0111-111-800-800-1450

Taiwan 080-008800-Thailand

0019-991-1111-800-800-1450

Fax 886-2-2378-6808

Email [asia@ti.com](mailto:asia@ti.com)

Important Notice: The products and services of Texas Instruments and its subsidiaries described herein are sold subject to TI's standard terms and conditions of sale. Customers are advised to obtain the most current and complete information about TI products and services before placing orders. TI assumes no liability for applications assistance, customer's applications or product design, software performance, or integration of products. The publication of information regarding any other company's products or services does not constitute TI's approval, warranty or endorsement thereof.

ADG0138